Diffraction Control Unit
PW1710/00

Service Manual

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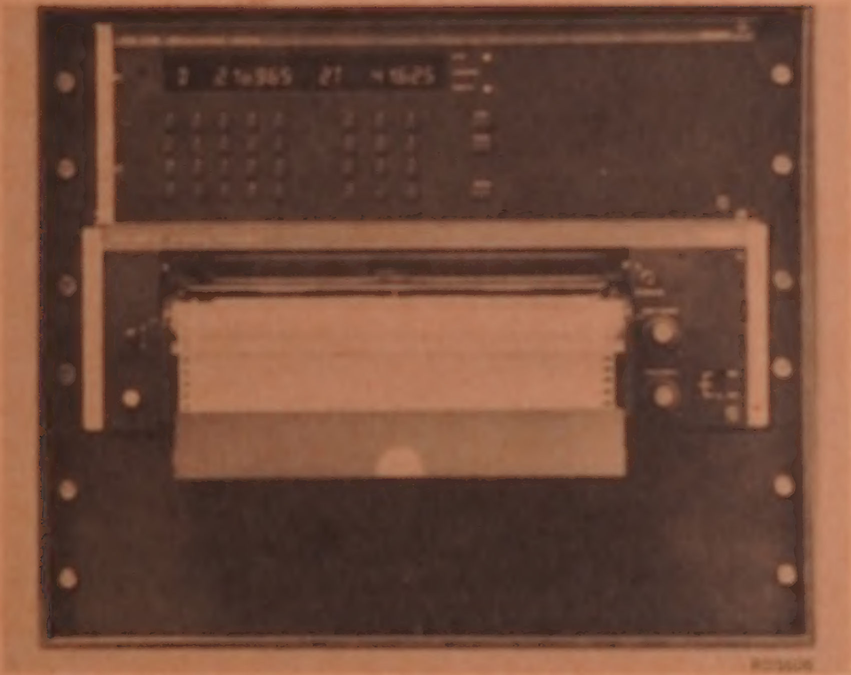

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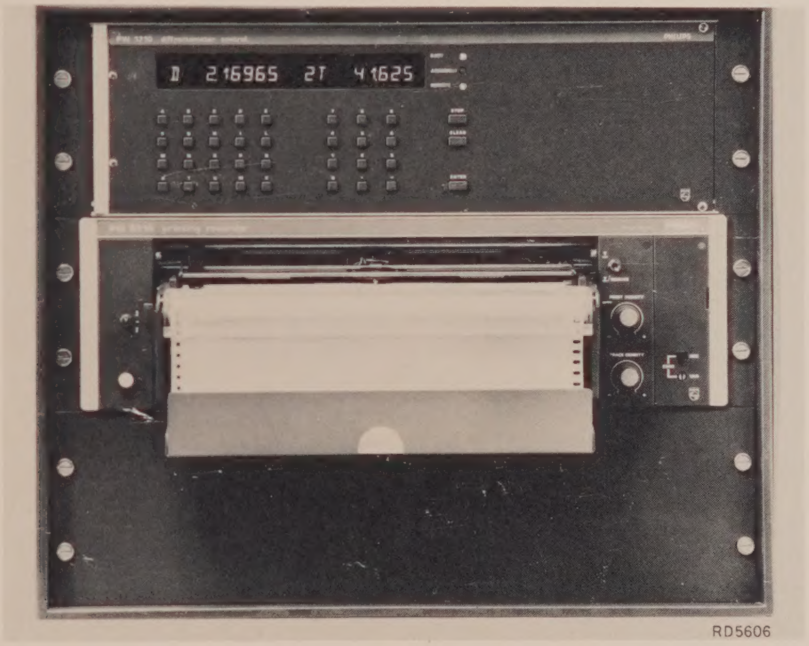
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CHAPTER 1. INTRODUCTION

CHAPTER 2. INSTALLATION

CHAPTER 3. SYSTEM DESCRIPTION

CHAPTER 4. HARDWARE DESCRIPTION

CHAPTER 5. SOFTWARE DESCRIPTION

CHAPTER 6. FAULT FINDING

CHAPTER 7. SPARE PARTS LIST

APPENDIX A. WIRING INFORMATION

APPENDIX B. V24/CURRENT LOOP PRINCIPLES

PW1710/00 Service Manual.

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*   *
*   DURING AND AFTER EVERY MAINTENANCE AND REPAIR   *
*   OPERATION ALL SAFETY PROCEDURES AND CHECKS MUST BE   *
*   CARRIED OUT ACCORDING TO THE GUIDE-LINES IN THE   *
*   GENERAL SAFETY MANUAL AND RELEVANT INSTALLATION AND   *
*   OPERATING MANUALS.   *
*   *
****

EDITION NOTICE 2nd Edition JUNE 1985

This is the first edition of this publication and is intended for use with the PW1710/00.

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1.1 INTRODUCTION

1.1.1 SYSTEM DESCRIPTION

The PW1710 is a microprocessor based control and measuring system, designed to provide Philips x-ray diffractometers with differing levels of automation.

Upgrading of existing diffractometer systems to a medium or high degree of automation is possible by adding the PW1710 with or without a computer.

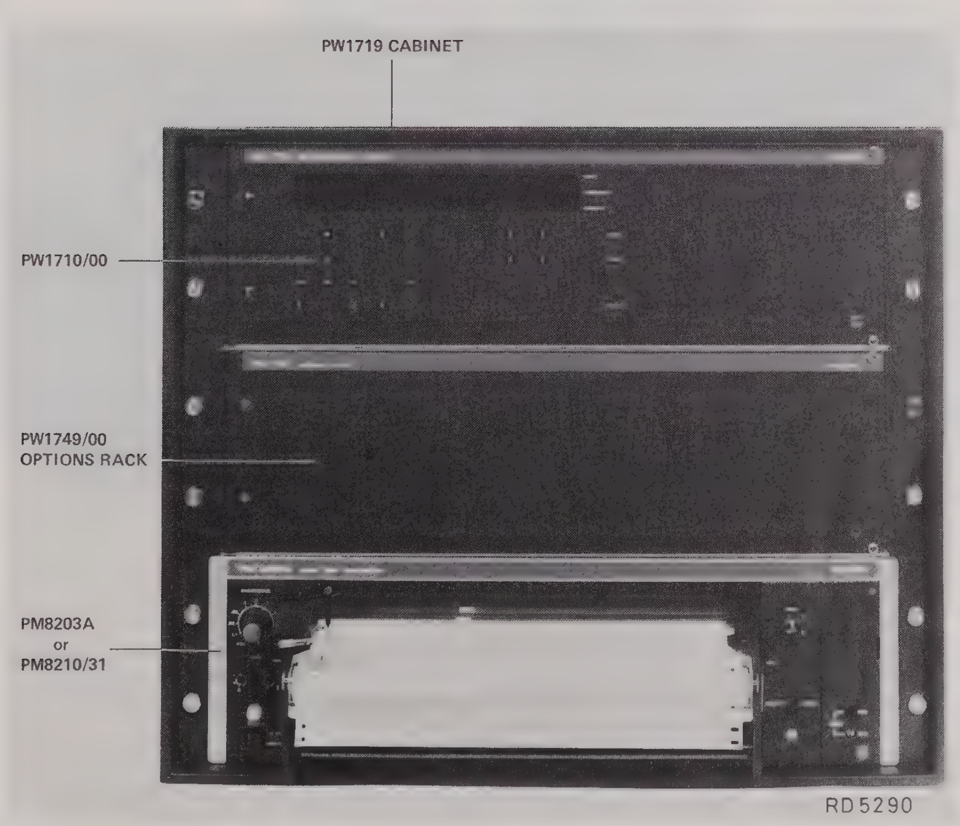
PW1719 CABINET
PW1710/00
PW1749/00
OPTIONS RACK
PM8203A
or
PM8210/31
RD5290

Figure 1.1 PW1710 System Fitted into a PW1719 Cabinet

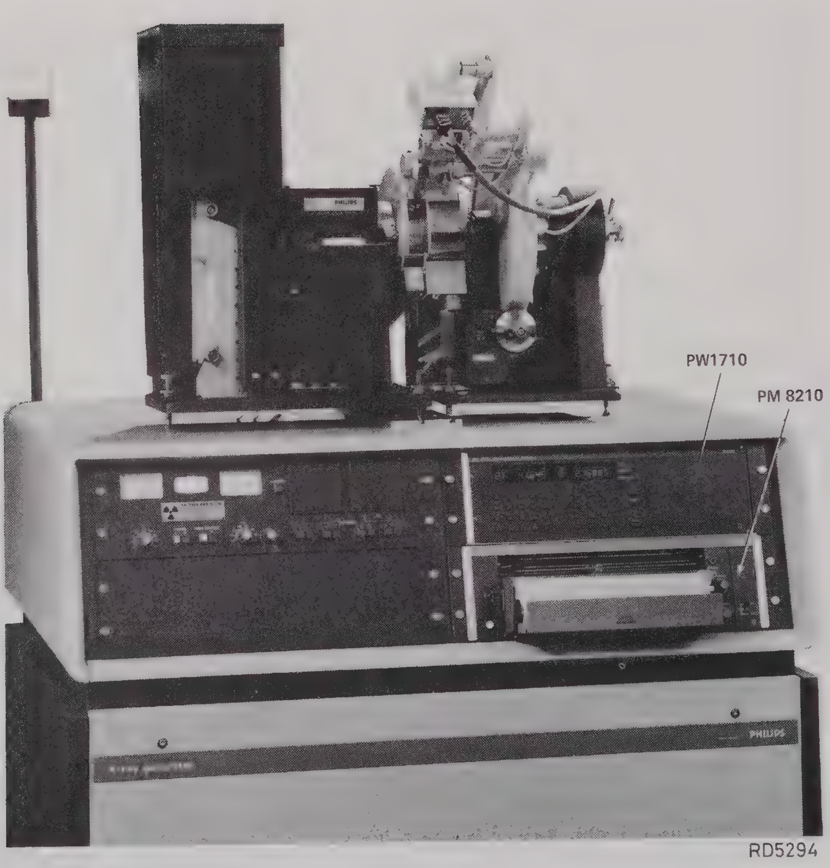

Figure 1.2 PW1710 Housed in a PW1730 Generator

The PW1710 provides four major functions, these are :

1. CONTROL OF X-RAY DIFFRACTOMETER.
2. MEASUREMENT AND PROCESSING OF X-RAY INTENSITIES.
3. CONTROL OF PERIPHERALS SUCH AS VDUs AND/OR COMPUTERS.
4. EXECUTION OF COMMANDS AND USER-MADE PROGRAMS.

1.1.2 MECHANICAL DESCRIPTION

The system comprises two modules:

The Control Module which houses the electronics

The Power Module which houses the power supply circuitry.

Figure 1.1 shows the PW1710 mounted in a stand-alone PW1719 cabinet to work with a PW1729 Generator. Figure 1.2 shows the PW1710 housed in the right-hand compartment of a PW1730 generator.

The PW1710 has its own front panel mounted alphanumeric keyboard and display plus extra command keys and system status indicators. Refer to figure 1.3.

35-key alphanumeric keyboard for input of measurement parameters and commands when no separate input/output terminal is used with the system.

20-digit alphanumeric display provides a variety of information including commands, parameters, error signals, and available memory space.

System status indicators show when the system is BUSY, in the ASSEMBLY mode, or in the REMOTE mode communicating with a terminal or computer.

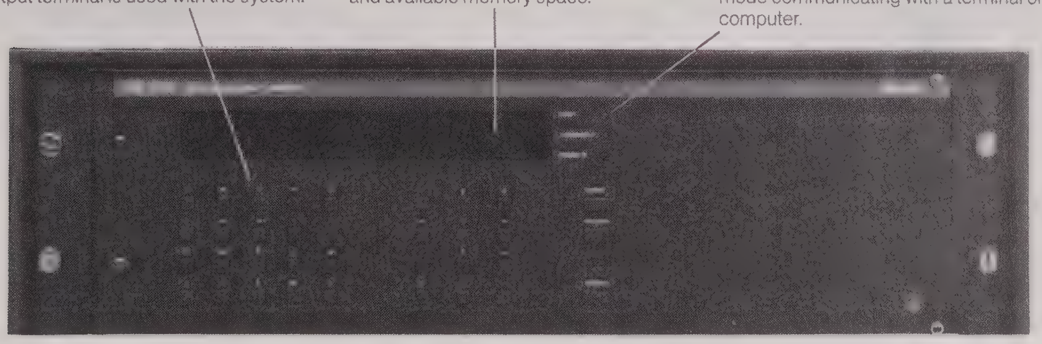

Figure 1.3 PW1710 Front Panel

A secondary control panel is provided for those functions which only need to be set occasionally. This panel is located behind the front panel of the control module. The functions which can be set at the secondary control panel include: a switch to select the attenuation for the detector pulses, a selector for matching the attenuation to the type of x-ray tube in use, and the controls for selection and adjustment of the HV for the detectors. Figure 1.4 shows this panel.

Once the system has been set up manually for a specific wavelength, change-over to a tube with a different anode only requires that the selector be set to the corresponding element name (CU, CO, FE, CR, or MO); the attenuation is then automatically adjusted.

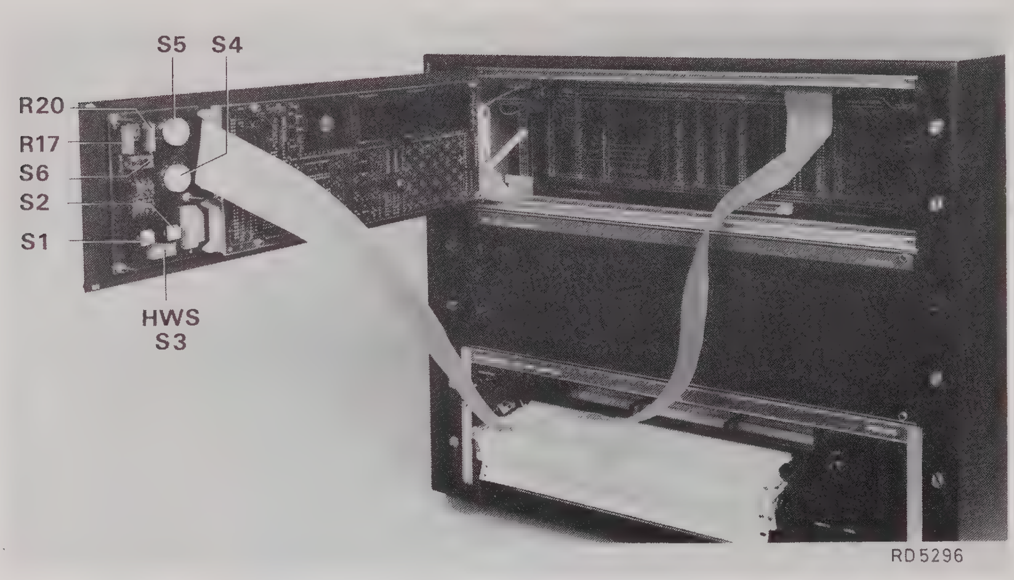

Figure 1.4 PW1710 Secondary Control Panel

In addition there are controls for the setting of the HV supply for the detectors, and pushbuttons for switching off the pulse-shift correction and for resetting the system (the RESET switch can be pressed by pushing a pencil or a small screwdriver through a small hole in the front panel, this means that the panel does not have to be opened every time you want to reset). Finally a block of slide switches is provided for defining the system´s hardware configuration. Refer to figure 1.4 (S3).

The Control Module is supplied with some printed circuit boards as standard, and others which are available as options. Table 1.1 shows the standard printed circuit boards, and table 1.2 the optional boards listed under their PW option number.

Table 1.1 Standard Printed Circuit Boards for the PW1710/00

Board name	Board Number	Board Position
Amplifier Analyser	5322 694 14331	X1
Detector Cable	5322 694 14481	X2
Window Control	5322 694 14332	X3
Ratemeter	5322 694 14333	X4
4 Digit Binary Counter	5322 694 14514	X5
Display Keyboard Control	5322 694 14471	X6
Recorder Control	5322 694 14477	X7
System Control	5322 694 14473	X10
Goniometer Control	5322 694 14472	X13
Goniometer Cable	5322 694 14483	X14
Stepping Motor Supply Driver	5322 694 14532	X15
Multiple Output Power Supply	5322 694 14479	X16
H.V. 2000 Supply	5322 694 14511	X18

Table 2. Optional Printed Circuit Boards for the PW1710/00

Option Number	Board Name	Board Number	Board Position
PW1712	Dual Serial Interface	5322 694 14475	X8
PW1713	Changer/Spinner/Shutter Control	5322 694 14476	X11
	Sample Changer Cable	5322 694 14482	X12
	Shutter/Spinner Driver	5322 694 14478	X17
PW1714	Shutter/Spinner Driver	5322 694 14478	X17
PW1717	Interface for PW1170	5322 694 14479	X12
	Located in PW1749 Options Rack		
PW1747	Goniometer Control	5322 694 14472	X13
	Stepping Motor Supply Driver	5322 694 14532	X14
	Goniometer Cable	5322 694 14483	X15
PW1748	Amplifier Analyser	5322 694 14331	X1
	Detector Cable	5322 694 14481	X2
	Window Control	5322 694 14332	X3
	Ratemeter	5322 694 14333	X4
	4 Digit Binary Counter	5322 694 14514	X5
	H.V. 2000 Supply	5322 694 14511	X18
	Secondary Control Panel	5322 694 14503	

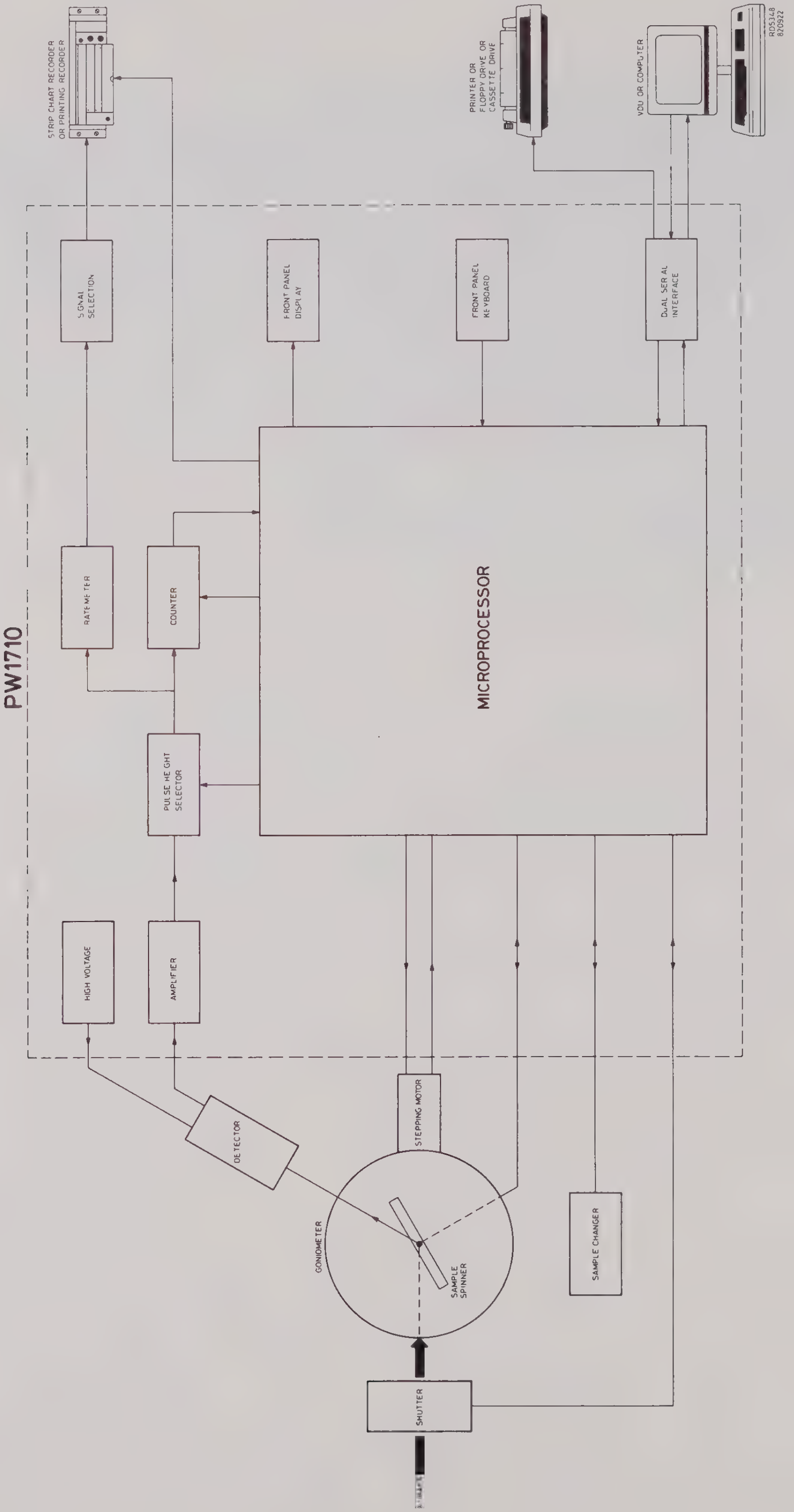
STRIP CHART RECORDER OR PRINTING RECORDER
PRINTER OR FLOPPY DRIVE OR CASSETTE DRIVE
VDU OR COMPUTER
RD5348 820922
PW1710
SIGNAL SELECTION
FRONT PANEL DISPLAY
FRONT PANEL KEYBOARD
DUAL SERIAL INTERFACE
RATEMETER
COUNTER
MICROPROCESSOR
PULSE HEIGHT SELECTOR
HIGH VOLTAGE
AMPLIFIER
DETECTOR
STEPPING MOTOR
GONIOMETER
SAMPLE SPINNER
SAMPLE CHANGER
SHUTTER

Figure 1.5 PW1710 in a Typical Diffractometry Set-up

1.1.3 ELECTRICAL DESCRIPTION

Figure 1.5 shows a block diagram of the PW1710 in a typical diffractometry set-up. It can be seen from this diagram that all the functions of the PW1710 are performed under the control of the microprocessor. This in turn is controlled by commands which are either stored in non-volatile memory, or keyed in from the front panel or control peripheral.

1.1.3.1 Control of Diffractometer

Control of the Diffractometer is achieved in three ways:

1. By controlling the goniometer (stepping motor), this is done by the Goniometer Control board and the Stepping Motor Supply Driver board.

2. By controlling the tube shield shutter using the optional PW1713 when the PW1775 is present.

3. By controlling the sample changer and/or spinner. The PW1710 can work with two sample changers and a spinner, either seperately or together. The interface between the changer and/or spinner and the system controller is dependant on which system you have.

   The Interface that is required, is as follows:

Sample changer PW1170	You must have PW1717 fitted, and the Interface board provides all the necessary control and drive signals for the sample changer.
Sample spinner PW1774	You must have PW1714 fitted, the control and drive signals for the spinner are provided by the Shutter/Spinner Drive board.
Sample changer/spinner PW1775, which comprises Sample changer PW1775, Sample spinner PW1774, and Radiation shield PW1771.	You must have PW1713 fitted, and the control and drive signals for the changer, spinner, and shutter are provided by the Changer/Spinner/Shutter Control board and the Shutter/Spinner Drive board.

1.1.3.2 Measurement and Processing of X-ray Intensities

Measurement and processing of x-ray intensities is achieved under the control of the microprocessor by the Amplifier Analyser, Window Control, 4 Digit Binary Counter, Ratemeter, Recorder control and HV 2000 boards.

1.1.3.3 Control of Peripherals

Peripherals such as VDUs, printers or computers are controlled by the optional Dual Serial Interface board which provides for two simultaneously controlled peripheral channels; the second channel is an input/output channel for either a hard copy device or a cassette recorder enabling the dumping and reading of user defined program. A terminal or VDU connected to the input/output channel can be selected as the control device for the PW1710 if so required.

1.1.3.4 Execution of Commands and User-Made Programs

As previously mentioned, commands may be given via the PW1710 front panel or a peripheral device. User-made programs can be assembled in the PW1710 memory which has aproximately 3500 bytes available for this purpose. Up to 255 different programs may be assembled. These programs are executed after the appropriate command is given from either the PW1710 front panel or a peripheral device.

1.1.4 USE OF THE MANUAL

This manual is intended for service engineers, and contains a technical description of the unit and its various options, it is intended to assist the service engineer install the PW1710 and its options, and to fault-find and repair the unit up to component level.

Readers should have read the PW1710/00 Users Manual (Ordering code: 9499.300.20311).

Throughout the manual such terms as right, left, front, rear, upper and lower are used to identify parts of the unit, or to describe operations or procedures. These terms relate to the position of an observer who is facing the front of the diffractometer unless a specific statement is made to the contrary in the relevant part of the text.

The manual contains certain items which require special attention. These items are given as either WARNING, CAUTION or NOTE. When these headings are used they have the following meaning:

WARNING: Denotes information which, if disregarded, may result in danger to the health or safety of the service engineer, the operator, or of any other person in the vicinity.

CAUTION: Denotes information which, if disregarded, may result in damage to equipment, excessive wear, or unsatisfactory equipment performance.

NOTE: Denotes information of particular importance for the understanding or adjustment of the diffractometer.

1.1.5 PARTS OF THE MANUAL

The manual comprises seven Chapters and two Appendices as follows:

CHAPTER 1	INTRODUCTION, contains an introduction to the PW1710, an introduction to the manual, and a technical specification.
CHAPTER 2	INSTALLATION, contains installation instructions for the PW1710 and all possible options.
CHAPTER 3	SYSTEM DESCRIPTION, comprises a description of the PW1710 including hardware/software, the XRA-bus, a memory map and how they all work together.
CHAPTER 4	HARDWARE DESCRIPTION, consists of an Introduction with general information and a list of mnemonics and signal names, and a sub-section for each of the cards in the PW1710. Each sub-section will have a description of the function performed by that particular card and a description of the card.
CHAPTER 5	SOFTWARE DESCRIPTION, provides a list of the commands available, together with a description of their effect and how they perform that task. It also shows the "Initialization" procedure and the Test facilities.
CHAPTER 6	FAULT FINDING, provides fault finding charts and information.
CHAPTER 7	SPARE PARTS LIST, comprises a list of spare parts for each card, and the Power Unit.
APPENDIX A	WIRING INFORMATION, comprises the overall wiring diagram and information about the wiring between the PW1710/00 and the Options Rack PW1749.
APPENDIX B	V24/CURRENT LOOP PRINCIPLES, consists of a description of the interface methods used in both V24 and Current Loop.

1.2 TECHNICAL SPECIFICATION

1.2.1 FUNCTIONS

1.2.1.1 Standard in PW1710:

Analog channel control:
Detector PW1964/70 or PW1711/10 can be used.

Goniometer control:
Goniometer equiped with stepping motor and shaft encoder.

Strip chart recorder control:
Recorders PM8203A and PM8210/31 can be used.

Display and keyboard control.

System control and non-volatile storage of measuring parameters and data.

Power supply for standard PW1710 plus options.

Calculations in simple APD.

1.2.1.2 Options to be Fitted into the PW1710

PW1712 Dual Serial Interface.

PW1713 Interface for PW1775 and PW1774 Changer/Spinner.

PW1714 Interface for PW1774 Spinner.

PW1717 Interface for PW1170 Changer.

1.2.1.3 Options to be Installed in the PW1749 Options Rack

PW1747 Additional stepping motor interface.

PW1748 Second detector interface.

1.2.2 RELATED PRODUCTS

Detectors:	PW1711/10 PW1964/70	Sealed gas filled detector Scintillation Detector
Sample changers:	PW1775/00 PW1774/00 PW1170	21/42 positions sample changer spinner Sample spinner 35 positions sample changer
Terminals:	P817/001 PC1409/01 PW1340/00	Visual display unit Mosaic printer Communications cable
Goniometer:	PW1050/81 PW1396/17 PW1397/55 PW1392/10	Vertical goniometer + stepper motor Stepping motor + cable Independent θ drive assembly Retrofit cable for PW1396/10
Recorders:	PM8203A PM8210/31	One line strip chart recorder One line printing strip chart recorder
Off-line storage:	PM4202/01	Digital Cassette Recorder
Housings:	PW1719/00 PW1749/00	19" triple height cabinet 19" options rack
Spares:	PW1718/00	S-module (spare parts kit)

1.2.3 SPECIFICATIONS

1.2.3.1 Detector Circuit:

- Maximum count rate	500 000 c/s.
- Dead time correction accuracy at 500 000 c/s.	< 1 %
- Dynamic range of amplification selector	40
- Automatic correctable pulse shift	Up to 50 %
- Upper and Lower level	0 to 99 %
- Rate meter range	100 to 500000 c/s
- Rate meter time constant	fixed 0.1 to 5 sec. matched to scan speed matched to counting range
- Intensity measuring interval	0 to 3276 sec.
- H.V. supply for - sealed detector	1500 to 2000 V
- scintillation detector	800 to 1200 V
- Detector pulse attenuation	1 to 8
- Selector switch to match attenuation to x-ray tube used	Cr, Fe, Co, Cu and Mo anode.
- Maximum accumulated counts	4×10^9 counts

1.2.3.2 Goniometer Circuit:

- Angle control in both directions with or without Shaft Encoder.	
- Range together with goniometer PW1050	
θ/2θ coupled to 1:2 ratio	0 to 160 °2θ
(optional) 2θ independent	0 to 360 ° θ
θ independent	0 to 160 °2θ
- Setting speed with anti-backlash provision	typical 2 °/s
- Continuous scan speed	0.001 to 1.27 °/s
- Step size range	0.005 to 160 °

1.2.3.3 Front Panel Control:

- Full use of instruction set
- Commands entered via alpha-numeric keyboard
- Initial settings on separate panel behind front cover

1.2.3.4 Parameter Control:

- Microprocessor controlled	
- User's memory area (Backed-up against power failure by rechargable batteries).	3500 bytes
Back-up time interval:	> 1000 hrs.
- Number of programs	max. 255
Program length	max. 255 bytes
- Number of registers	max. 255
Register length	4 bytes
Register capacity (neg. and pos.)	10^{-40} to 10^{+41}
- Calculation functions	ADD, SUBTRACT, MULTIPLY DIVIDE and SQUAREROOT

1.2.3.5 Output:

- Diffractogram to a strip chart recorder or printing strip chart recorder, the ratio between paper speed and goniometer scan speed: 1 to 50 mm/°2θ
- Digital output to Printing recorder PM8210
- All results can be displayed on the 20 digit display

1.2.4 ELECTRICAL REQUIREMENTS

- Supply voltage	220 Vac -12% +10%, 47 to 63 Hz., beta < 0.05
- Power requirements	< 200 VA all options included.

1.2.5 MECHANICAL PROPERTIES

- 19" Electronics unit	135 mm high	350 mm deep	4 kg. weight
- 19" Power unit	135 mm high	120 mm deep	9 kg. weight
- Mains cable	1.8 m long		

1.2.6 ENVIRONMENTAL CONDITIONS

- Operation	Temp. +5 to +55 °C	Rel. hum. 20 to 80 %
- Storage	Temp. -40 to +70 °C	Rel. hum. < 80 %

1.2.7 SAFETY PROFILE

- IEC 348
- CSA-C22.2 nr 151.

1.2.8 OPTIONS

PW1712 - Printed circuit board and 2 null-modems to allow communication with a terminal, computer, modem, cassette drive and/or hard copy device.

- Simultaneous second channel
- Off-line data storage/retrieval to/from digital cassette
- Switch selectable:

RS232C / V-24 or optically isolated 20 mA current loop

Full Duplex

Baud rates	50 to 9600 baud
Number of stop bits	1 or 2
Number of bits per character	7 or 8
Parity check	Odd / Even / None
Handshake type	Hardware or Software protocol
Echo	Yes or No

PW1713 - Set of printed circuit boards to control and supply all functions of the PW1775 and PW1774 21/42 position Sample Changer Spinner. (Load/unload - magazine drive - sample indication - lift - spinner - shutter).

PW1714 - Printed circuit board and cable to control and supply the PW1774 Sample Spinner.

PW1717 - Printed circuit board and cable to control and supply the PW1170 35 position Sample Changer. (Load/unload - cassette drive - sample indication).

PW1747 - Set of printed circuit boards to control and supply an independant second Stepping Motor (Slew - Scan - Calibrate).

PW1749 - Set of printed circuit boards to control and supply a complete second detector channel (Amplification - Discrimination - Digitizing - Counting).

1.2.9 LIST OF TYPE-NUMBERS

PW1710/00	Control module for diffractometry
PW1050/80	Vertical goniometer with stepping motor
PW1050/81	Vertical goniometer with stepping motor
PW1170	35-position sample changer to be used with PW1710/00
PW1178/00	Kit to convert PW1170/00/01/02 into PW1170
PW1340/00	Terminal cable
PW1386/55	Automatic divergence slit.
PW1392/10	Retro-fit cable for PW1396/10 and PW1050/80 up to Serial No. DY4006
PW1396/10	Stepping motor with cable
PW1396/17	Stepping motor with cable
PW1397/55	Indepedent theta drive assembly
PW1711/10	Sealed gas-filled detector
PW1712/00	Dual serial interface with 2 null-modems
PW1713/00	Control interface for changer/spinner PW1775
PW1714/00	Control interface for spinner PW1774
PW1717/00	Control interface for changer PW1170
PW1718/00	Spare-part kit for PW1710
PW1719/00	19" Triple height cabinet
PW1747/00	Additional stepping motor control
PW1748/00	Additional detector interface
PW1749/00	19" Options rack for PW1710 options (PW1747,PW 1748)
PW1774	Sample Spinner
PW1775	Sample Changer
P817/001	Visual display unit
PC1409/01	Mosaic printer (KSR 43)
PM8203A	One line strip-chart recorder
PM8210/31	One line printing recorder

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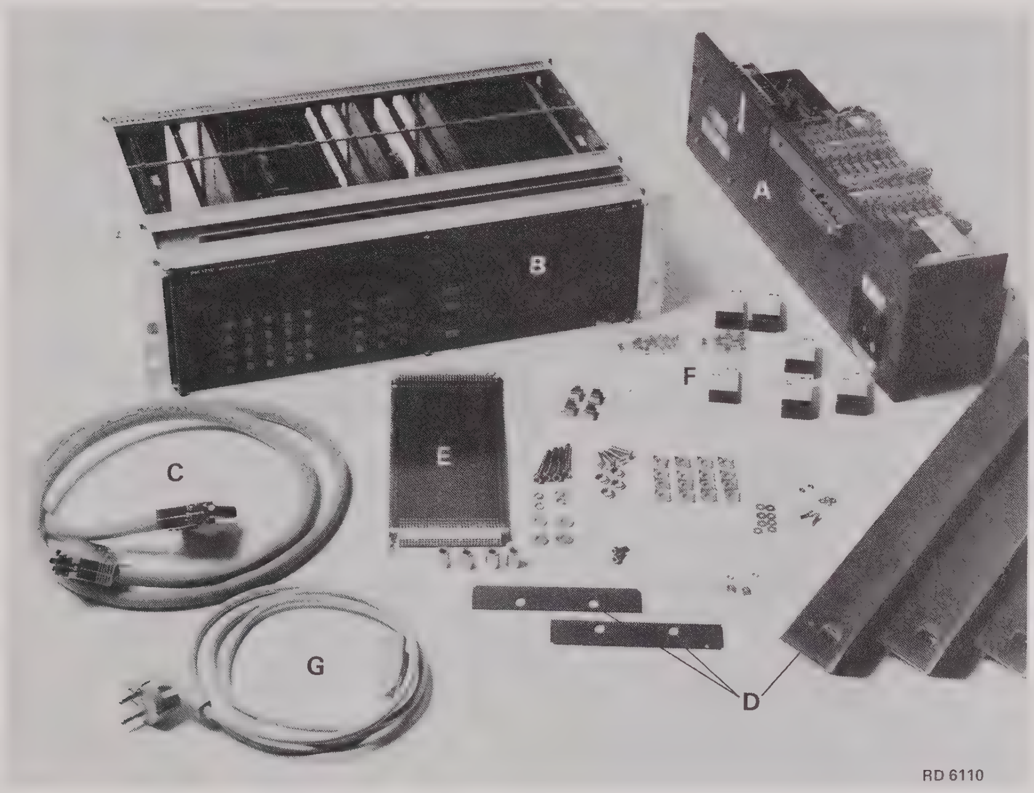
Figure 2.23 Wiring between the PW1710/00 and the PW1749/00 . . 2-63

INSTALLATION OF THE SYSTEM SHOULD ONLY BE CARRIED OUT BY A
****
PHILIPS SERVICE ENGINEER, OR BY OTHERWISE AUTHORIZED PERSONNEL.
****

2.1 GENERAL



A: Power Module: width 19", height 135mm, depth 120mm, weight 9 kg. approx.

B: Control Module: width 19", height 135mm, depth 350mm, weight 4 kg. approx.

C: Supply Cable between Power Module and Control Module.

D: Mounting material for mounting PW1710 into PW1719 Cabinet.

E: Extension board.

F: Set of spare fuses.

G: Mains cord.

Figure 2.1 PW1710 Component Parts

2.1.1 INTRODUCTION

These installation instructions cover three basic areas :

1. Installation of the PW1710 delivered with various options as a complete new system. Described in sections 2.3 and 2.4.

2. Installation of the PW1710 delivered as an individual item to be retro-fitted to an existing system. Described in section 2.6.

3. Installation of various options which may have to be installed in an existing PW1710 system. Described in section 2.5.

Packing details of the PW1710 and the various options concerned with it, are provided in section 2.2.

If the PW1710 is delivered as a new system, it will be installed in either a stand-alone cabinet PW1719 to work with various generators (described in section 2.3), or be installed in the PW1730 generator rack (described in section 2.4).

Each installation guide is given as a sequence of steps, each step referring you to either another section in this manual, or to another installation manual, for more detailed instructions on how to complete that particular step.

Paragraph 2.1.2 provides an overview of system installation which you can use as a step-by-step guide when you are installing the PW1710.

NOTE: *It is important that you read the complete installation section for your system before you start to install it.*

2.1.2 OVERVIEW OF SYSTEM INSTALLATION

The table 2.1 provides an overview of the system installation in the sequence in which it should be performed. The brackets around an action, for example: (INSTALL), indicate that the equipment being referred to is optional, and you therefore only need to perform that step if your sytem includes that option.

Table 2.1 Overview of System Installation

STEP	ACTION	EQUIPMENT	PW No.	Documentation Ref.	O.K.
1A	INSTALL or	Generator	PW1730	9499 305 04211	
1A	INSTALL	Generator	PW1729	9499 305 00811	
1B	INSTALL	Tube shield	PW1316/xx	Installation Manual	
1C	INSTALL	X-ray tube	PW22xx/xx	Installation Manual	
1D	CHECK	kVs, mAs, Shutter	--------	-------	
2A	INSTALL	PW1710	PW1710	This Manual	
2A	(INSTALL)	Options Rack	PW1749	This Manual	
2A	(INSTALL)	Dual Serial Interface	PW1712	This Manual	
2A	(INSTALL)	Terminal(s)	--	This Manual	
2B	CHECK	Communication	--	This Manual	
3A	INSTALL	Goniometer	PW1050	9499 300 20111	
3A	(INSTALL)	Spinner	PW1774	9499 305 06211	
3A	(INSTALL)	Second Detector supports		This Manual	
3B	CHECK	Motor Drive		This Manual	
3C	MECH. ALIGN	Goniometer	PW1050	9499 300 20111	
4A	INSTALL	Recorder or	PM8203A or	9499 430 06911	
4A	INSTALL	Recorder	PM8210/31	9499 430 06701 plus	
4B	CHECK	Recorder	"	9499 430 05601	

continued

Table 2.1 (continued) Overview of System Installation

STEP	ACTION	EQUIPMENT	PW No.	Documentation Ref.	O.K.
5	ALIGN	Goniometer plus knife edges (θ/ 2θ coupled 1:2)	PW1050	9499 300 20111	
6A	INSTALL	Monochromator	PW1752/00	9499 303 00611	
6B	ALIGN	Monochromator	PW1752/00	9499 303 00611	
7A	(INSTALL)	Spinner I/F	PW1714	This Manual	
7B	(CHECK)	Spinner I/F	PW1714	This Manual	
8A	(INSTALL)	2nd Stepping Motor I/F	PW1747	This Manual	
8A	(INSTALL)	Adapter kit	PW1397/55	9499 300 22611	
8A	(INSTALL)	Stepping Motor	PW1396/17	This Manual	
9	(ALIGN)	θ drive			
10A	(INSTALL)	Sample Changer and I/F.	PW1775 PW1713	This Manual " "	
	or	or	or		
10A	(INSTALL)	Sample Changer and I/F.	PW1170 PW1717	This Manual " "	
10B	(CHECK)	Sample Changer and I/F.	As fitted " "	This Manual " "	
11A	(INSTALL)	2nd Detector and I/F.	PW1711/10 PW1748	This Manual " "	
11A	(CHECK)	2nd Detector and I/F.	PW1711/10 PW1748	This Manual " "	
12	CLOSE	All doors and panels			
13	COMPLETE	Acceptance test			

2.2 PACKING DETAILS: STANDARD PW1710 AND OPTIONS

2.2.1 PW1710

The PW1710 is shipped in one carton box with dimensions :

64 - 49 - 41 cm

The contents of the box are shown in figure 2.1.

EXERCISE NORMAL CAUTION DURING UNPACKING. NO SPECIAL ACTIONS ARE REQUIRED.

2.2.2 OPTIONS

The following options are each shipped in one carton box:

EXERCISE NORMAL CAUTION DURING UNPACKING. NO SPECIAL ACTIONS ARE REQUIRED.

PW1711/10
PW1712/00
PW1713/00
PW1714/00
PW1717/00
PW1718/00
PW1719/00
PW1747/00
PW1748/00
PW1749/00

To start the INSTALLATION go to Section 2.3.

2.3 INSTALLING THE PW1710 IN STAND-ALONE CABINET PW1719/00

2.3.1 INSTALLATION GUIDE

STEP 1. Install the generator. This generator will probably be a PW1729. The installation procedure for the generator is provided in the manual which comes with the generator. The ordering code of this manual is: 9499 303 00811.

STEP 2. Mechanically pre-align the goniometer PW1050/81. Refer to the Installation manual which comes with the goniometer. The ordering code for this manual is: 9499 300 20111. Install the spinner PW1774 or the sample changer PW1170 or the changer/spinner PW1775. To install these accessories refer to Section 2.5.

STEP 3. Install the PW1719/00 cabinet.

STEP 4. Install the PW1710 POWER MODULE in the PW1719/00 cabinet.

STEP 5. Install the recorder, if present.

STEP 6. Install the OPTIONS RACK PW1749/00, if present.

STEP 7. Install the PW1710 CONTROL MODULE.

STEP 8. Connect all cables.

STEP 9. Continue with Section 2.8 : FIRST TIME SWITCHING-ON and ADJUSTMENTS.

2.3.2 DETAILED "STEP" INSTRUCTIONS

STEP 1. INSTALLATION OF THE GENERATOR

1. Refer to the installation documentation that was sent with the generator.

STEP 2. INSTALLION OF THE GONIOMETER

1. Refer to the goniometer Installation Manual.

STEP 3. INSTALLATION OF THE PW1719/00 CABINET

1. Refer to the packing list to check the contents of the box in which the PW1719/00 has been shipped. The four bolts have been delivered to fix the PW1710 POWER MODULE. The cabinet is shipped with two blank panels. If a recorder and/or an OPTIONS rack is present, these panels are not used.

2. Unpack the box and position the cabinet on a table.

NOTE: *When the PW1710 is to be mounted into the PW1719 cabinet it must be fixed to the cabinet frame by means of the delivered screws, earth plates, o-rings and distance pieces as shown in figure 2.5.*

STEP 4. INSTALLATION OF PW1710 POWER MODULE

1. Refer figure 2.1 to check the contents of the box in which the PW1710 has been shipped.
2. Unpack the box. (If a PW1712 dual serial interface is to be installed, refer to Section 2.5).
3. Mount the POWER MODULE by means of the four bolts delivered with the PW1719/00. Refer to figures 2.2 and 2.3. In figure 2.3, the RECORDER, OPTIONS RACK and CONTROL MODULE have already been installed. Ensure that the mains cable at the rear panel is not connected to the mains.
4. Mount the two support brackets as shown in figure 2.2 (A). If there is no OPTIONS rack present, these brackets should be in the HIGHER position (B).

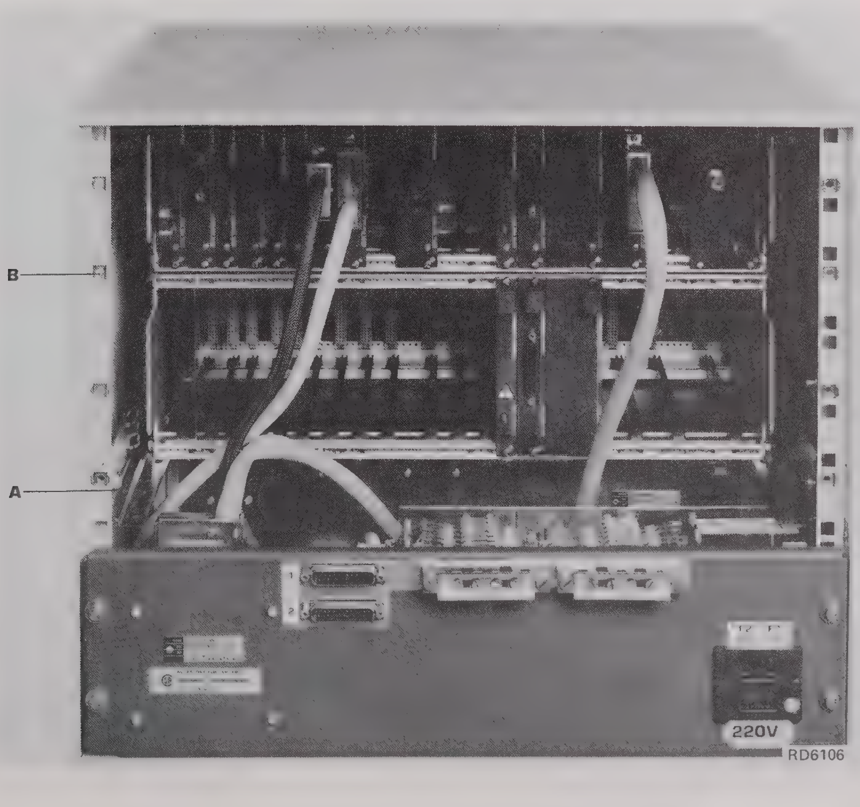


Figure 2.2 Position of Supporting Brackets

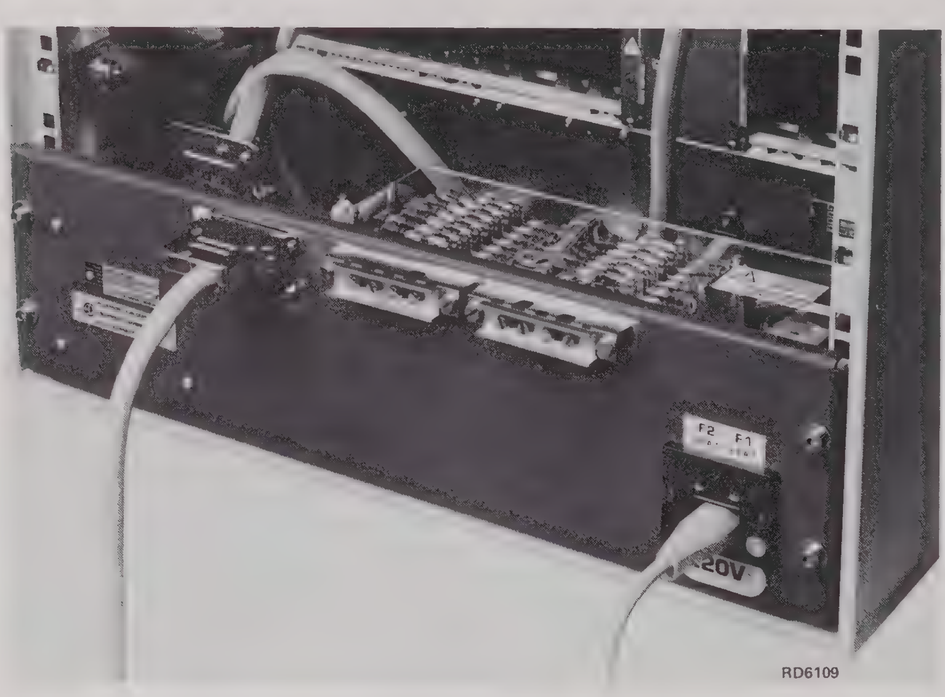

F2
F1
20V
RD6109

Figure 2.3 PW1710 Power Module

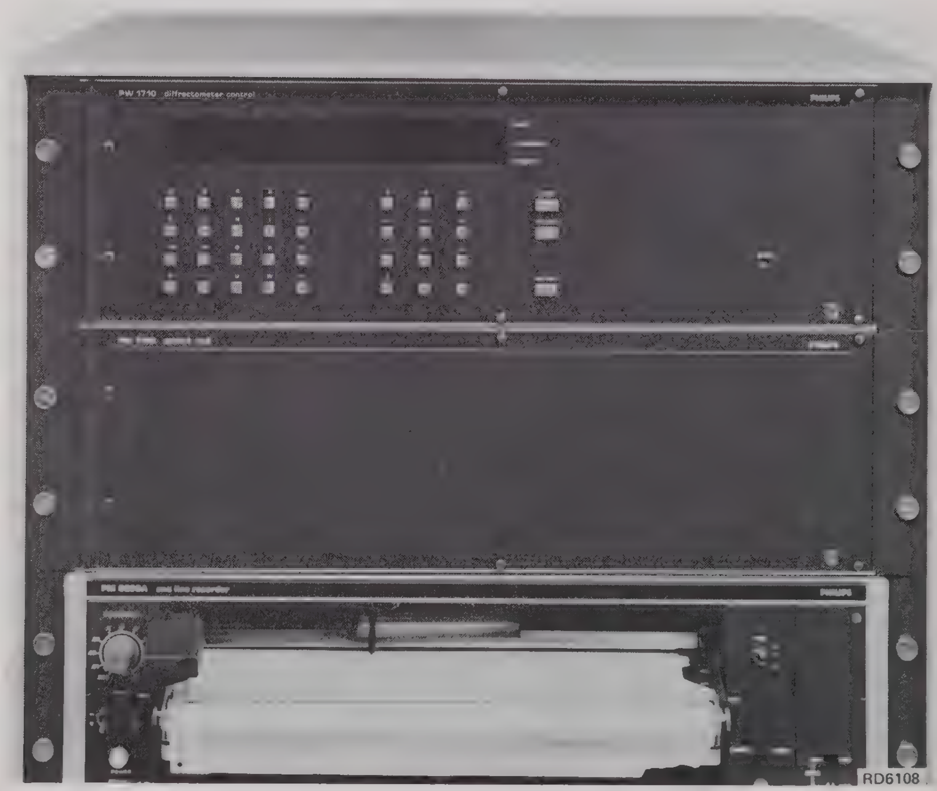
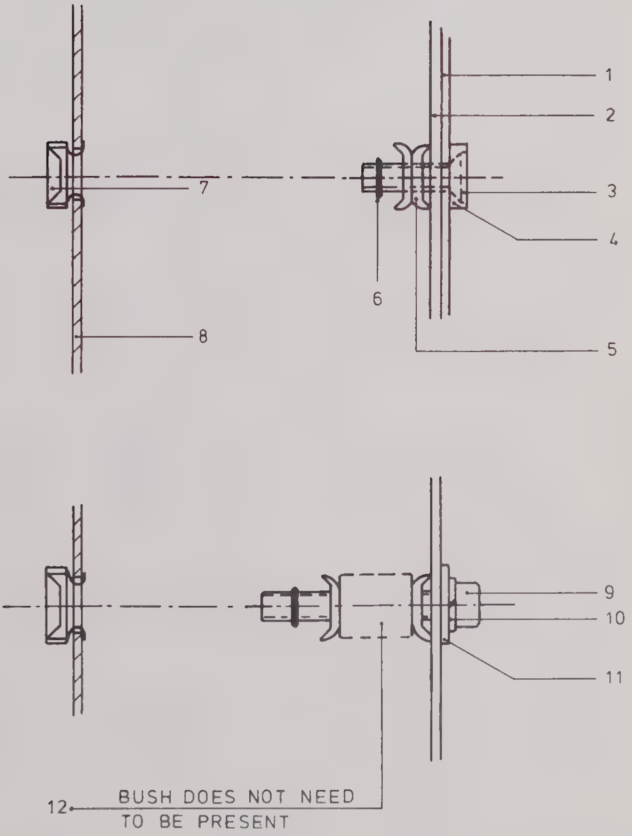

PW 1710 diffractometer control
RD6108

Figure 2.4 PW1710 Together With PW1749

1 COVER STRIP 3U
2 ELECTRONIC RACK ASSY
3 COUNTER SUNK SCREW ST ST M5 × 20
4 COUNTER SUNK WASHER CR NI ST 5
5 EARTH PLATE
6 O-RING
7 NUT GRIP ST ZN M5
8 CABINET ASSY
9 SCREW HEX SOCK ST ZN M5
10 CURVED SPR WASH ST ZN 5.1
11 WASHER ST ZN 5.3 × 15
12 BUSH
13 EARTH RING


1
2
3
4
5
6
7
8
9
10
11
12
BUSH DOES NOT NEED TO BE PRESENT

RD6081
850607

Figure 2.5 PW1710 Method of Mounting

STEP 5. INSTALLATION OF THE RECORDER PM8203A OR PM8210/31

NOTE: The jumpers indicated with "10" on the RECORDER CONTROL card have to be opened if a PM8203A is used. If a PM8210/31 is used, these jumpers should be closed. The RECORDER CONTROL card has been factory set for PM8210/31.

PM8203A

1. Ensure that the jumpers marked "10" on the RECORDER CONTROL are open. Refer to figure 2.22 for the position of the board in the PW1710 CONTROL MODULE. Refer to figure 2.6 for the board lay-out.
2. Slide the recorder into the PW1719/00 cabinet.
3. Select on the front of the recorder the following settings:

   "REMOTE" and CHART SPEED "10"
4. Set switch HWS 5 (Secondary Control Panel) to "1".
5. Set the ON/OFF switch to ON.
6. Set the ZERO/REC switch to REC.

PM8210/31

1. Ensure that the jumpers marked "10" on the RECORDER CONTROL are closed. Refer to figure 2.21 for the position of the board in the PW1710 CONTROL MODULE. Refer to figure 2.6 for the board lay-out.
2. Install the recorder according to the information in the operators/service manual for PM8210/31, which is delivered with the recorder. The ordering code of the manual is: 9499 430 05601. Also read the supplementary information in manual 9499 430 06701, which is also delivered with the recorder.

   The following settings are factory set inside the recorder:

   SERIAL INTERFACE: V24, 9600 baud, 7 bits/character, NO parity, full duplex.

   CPU INTERFACE CARD: MESSAGE is selected, for SKIP MESSAGE "PM8210/31 READY" (and approximately 8 cm of paper); connect the center two jumpers of the four present.
3. Slide the recorder into the PW1719/00 cabinet from the front.
4. Set PENLIFT to " REMOTE " on front of recorder.
5. Set switch HWS 5 (Secondary Control Panel) to "0".
6. Connect the Recorder cable, clamp the piece of bared shielding to the frame of the recorder using the cable clamp on the rear, and using an extra cable clamp secure the cable to avoid mechanical damage.

STEPS 6 and 7. OPTIONS RACK AND PW1710 CONTROL MODULE

1. Refer to the packing list to check the contents of the box in which the PW1749/00 has been shipped.

2. Position the PW1710 CONTROL MODULE on top of the OPTIONS RACK. Mount the connecting material. Refer to figure 2.4 (A). Slide the two modules into the cabinet.

3. Ensure that the jumper (A) on the system controller card has been closed, as otherwise the message BATTERY ERROR will be generated each time that the PW1710 is switched off and then on. Refer to figure 2.7.

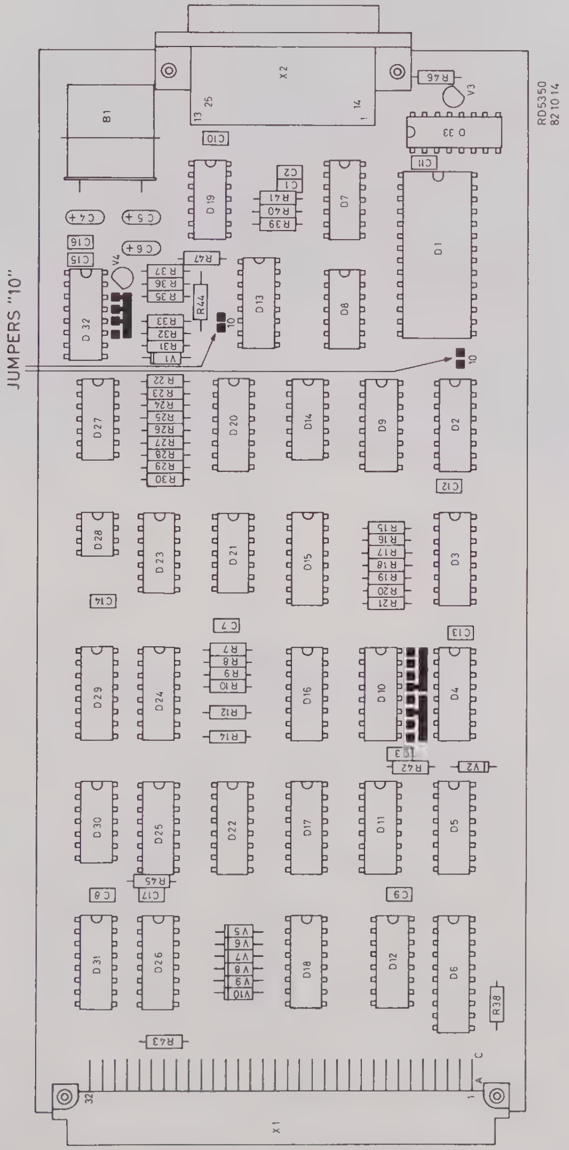

JUMPERS "10"
10
10
RD5350
821014
X2
X1
B1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
R38
R42
R43
R44
R45
R46
R47
13
25
14
1
32
1
A
C

Figure 2.6 Recorder Control Card

STEP 8. CONNECTION OF CABLES

1. Connect all cables according to the diagram shown on figure 2.21. Refer also to figure 2.23 for the interconnection between the motherboard of the PW1710 CONTROL MODULE and the motherboard of the OPTIONS RACK.

   Press the bared part of each cable into the appropriate slot on the slotted bar mounted at the rear of the Power Unit, and secure them with the clamping piece.

   If an OPTIONS RACK PW1749/00 is to be installed, an extra slotted bar is delivered with the OPTIONS RACK, this slotted bar must be mounted onto the rear of the power unit.

2. To connect the supply cable to the generator:

   In the PW1729 remove the left-hand side-panel of the generator. The PW1710 POWER MODULE supply cable should be connected to either the mains socket on the rear of the PW1729 or to the same power line as the PW1710.

STEP 9. CONTINUE WITH SECTION 2.8 FOR THE FIRST TIME SWITCHING ON PROCEDURE

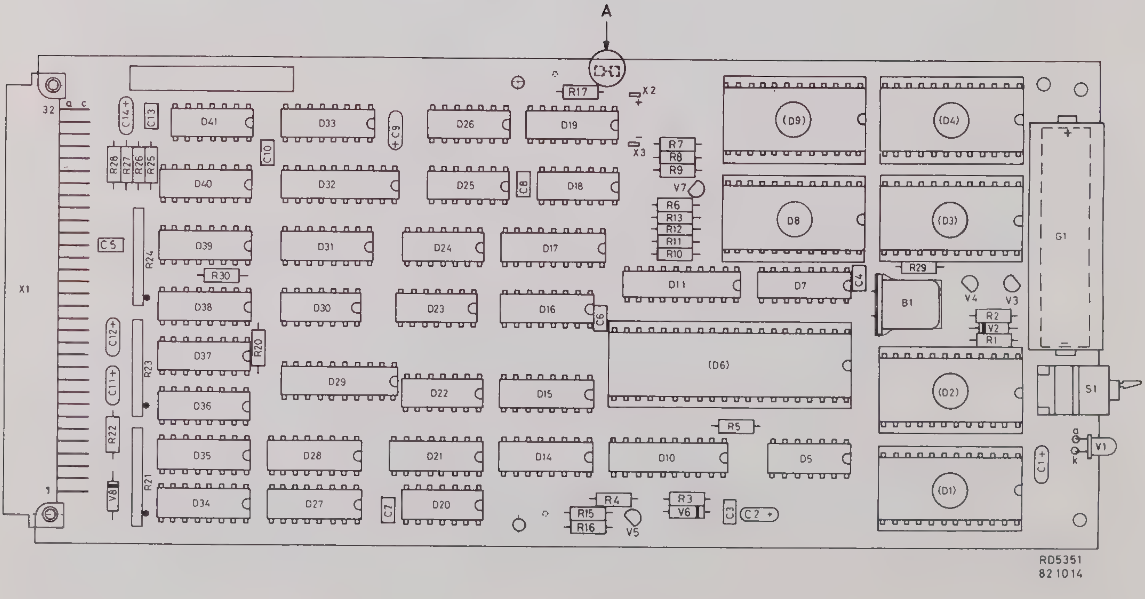

A
X1
32
a c
1
X2
X3
D41
D40
D39
D38
D37
D36
D35
D34
D33
D32
D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D15
D14
D11
D10
D7
D5
(D6)
(D9)
D8
(D4)
(D3)
(D2)
(D1)
G1
B1
S1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R15
R16
R17
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
V1
V2
V3
V4
V5
V6
V7
V8
a
k
RD5351
821014

Figure 2.7 System Control Card

2.4 INSTALLING THE PW1710 IN THE PW1730 GENERATOR

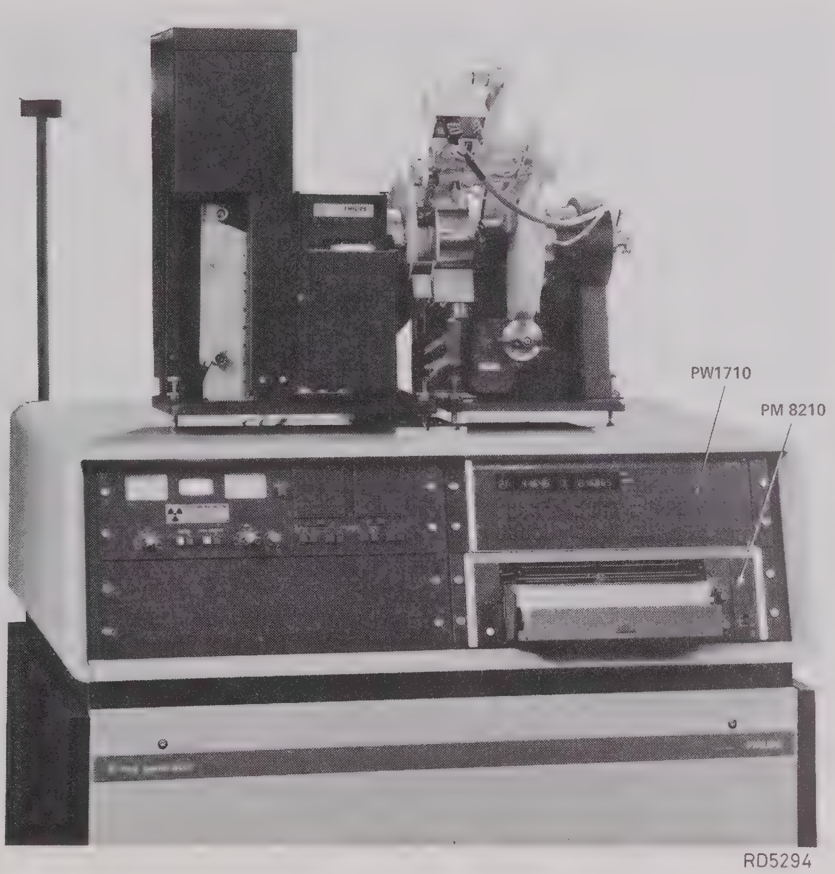


Figure 2.8 The PW1710 Mounted in the PW1730 Generator

2.4.1 INSTALLATION GUIDE

STEP 1. Install the PW1730 generator. The installation procedure for the generator is provided in the manual which comes with the generator. The ordering code of this manual is: 9499 305 02711.

STEP 2. If the generator is a PW1730/00 (or a PW1730/10 up to DY1416), mount the brackets to support the PW1710 CONTROL and POWER modules.

STEP 3. Install the PW1712 Dual Serial Interface (if present).

STEP 4. Install the POWER MODULE.

STEP 5. If present, install the recorder.

STEP 6. If present, install the OPTIONS rack.

STEP 7. Install the PW1710 CONTROL MODULE.

STEP 8. Install the Goniometer.

STEP 9. Connect all cables.

STEP 10. Continue with Section 2.8.

2.4.2 DETAILED "STEP" INSTRUCTIONS

NOTE: When the PW1710 is to be mounted into the top compartment of the PW1730 generator it must be fixed to the generator frame by means of the delivered screws, earth plates, o-rings and distance pieces as shown in figure 2.5.

STEP 1. INSTALLATION OF THE GENERATOR

1. Refer to the installation documentation that was sent with the generator.

   When the installation is complete, disconnect the generator from the mains so that you can continue with the rest of the installation steps.

STEP 2. MECHANICALY UPDATE THE PW1730 GENERATOR (/00 version):

Refer to figure 2.9 to see the position of the brackets required to support the PW1710 modules in the PW1730/00 generator. Mount the brackets as follows:

1. Remove the blank panels at the front upper and right-hand section of the generator cabinet.

2. Remove the rear and side panels of the generator cabinet. Mount the brackets as shown in figure 2.9.

STEP 3. INSTALL THE PW1712:

1. If the PW1712 Dual Serial Interface option should be installed, refer to Section 2.5 for instructions on how to install it.

STEP 4. INSTALL THE PW1710 POWER MODULE:

1. Slide the POWER MODULE into the generator from the rear. The module should be bolted to the frame by means of the four long bolts delivered with the PW1710.

2. Connect the supply cable to the 220V mains socket located at the rear.

   In PW1730/00/10 generator which do not have this connector, the POWER MODULE can be supplied from the 220 Volt mains socket at the rear of the generator.

POWER CONSUMPTION OF PW1710 IS LESS THAN 200 VA.

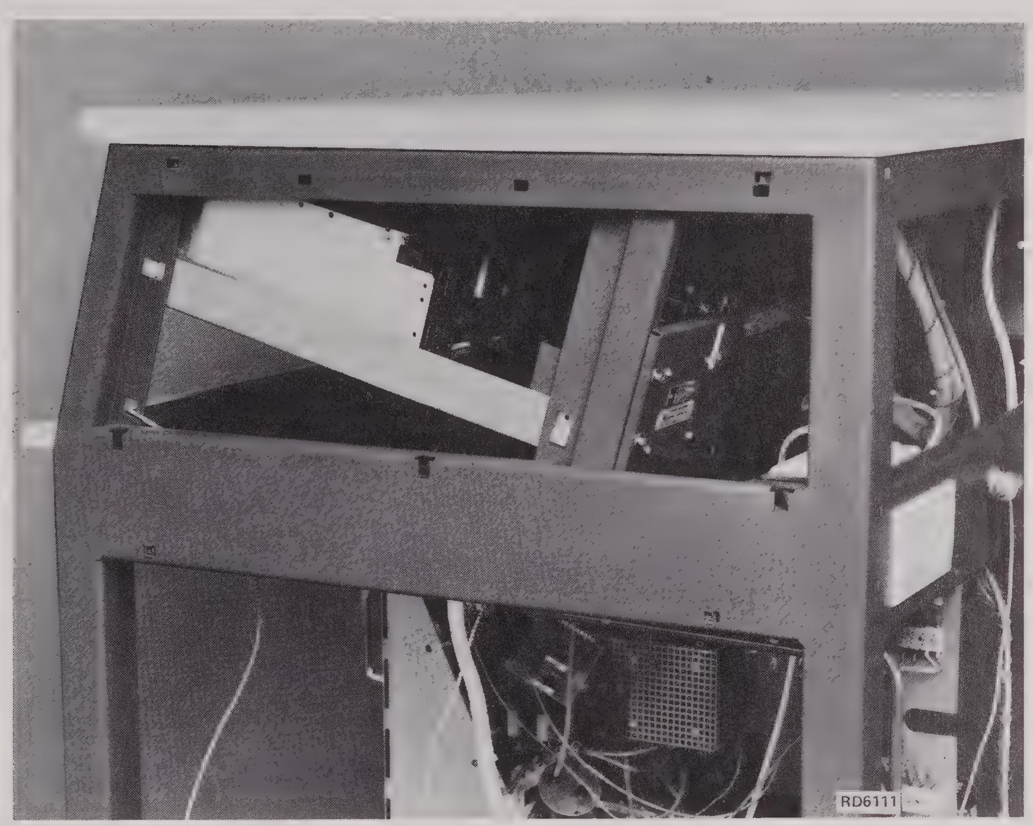


Figure 2.9 Location of Support Brackets in the PW1730 Generator

STEP 5. INSTALLATION OF THE RECORDER PM8203A or PM8210/31:

NOTE: *The jumpers indicated with "10" on the RECORDER CONTROL card have to be opened if a PM8203A is used. If a PM8210/31 is used, these jumpers should be closed. The RECORDER CONTROL card has been factory set for PM8210/31.*

PM8203A

1. Ensure that the jumpers marked "10" on the RECORDER CONTROL are open. Refer to figure 2.21 for the position of the board in the PW1710 CONTROL MODULE. Refer to figure 2.6 for the board lay-out.

2. If a PW1743/00 is present, the recorder should be positioned on top of the generator, the recorder is already equipped with rubber feet. If there is no PW1743 present, slide the recorder into the left-hand lower compartment at the front of the generator. The brackets at each side should then be removed.

3. On the front of the recorder, select the following settings:

   "REMOTE" and CHART SPEED "10"

4. Set switch HWS 5 (Secondary Control Panel) to "1".

5. Set the ON/OFF switch to ON.

6. Set the ZERO/REC switch to REC.

7. Connect the Recorder cable, clamp the piece of bared shielding to the frame of the recorder using the cable clamp on the rear, and using an extra cable clamp secure the cable to avoid mechanical damage.

PM8210/32

1. Ensure that the jumpers marked "10" on the RECORDER CONTROL are closed. Refer to figure 2.21 for the position of the board in the PW1710 CONTROL MODULE. Refer to figure 2.6 for the board lay-out.

2. If a PW1743/00 is present, the recorder should be positioned on top of the generator, the recorder is already equipped with rubber feet. If there is no PW1743 present, slide the recorder into the left-hand lower compartment at the front of the generator. The brackets at each side should then be removed.

3. Install the recorder according to the information in the operators/service manual for PM8210/32, which is delivered with the recorder. The ordering code of the manual is: 9499 430 05601. Also read the supplementary information in manual 9499 430 06701, which is also delivered with the recorder.

   The following settings are factory set inside the recorder:

   SERIAL INTERFACE: V24, 9600 baud, 7 bits/character, NO parity, full duplex.

   CPU INTERFACE CARD: MESSAGE is selected, for SKIP MESSAGE "PM8210/31 READY" (and approximately 8 cm of paper); connect the center two jumpers of the four present.

4. Set PENLIFT to " REMOTE " on front of recorder.

5. Set switch HWS 5 (Secondary Control Panel) to "0".

6. Connect the Recorder cable, clamp the piece of bared shielding to the frame of the recorder using the cable clamp on the rear, and using an extra cable clamp secure the cable to avoid mechanical damage.

STEPS 6 and 7. INSTALLATION OF OPTIONS RACK and INSTALLATION OF PW1710 CONTROL MODULE:

1. If any of the options PW1712, PW1713, PW1714 or PW1717 should be present, install them, to do so refer to section 2.5. Then install the PW1710 CONTROL MODULE.

2. Slide the CONTROL MODULE together with the OPTIONS RACK into the upper section of the generator compartment.

3. Connect the cables between the motherboards of the CONTROL MODULE and the OPTIONS RACK as shown in figure 2.23 at the rear of this Chapter. The motherboards are located behind the front panels of the modules.

STEP 8. INSTALL THE GONIOMETER:

1. Install the goniometer according to the instructions delivered with it.

STEP 9. CONNECTION OF CABLES:

1. Connect all cables as shown in figure 2.21.
2. Check all connections carefully.

STEP 10. PROCEED WITH Section 2.8.

2.5 INSTALLATION OF OPTIONS

Installation procedures for the following options have been provided:

OPTION	Described in PARA:
PW1749/00 Options Rack	2.5.1
PW1711/10 Detector PW1964/70 Detector	2.5.2
PW1712/00 Dual serial interface P817/001 VDU PC1409/01 KSR 43	2.5.3
PW1713/00 Control interface for PW1775	2.5.4
PW1714/00 Control interface for PW1774 spinner	2.5.5
PW1717/00 Control interface for PW1170	2.5.6
PW1719/00 Triple-height cabinet	2.5.7
PW1747/00 Additional stepping motor interface	2.5.8
PW1748/00 Additional detector interface	2.5.9

2.5.1 INSTALLATION OF OPTIONS RACK PW1749/00

If a second counting channel and/or a second (one-theta) stepper motor drive have to be installed, OPTIONS RACK PW1749/00 is required.

1. Refer to the packing list to check the contents of the box in which the PW1749/00 has been shipped.
2. Unpack the box.
3. Position the PW1710 CONTROL MODULE on top of the OPTIONS RACK. Mount the connecting material (refer to figure 2.4 [A]). Slide the two modules into the cabinet.

4. Mount the brackets in the PW1719/00 cabinet or PW1730 generator. Refer to figures 2.2 and 2.9.

5. Set the jumpers on the PW1710 and PW1749 motherboards according to the table on figure 2.23.

6. Connect the cables between the motherboard of PW1710 CONTROL MODULE and the motherboard of the OPTIONS RACK. Refer to figure 2.23.

7. Mount the delivered slotted bar next to the one on the Power Module.

2.5.2 INSTALLATION OF PW1711/10 OR PW1964/70 DETECTORS

1. First read the instructions given in the manual delivered with the detector.

2. Connect the supply/signal cable as shown in figure 2.21.

3. Proceed with section 2.8.

2.5.3 INSTALLATION OF DUAL SERIAL INTERFACE PW1712/00

1. Refer to the packing list to check the contents of the box in which the PW1749/00 has been shipped.

2. Unpack the box.

3. Remove the mains supply cable from its socket.

4. Mount the cable with connectors X100 and X101 onto the rear panel of the PW1710 POWER MODULE, ensure that the connector base plate is on the outside edge of the back panel. Refer to figure 2.3 (A). First mount connector X101 in position 2. Then mount connector X100 in position 1. Use the connecting material delivered. Fix the cable with the two tie-wraps to the extension of the fuse-plate.

5. Set the Interface switches according to the device that is to be connected.

   When you are installing the Dual Serial Interface, you have to select the correct parameters for the peripheral device(s) connected to your system. This is achieved by several slide switches located on the board. These switches allow you to select for interfaces 1 and 2, the current source, whether or not handshake mode is required, the parity, the number of bits per character and the baud rate.

2.5.3.1 Switch and Jumper Settings

There are three rows of slide switches, indicated by X, Y and Z. Each slide switch can be set to position A or B. Tables 2.2, 2.3 and 2.4 give an overview of what is actually selected if a switch is set in position A or B.

For the baudrate, four switches have to be set. These switches have been named N0, N1, N2 and N3 in the general baudrate table (2.4).

Legend:	
IF1 means Port 1	HS means handshake
IF2 means Port 2	DO means data only (software handshake or current loop)

C means current source in interface
CS means current source
NC means current source outside interface
CL means current loop 20 mA
TMIT means transmit
RCV means receive

Table 2.2 Switches S1 to S6

SWITCH NUMBER	SWITCH POSITION A	B	SWITCH ROW "X"
S1.1	C	NC	IF2 : CS TMIT
S1.2	C	NC	IF2 : CS TMIT
S2.1	C	NC	IF1 : CS TMIT
S2.2	C	NC	IF1 : CS TMIT
S3.1	C	NC	IF1 : CS RCV
S3.2	C	NC	IF1 : CS RCV
S4.1	C	NC	IF2 : CS RCV
S4.2	C	NC	IF2 : CS RCV
S5.1	DO	HS	IF2 : HANDSHAKE
S5.2	V24	CL	IF2 : MODE
S6.1	DO	HS	IF1 : HANDSHAKE
S6.2	V24	CL	IF1 : MODE

Table 2.3 Switches S1 to S6

SWITCH NUMBER	SWITCH POSITION A	B	SWITCH ROW "Y"	SWITCH NUMBER	SWITCH POSITION A	B	SWITCH ROW "Z"
S7.1	1	0	IF2 : FIXED "8" BIT	S11.1	1	0	IF2 : BAUDRATE N1
S7.2	YES	NO	IF2 : ECHOPLEX	S11.2	1	0	IF2 : BAUDRATE N0
				S12.1	1	0	IF2 : BAUDRATE N3
				S12.2	1	0	IF2 : BAUDRATE N2
				S13.1	1	0	IF1 : BAUDRATE N3
				S13.2	1	0	IF1 : BAUDRATE N1
S8.1	1	0	IF1 : FIXED "8" BIT	S14.1	1	0	IF1 : BAUDRATE N0
S8.2	1	0	IF1 : BAUDRATE N2	S14.2	YES	NO	IF1 : ECHO-PLEX
S9.1	2	1	IF1 : STOP BIT(S)	S15.1	2	1	IF2 : STOP BIT(S)
S9.2	YES	NO	IF1 : PARITY CHECK	S15.2	YES	NO	IF2 : PARITY CHECK
S10.1	EVEN	ODD	IF1 : PARITY TYPE	S16.1	8	7	IF2 : BITS/CHAR.
S10.2	8	7	IF1 : BITS/CHAR.	S16.2	EVEN	ODD	IF2 : PARITY TYPE

Table 2.4 Baudrate Settings

BAUDRATE	N3	N2	N1	N0
50	0	0	1	0
75	0	0	1	1
110	1	1	1	1
134,5	0	1	0	0
150	1	1	1	0
200	0	1	0	1
300	1	1	0	1
600	0	1	1	0
1200	1	0	1	1
1800	1	0	1	0
2400	0	1	1	1
3600	1	1	0	0
4800	1	0	0	1
9600	1	0	0	0
19200	0	0	0	0

Figure 2.10 shows an enlarged view of the slide switches with them set to provide the following interface parameters:

Interface 1: V24, 9600 BAUD, 7 bits/character, NO parity, echo YES, 1 stop bit.

Interface 2: V24, 300 BAUD, 8 bits/character, NO parity, echo YES, 1 stop bit, 8th bit set to 0.

THESE SETTINGS ARE THE CORRECT SETTINGS IF A P817/001 OR P816/001 IS TO BE CONNECTED TO THE I/O CHANNEL (POSITION 1) AND A PC1409/01 KSR TO THE SECOND OUTPUT CHANNEL (POSITION 2).

6. Insert the interface board into the PW1710 CONTROL MODULE. Refer to figure 2.22. Connect the cable between board and POWER MODULE.

7. Connect the VDU according to figure 2.21. Use the NULL-MODEM, which is delivered with the PW1712. The VDU should be set as follows:

   Baud rate: 9600, 8 bits/character, NO parity, 1 stop bit.

   Refer to the manual for P817/001/002 (ordering code: 5122 991 28702) Chapters 5 and 6 or for the P816/001/002 (ordering code: 5122 991 32950). The manual is delivered with the VDU.

8. Connect the PC1409/01 according to the diagram in figure 2.21. Use the NULL-MODEM which has been delivered with the PW1712. Settings on PC1409/01 should be as follows:

   30 cps, NO parity, FULL DUPLEX.

   Selection of these settings to be made with push buttons on keyboard panel. Refer to manual 391, Part 9 for the 43 TELEPRINTER, issued by TELETYPE. The manual is delivered with the PC1409.

9. If a different I/O device has to be connected, make sure that the selected parameters on the interface of PW1712, and the selected parameters in the I/O device correspond to each other. The information about V24 protocol as given in Section 2.5.3.1 will be sufficient.

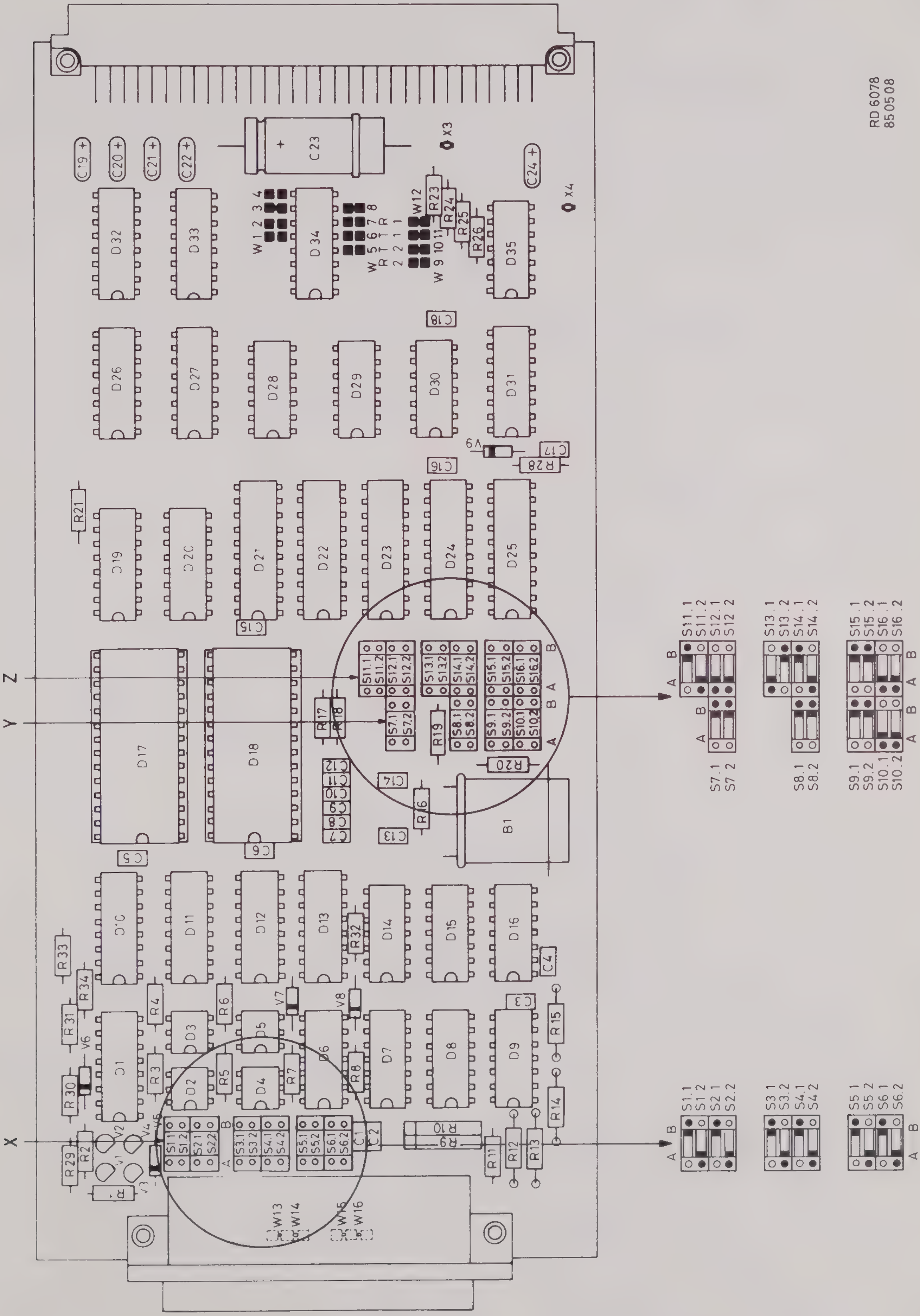
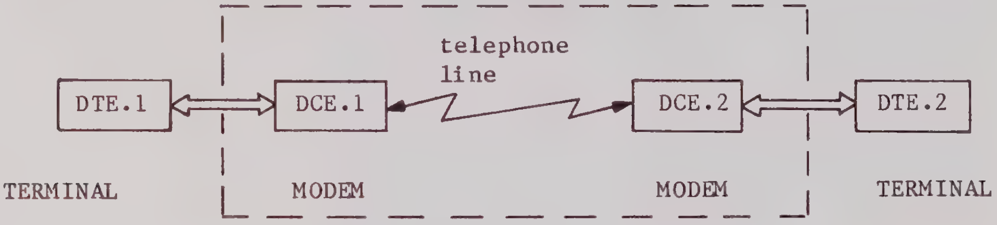

RD 6078
850508
X
Y
Z
A
B
S1.1
S1.2
S2.1
S2.2
S3.1
S3.2
S4.1
S4.2
S5.1
S5.2
S6.1
S6.2
S7.1
S7.2
S8.1
S8.2
S9.1
S9.2
S10.1
S10.2
S11.1
S11.2
S12.1
S12.2
S13.1
S13.2
S14.1
S14.2
S15.1
S15.2
S16.1
S16.2
W 1 2 3 4
W 5 6 7 8
W 9 10 11 W12
W13 W14 W15 W16
X3
X4
B1
C23
D17
D18

Figure 2.10 Serial Interface Card, Switches and Jumpers

2.5.3.2 Interface Protocol

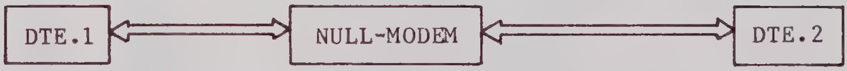
This section provides information about the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE) using the CCITT-V24 or the EIA-RS 232C protocol.

LONG DISTANCE CONNECTION
****

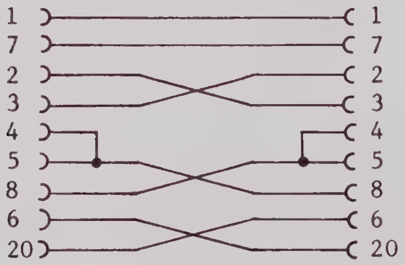

telephone line
DTE.1
DCE.1
DCE.2
DTE.2
TERMINAL
MODEM
MODEM
TERMINAL

SHORT DISTANCE CONNECTION (<15 M)
****

" NULL-MODEM " REPLACES DCE.1, TELEPHONE LINE AND DCE.2


DTE.1
NULL-MODEM
DTE.2

NULL-MODEM PIN-OUT


1
7
2
3
4
5
8
6
20
1
7
2
3
4
5
8
6
20

CONNECTORS .... DTE DCE

MALE FEMALE

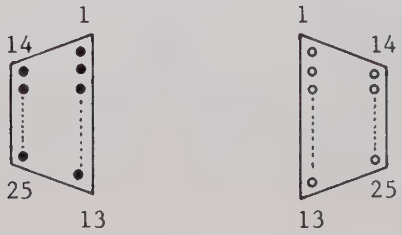
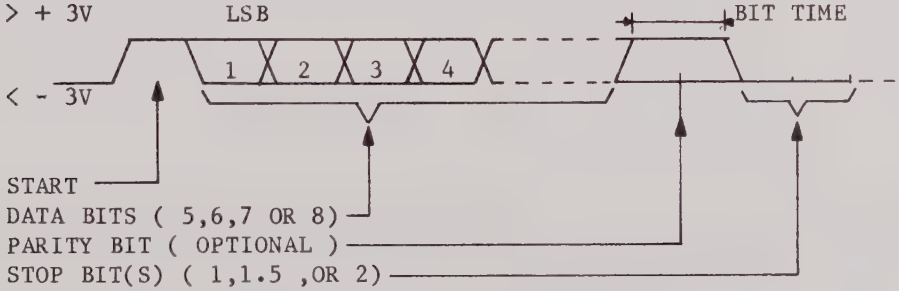

1
14
25
13
1
14
25
13

Table 2.5 Interface Between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE)

Pin No.	Signal No.	Mne-Monic	Name	Function	Level
1	101	P.GND	PROTECTIVE GROUND	CONNECTED TO FRAME	0V
7	102	S.GND	SIGNAL GROUND	CONNECTED TO 0V	0V
2	103	TXD	TRANSMITTED DATA (DTE ----> DCE)	OUTPUT FROM DTE	> +3V = START
3	104	RXD	RECEIVED DATA (DTE <---- DCE)	INPUT TO DTE	< -3 V = STOP
4	105	RTS	REQUEST TO SEND (DTE ----> DCE)	DTE WANTS TO SEND	|Vmax| <25
5	106	CTS	CLEAR TO SEND (READY TO SEND)	DCE READY TO TRANSMIT	> +3 V = ON
6	107	DSR *	DATA SET READY (DTE <---- DCE)	DCE IS READY TO OPERATE	< -3 V = OFF
8	109	DCD *	DATA CARRIER DETECTED (DTE <---- DCE)	CARRIER RECEIVED	
20	108.2	DTR *	DATA TERMINAL READY (DTE -----> DCE)	DTE READY TO OPERATE	

* HERE USED TO TEMPORARILY HALT THE DATA EXCHANGE

DATA FORMAT (ASYNCHRONOUS MODE)



THE FOLLOWING PARAMETERS HAVE TO BE SELECTED BY MUTUAL AGREEMENT BETWEEN DTE.1 AND DTE.2 :

1. BAUD-RATE
2. NUMBER OF BITS PER CHARACTER
3. NUMBER OF STOP BITS
4. PARITY CHECK YES/NO , EVEN/ODD
5. FIXED VALUE FOR BIT 8 (ASCII IS 7 BITS !!)
6. ECHO YES/NO

Table 2.6 Interface Between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE)

EXPRESSION	MEANING
FULL DUPLEX	Receiver and transmitter can operate simultaneously
HALF DUPLEX	Interface has to be switched from receive to transmit mode or visa versa
ECHO PLEX	Data from transmitter is NOT routed internally to the receiver
DIRECT OPERATION	Data from transmitter is routed internally to the receiver
PARITY CHECK	An extra bit, added by the transmitter and making the number of ones per character even or odd is tested by the receiver
PARITY ERROR	The parity bit is not according to the type of check
FRAMING ERROR	The parity bit is not according to format
BAUD RATE	Number of bits per second
ECHO	Data to receiver is echoed back by the transmitter

2.5.4 PW1713/00 CONTROL INTERFACE FOR PW1775

IT IS ASSUMED THAT THE PW1775 HAS BEEN PROPERLY INSTALLED. REFER TO THE INSTALLATION MANUAL SENT WITH THE PW1775.

1. Switch OFF the supply to the PW1710 POWER MODULE.
2. Refer to the packing list to check the contents of the box in which the PW1713/00 has been shipped. Unpack the box.
3. Check the jumpers settings on the Changer/Spinner/Shutter Control card are as given in table 2.8 (in section 2.7).
4. Insert the three boards as indicated in Figure 2.21.
5. Connect all cables as shown in figure 2.21.
6. Set HWS 0 (Front panel) to "0".
7. Proceed with the check-out procedure in Section 2.8.3.

2.5.5 INSTALLATION OF CONTROL INTERFACE PW1714/00 FOR SPINNER PW1774

IT IS ASSUMED THAT THE SPINNER PW1774 HAS BEEN PROPERLY INSTALLED. REFER TO THE INSTALLATION MANUAL, WHICH IS SHIPPED WITH THE SYSTEM.

NOTE: The supply voltage for the motors in PW1775 and PW1774 should be 24 V a.c. Refer to figures 4.67 and 4.68.

1. Refer to the packing list to check the contents of the box in which the PW1714/00 has been shipped. Unpack the box.
2. Insert the printed circuit board and connect the cable as shown in Figure 2.21.
3. Proceed with the check-out procedure in Section 2.8.3.

2.5.6 INSTALLATION OF CONTROL INTERFACE PW1717 FOR SAMPLE CHANGER PW1170

CHECK THAT THE SAMPLE CHANGER HAS BEEN PROPERLY INSTALLED.

NOTE: The supply voltage for the PW1170 should be 48 V a.c. The standard setting in the factory is 24 V a.c. Refer to figures 4.67 and 4.68.

If this voltage has to be set to 48 V a.c., proceed as follows:

1. REMOVE the mains cable from the 220 V socket on the PW1710 POWER MODULE.

2A. IN PW1710 SYSTEMS WITH SERIAL NUMBER UP TO DY 616:

- Remove the plastic cover above the fuse panel in the POWER MODULE (4 screws). Refer to figure 2.3 (B).
- Loosen the fuse panel.
- The orange wire connected to terminal 16 of the transformer below the fuse plate, means that 24 V a.c has been selected. To select 48 V a.c this wire should be connected to terminal 20 of this transformer.
- Change fuse F115 from 315 mA Slow Blow (for 24 V) to 1.6A Slow Blow (for 48 V).

2B. IN PW1710 SYSTEMS WITH SERIAL NUMBER DY 617 AND OVER:

- Remove the plastic cover above the fuse panel.
- Move the orange wire from fuse F115 to fuse F114. This latter fuse already has an orange wire at the other side.
- The 1.6 A (Slow Blow) fuse is already in postion F114.

Now complete the installation of the PW1717 as follows:

3. Refer to the packing list to check the contents of the box in which the PW1717/00 has been shipped. Unpack the box.

4. Insert the printed circuit board and connect the cable as shown in Figure 2.21.

5. Set HWS 0 (Front Panel) to "1".

6. Proceed with the check-out procedure in Section 2.8.3.

2.5.7 INSTALLATION OF CABINET PW1719/00

1. Refer to the packing list to check the contents of the box in which the PW1719/00 has been shipped. The four bolts have been delivered to fix the PW1710 POWER MODULE. The cabinet is shipped with two blank panels. If a recorder and/or an OPTIONS rack is present, these panels are not used.

2. Unpack the box and position the cabinet on a table.

2.5.8 INSTALLATION OF PW1747/00 INTERFACE FOR ADDITIONAL STEPPING MOTOR

NOTE: With this interface it is possible to control a second stepping motor (usually a one-theta drive). Keep in mind however that the control is not a completely indepedent one, so that it is not possible to control a second diffractometer set-up in the same way as with the standard PW1710 stepping motor control.

1. Refer to the packing list to check the contents of the box in which the PW1747/00 has been shipped. Unpack the box.

2. Install the PW1749/00 OPTIONS RACK:
   a. Refer to the packing list to check the contents of the box in which the PW1749/00 has been shipped.
   b. Unpack the box.
   c. Position the PW1710 CONTROL MODULE on top of the OPTIONS RACK. Mount the connecting material (refer to figure 2.4 [A]). Slide the two modules into the cabinet.
   d. Mount the brackets in the PW1719/00 cabinet or PW1730 generator. Refer to figures 2.2 and 2.9.
   e. Set the jumpers on the PW1710 and PW1749 motherboards according to the table on figure 2.23.
   f. Connect the cables between the motherboard of PW1710 CONTROL MODULE and the motherboard of the OPTIONS RACK. Refer to figure 2.23.
   g. Mount the delivered slotted bar next to the one on the POWER UNIT.

3. Check that the switches and jumpers on the Goniometer Control Card 5322 694 14472 are set correctly, as is shown in figure 2.11.

4. Insert the three printed circuit boards as shown in Figure 2.22.

5. Connect the cables to the second stepping motor in the same way as for the standard motor control. See figure 2.21.

6. Proceed with the check-out procedure in Section 2.8.3.

2.5.9 INSTALLATION OF PW1748 INTERFACE FOR ADDITIONAL DETECTOR

If a second detector is to be used (for example, in POT-FLUX applications) the PW1748 interface should be installed as follows:

1. Refer to the packing list to check the contents of the box in which the PW1748/00 has been shipped. Unpack the box.

2. Install the PW1749/00 OPTIONS RACK:
    a. Refer to the packing list to check the contents of the box in which the PW1749/00 has been shipped.
    b. Unpack the box.
    c. Position the PW1710 CONTROL MODULE on top of the OPTIONS RACK. Mount the connecting material (refer to figure 2.4 [A]). Slide the two modules into the cabinet.
    d. Mount the brackets in the PW1719/00 cabinet or PW1730 generator. Refer to figures 2.2 and 2.9.
    e. Set the jumpers on the PW1710 and PW1749 motherboards according to the table on figure 2.23.
    f. Connect the cables between the motherboard of PW1710 CONTROL MODULE and the motherboard of the OPTIONS RACK. Refer to figure 2.23.
    g. Mount the delivered slotted bar next to the one on the POWER UNIT.

3. Check that the switches, jumpers and links on the following three cards are as shown in the indicated figure:

    - Window control card .... Figure 2.12
    - Ratemeter card .... Figure 2.13
    - 4 Digit binary counter .... Figure 2.14

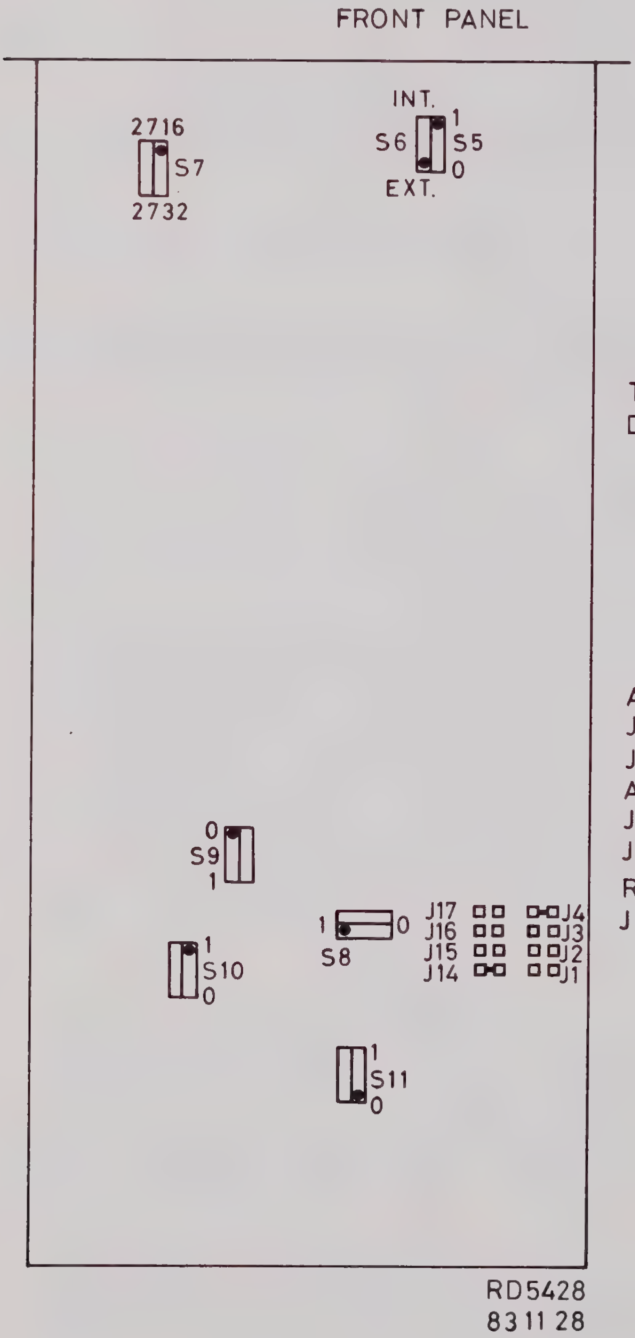
4. Insert all the printed circuit boards as indicated in Figure 2.22.

5. Connect the cables as shown in Figure 2.21.

6. Install the Secondary Control Panel. This panel should be mounted on the inside of the OPTIONS RACK cabinet front panel, on the right-hand side. See figure 2.23.

7. Adjust the two potentiometers for the H.V. supply for the detectors to mid-position (10 turns from one end).

8. Proceed with the check-out procedure in Section 2.8.3.


FRONT PANEL
INT.
1
S6
S5
0
EXT.
2716
S7
2732
0
S9
1
1
S10
0
1
0
S8
J17
J16
J15
J14
J4
J3
J2
J1
1
S11
0
RD5428
83 11 28

THE SWITCH SETTINGS IF
DONE AS SHOWN GIVE :

S5 1 = NO HIGH VOLT
S6 0 = EXT. CLOCK
S7 0 = PROM TYPE 2716
S8 1 = SHAFT ENCODER
S9 0 = NO AUT CALIBRATE
S10 1 = 1 REV = 2°
S10 0 = 1 REV = 1°

ADD. SETTING FOR θ DRIVE
JUMPER J4 SHOULD BE CLOSED
JUMPER J14 SHOULD BE CLOSED
ADD. SETTING FOR 2θ DRIVE
JUMPER J3 SHOULD BE CLOSED
JUMPER J14 SHOULD BE CLOSED
REST OF THE JUMPER
J1 - J14 ARE OPEN.

Figure 2.11 Goniometer Control Card Switches and Jumpers

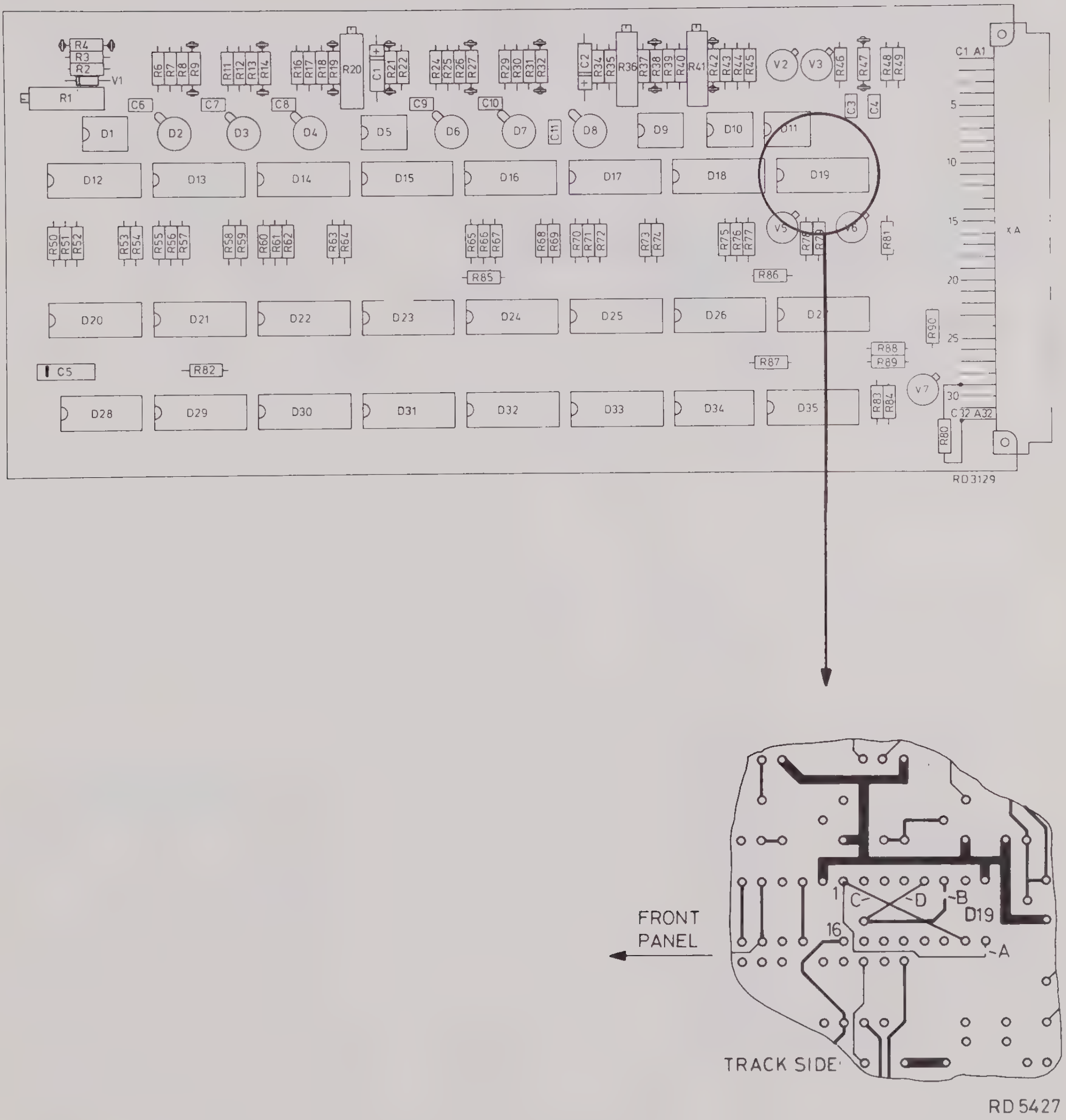
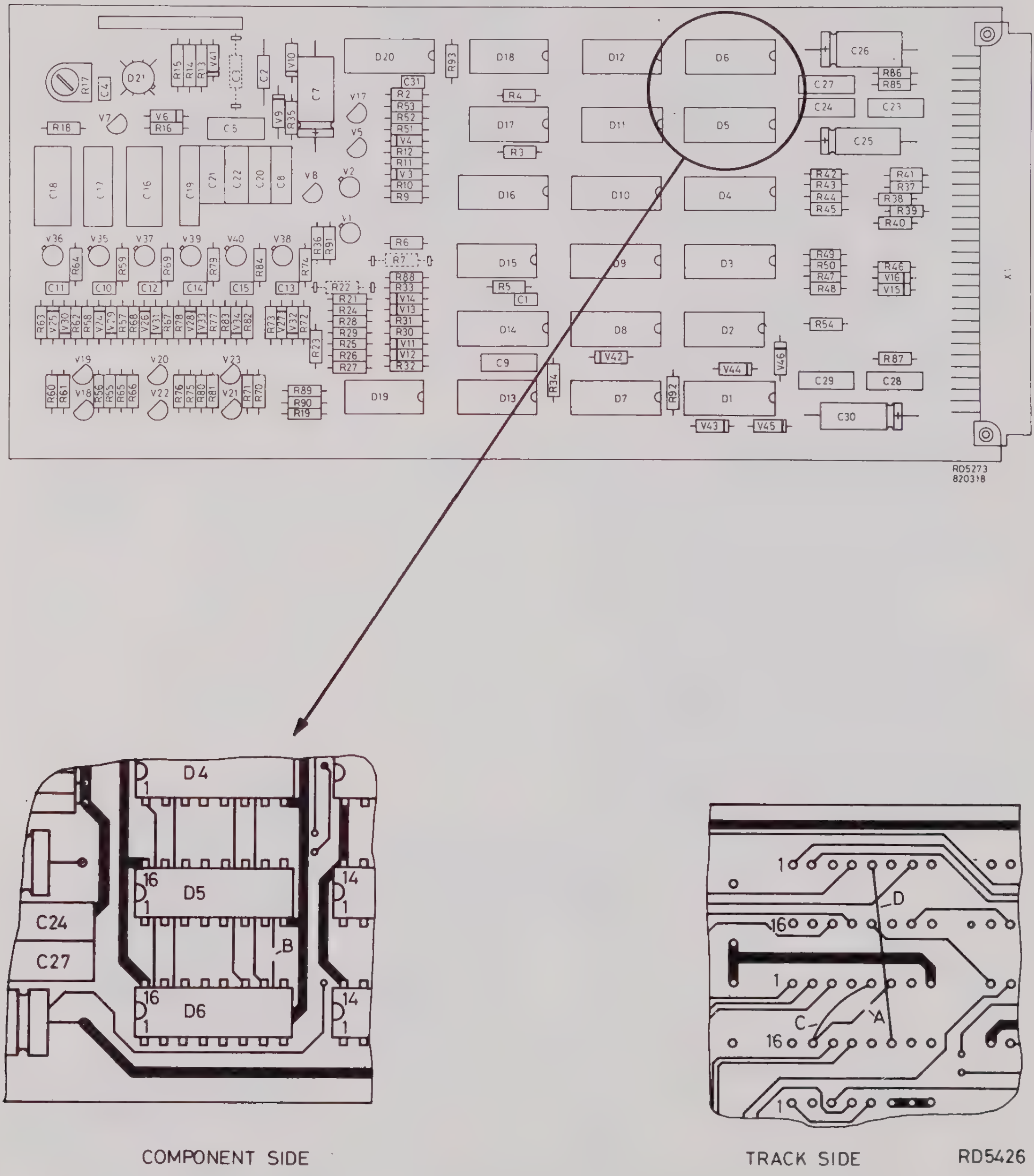

D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D28
D29
D30
D31
D32
D33
D34
D35
R1
R20
R36
R41
R85
R86
R87
R82
C5
V1
V2
V3
V5
V6
V7
C1 A1
C32 A32
5
10
15
20
25
30
XA
RD3129
FRONT PANEL
TRACK SIDE
1
16
C
D
B
A
D19
RD5427

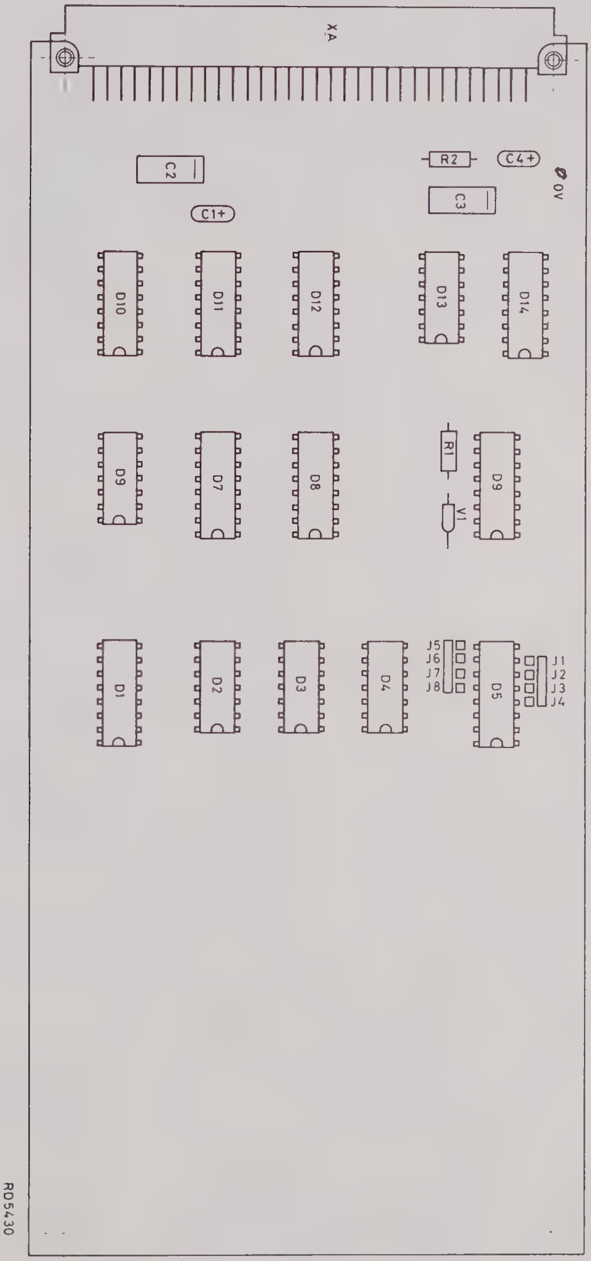
Figure 2.12 Window Control Card Link Settings


D20
D18
D12
D6
D17
D11
D5
D16
D10
D4
D15
D9
D3
D14
D8
D2
D19
D13
D7
D1
C26
C27
C24
C23
C25
C29
C28
C30
C7
C5
C9
X1
RD5273
820318
D4
D5
D6
C24
C27
16
1
14
B
1
16
D
C
A
RD5426

COMPONENT SIDE

TRACK SIDE

Figure 2.13 Ratemeter Card Link Settings


XA
C2
C1+
R2
C4+
C3
0V
D10
D11
D12
D13
D14
D9
D7
D8
R1
V1
D9
D1
D2
D3
D4
J5
J6
J7
J8
D5
J1
J2
J3
J4
RD5430

Open Jumpers
J2 and J7

Close Jumpers
J3 and J8

Figure 2.14 4 Digit Binary Counter Card Jumper Connections

2.5.10 INSTALLATION OF THE PM4202/01 CASSETTE RECORDER

If your does not have a Cassette Recorder PM4202/01 installed, and you wish to install one, do that as follows:

1. The recorder must be connected to the Dual Serial Interface in the PW1710/00 via a null modem and a PW1340 cable.
2. The switch settings on the rear of the cassette recorder must be as shown in figure 2.15.
3. The switches on the Dual Serial Interface board must be set as shown in figure 2.16. Serial interface 1 is set for a printer and serial interface 2 for the recorder, table 2.7 shows the meaning of the switch settings.
4. Jumpers W9, W10, W11 and W12 on thhe Dual Serial Interface board must all be "CLOSED".

Table 2.7 Dual Serial Interface Board Switch Setings

INTERFACE 1 (PRINTER)		INTERFACE 2 (PM4202)	
SWITCH	FUNCTION	SWITCH	FUNCTION
S6.1	Handshake	S5.1	Handshake
S6.2	V24	S5.2	V24
S8.1	Bit 8 = 0	S7.1	Bit 8 = 0
S14.2	Echo-plex	S7.2	Echo-plex
S9.1	2 Stop bits	S15.1	1 Stop bit
S9.2	No Parity	S15.2	No Parity
S10.1	Even parity	S16.1	Even Parity
S10.2	8 bits/char	S16.2	8 Bits/char
S8.2	300 Baud	S11.1	2400 Baud
S13.1	" "	S11.2	" "
S13.2	" "	S12.1	" "
S14.1	" "	S12.2	" "

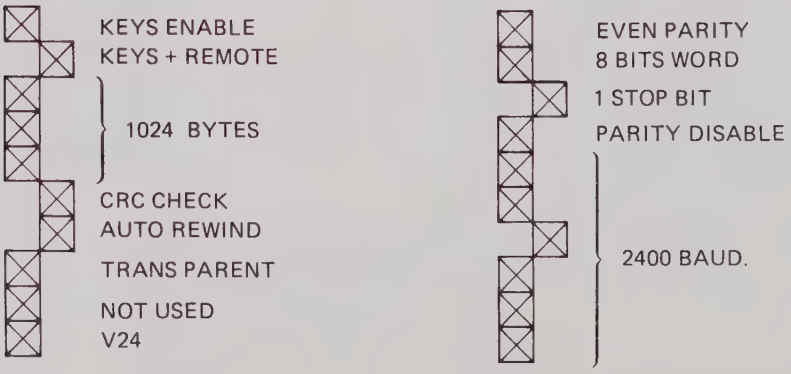

KEYS ENABLE
KEYS + REMOTE
1024 BYTES
CRC CHECK
AUTO REWIND
TRANS PARENT
NOT USED
V24
EVEN PARITY
8 BITS WORD
1 STOP BIT
PARITY DISABLE
2400 BAUD.

Figure 2.15 Cassette Switch Settings

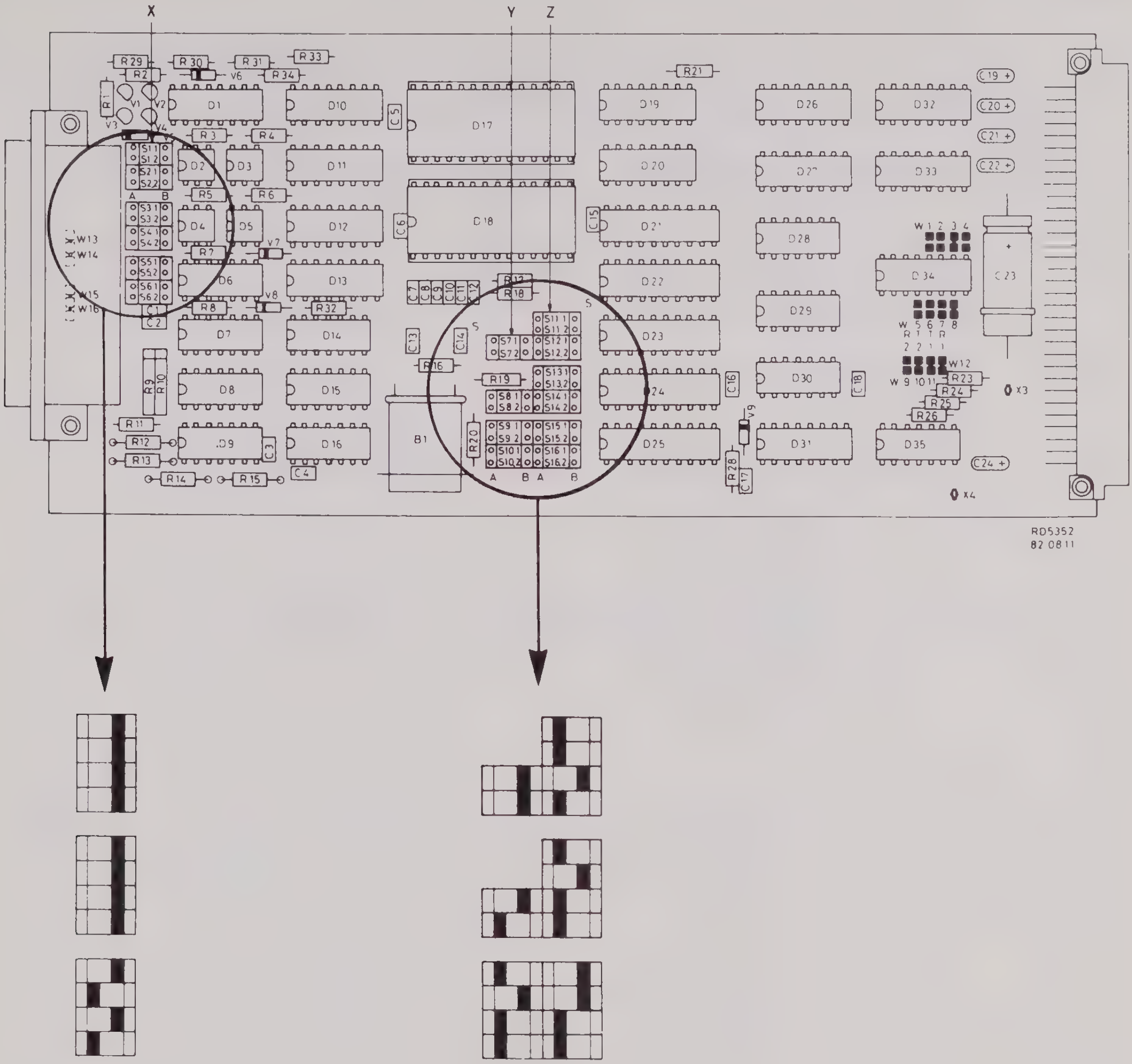


Figure 2.16 Serial Interface Card Switches and Jumpers (with PM4202)

2.6 RETROFIT

Upgrading of existing diffractometer systems with the PW1710 is possible. The specific actions required are summarized below:

2.6.1 GONIOMETERS PW1050/.... TO PW1050/81

1. The goniometer used with PW1710 should have a stepping motor. The standard goniometer type used is PW1050/81.

NOTE: *If a goniometer which has a synchronuous motor is present, update kit PW1397/50 and Stepping motor PW1396/17 is required to convert this goniometer into a PW1050/81. The update can be performed in the field.*

The PW1397/50 kit includes the instructions for the update. The PW1396/17 is identical to PW1396/10 with the exception that the PW1396/17 uses a 25-pole connector instead of a 15-pole connector.

2. If the PW1710 is to be connected to a PW1050/80/81 with serial numbers up to DY 4006, cable PW1392/10 is required. This cable is also required if a PW1050/70/71/76/77 is provided with a PW1396/10 stepping motor.

3. The stepping motor of goniometers PW1050/81 and retrofit versions may run too fast when driven with PW1710. To correct this, proceed as follows:

   a. Make the connection shown as a dotted line in figure 2.8 between the slider of MS1 and 1 of connector X1.

   b. Then check that jumper J5 on the Goniometer Control Card is set to "1".

2.6.2 UPDATE OF PW1050 WITH ONE-THETA DRIVE

For this update, PW1397/55 is required. This update can be performed in the field, the instructions for the update are included in the kit.

2.6.3 RETRO-FIT OF PW1170/00/01/02

The PW1170 is the standard sample changer to be used with the PW1710. If a PW1170/00/01/02 is present, it should updated. The update can be performed in the field. Update kit PW1178/00 is required. The update instructions are included in the kit.

2.6.4 GENERATORS PW1730

The PW1710 can be mounted without modification into PW1730/10. If the PW1710 is to be mounted into a PW1730/00, the generator should be mechanically adapted in order to accept the PW1710. Refer to paragraph 2.4 for the instructions on how to do this.

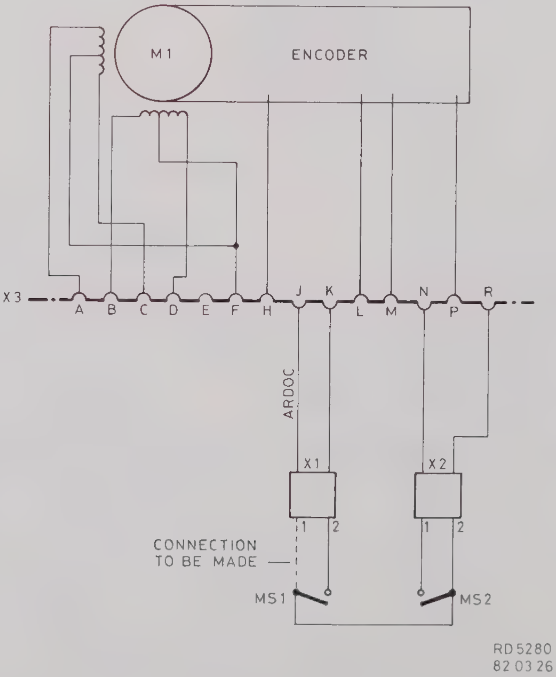


Figure 2.17 Goniometer PW1050/81 Adaption Cable Connection Diagram

2.7 SWITCH AND JUMPER SETTINGS

The following table provides a list of all the switches and jumpers and how they should be set after you have installed the PW1710. The settings given are for a standard PW1710, if your system has any of the options fitted, the settings for that option are given in the appropriate part of section 2.5.

Table 2.8 Standard settings

Switch or Jumper	Function	Setting	Comment
SYSTEM CONTROL CARD Component side			
S1	SID switch	0	
S2.1	Not used	-	
S2.2	Timer interrupt kill	ON	Up to DY700.
Track side			
J1 (B)	Battery OFF/ON	Closed	
J2 (T)	Timer interrupt kill	Closed	After DY701.
Memory extension -- Component side			
JS	SID ON	Closed	
JT	Trap ON	Closed	
S1.1	not used	0	
S1.2	not used	0	
S2.1	not used	0	
S2.2	not used	0	
S3.1	not used	0	
S3.2	not used	0	
S4.1	not used	0	
S4.2	not used	0	
S5.1	Sel 8k 4k ROM	4	
S5.2	Sel 8k 4k ROM	4	
S6.1	Sel 8k 4k ROM	4	
S6.2	Sel 8k 4k ROM	4	
DUAL SERIAL INTERFACE CARD Component side			
S1.1	IF2 Current source in interface/TMIT	B	
S1.2	IF2 Current source in interface/TMIT	A	
S2.1	IF1 Current source in interface/TMIT	B	
S2.2	IF1 Current source in interface/TMIT	A	
S3.1	IF1 Current source in interface/RCV	B	
S3.2	IF1 Current source in interface/RCV	A	
S4.1	IF2 Current source in interface/RCV	B	
S4.2	IF2 Current source in interface/RCV	A	
S5.1	IF2 Data only/HS	B	
S5.2	IF2 V24/CL	A	
S6.1	IF1 Data only/HS	B	
S6.2	IF1 V24/CL	A	
S7.1	IF2 Bit 8 1/0	B	
S7.2	IF2 Echo/No Echo	B	
S8.1	IF1 Bit 8 1/0	B	
S8.2	IF1 Baudrate	B	
S9.1	IF1 2/1 Stop bits	B	
S9.2	IF1 Parity Check YES/NO	B	
S10.1	IF1 Parity EVEN/ODD	A	
S10.2	IF1 8/7 Bits per character	B	

Table 2.8 Standard settings (continued)

Switch or Jumper	Function	Setting	Comment
DUAL SERIAL INTERFACE CARD	Component side (continued)		
S11.1	IF2 Baudrate	B	
S11.2	IF2 Baudrate	A	
S12.1	IF2 Baudrate	A	
S12.2	IF2 Baudrate	A	
S13.1	IF1 Baudrate	A	
S13.2	IF1 Baudrate	B	
S14.1	IF1 Baudrate	B	
S14.2	IF1 Echo/No Echo	A	
S15.1	IF2 2/1 Stop bits	B	
S15.2	IF2 Parity Check YES/NO	B	
S16.1	IF2 8/7 Bits per character	A	
S16.2	IF2 Parity EVEN/ODD	A	
J1	Address decoder	Open	
J2	Address decoder	Open	
J3	Address decoder	Closed	
J4	Address decoder	Open	
J5	Address decoder	Open	
J6	Address decoder	Open	
J7	Address decoder	Open	
J8	Address decoder	Closed	
J9	Interrupt RECV2	Closed	
J10	Interrupt TMIT2	Closed	
J11	Interrupt TMIT1	Closed	
J12	Interrupt RECV1	Closed	
J13	IF1 Signal Ground	Closed	
J14	IF1 Power Ground	Closed	
J15	IF2 Signal Ground	Closed	
J16	IF2 Power Ground	Closed	
SECONDARY CONTROL PANEL			
S1	CAL	-	Spring loaded
S2	RESET	-	Pushbuttons
S3.0	PW1775 or PW1170/10	0	HWS0
S3.1	2k or 4k RAM	1	HWS1
S3.2	Memory test YES or NO	0	HWS2
S3.3	Number of Detectors ONE or TWO	0	HWS3
S3.4	Spare	0	HWS4
S3.5	Recorder PM8210/31 or PM8203A	0	HWS5
S3.6	Theta drive Not present or Present	0	HWS6
S3.7	2 θ drive Not present or Present	1	HWS7
S4	ATT	2	Rotary switch
S5	TUBE att.	CU	Rotary switch
S6	SCINT/GAS Detector	Depending on System	

Table 2.8 Standard settings (continued)

Switch or Jumper	Function	Setting	Comment
GONIOMETER CONTROL CARD			
J1	Address decode	Open	
J2	Address decode	Open	
J3	Address decode	Closed	
J4	Address decode	Open	
J5	High Voltage YES/NO	0	
J6	External or Internal CLOCK	0	
J7	PROM type number 2716 or 2732	1	
J8	Encoder NO/YES	0	
J9	Automatic Calibrate YES/NO	0	
J10	Step size 0,005 or 0,01	0	
J11	Up Clockwise or Counter-Clockwise	1	
J14	Address decode	Closed	
J15	Address decode	Open	
J16	Address decode	Open	
J17	Address decode	Open	
AMPLIFIER ANALYSER CARD			
JB	DC Restorer ON/OFF	Closed	
JC	Pulse Height Correction ON/OFF	Closed	
JF	Discriminator	Closed	
4 DIGIT BINARY COUNTER CARD			
J1	Address decoder	Open	
J2	Address decoder	Closed	
J3	Address decoder	Open	
J4	Address decoder	Open	
J5	Address decoder	Open	
J6	Address decoder	Open	
J7	Address decoder	Closed	
J8	Address decoder	Open	

Table 2.8 Standard settings (continued)

Switch or Jumper	Function	Setting	Comment
RECORDER CONTROL CARD			
J1	Recorder PM8203A or PM8210/31	Open = 8203/Closed = 8210	
J2	Recorder PM8203A or PM8210/31	Open = 8203/Closed = 8210	
J3	IF baudrate	Closed	
J4	IF Baudrate	Closed	
J5	IF Baudrate	Closed	
J6	IF Baudrate	Open	
J7	Address decoder	Open	
J8	Address decoder	Open	
J9	Address decoder	Open	
J10	Address decoder	Closed	
J11	Address decoder	Open	
J12	Address decoder	Closed	
J13	Address decoder	Open	
J14	Address decoder	Open	
CHANGER/SPINNER/SHUTTER CONTROL CARD			
J1	Address decoder	Open	
J2	Address decoder	Open	
J3	Address decoder	Open	
J4	Address decoder	Closed	
J5	Address decoder	Open	
J6	Address decoder	Closed	
J7	Address decoder	Open	
J8	Address decoder	Open	
MOTHERBOARD			
J1	External Amp. input to X22	Open	
J2	External Amp. output to X22	Open	
J3	External Amp. input to ground	Closed	
J4	Second Detector selector to ground	Closed	
J5	+5V to LL input to Discriminator	Open	
J6	+5V to UL input to Discriminator	Open	
J7	X19 to Calib. input of Amplifier	Open	
J8	Sec. Cont. Panel to Cal. I/P of Amp.	Closed	
J9	Ratemeter output to X22	Closed	
J10	Ratemeter output to Recorder Control	Open	
J11	Option Rack indicator to ground	Open	

2.8 OPERATION

2.8.1 SWITCHING ON/OFF

The first time switching-on after installation should only be performed by a philips service engineer.

2.8.1.1 Pre-adjustments

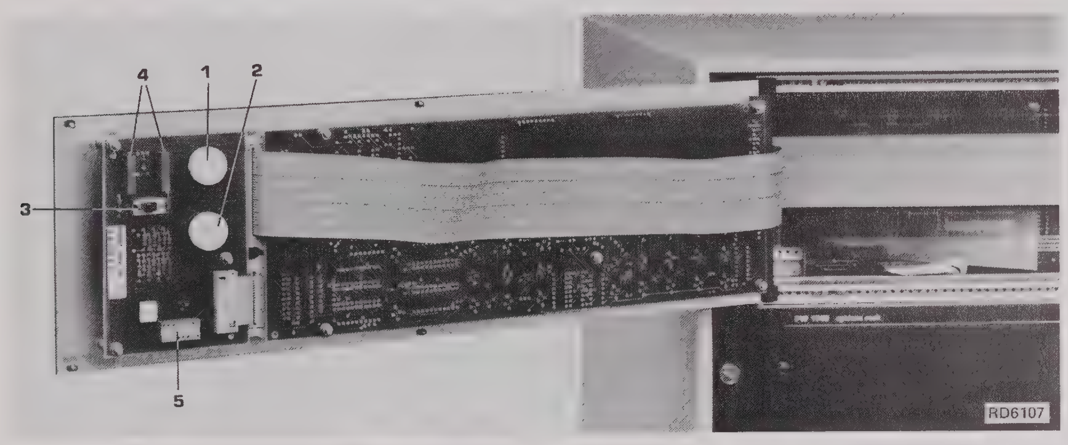


Figure 2.18 Secondary Control Panel

Check that the x-ray generator has been switched off, then open the front panel of the PW1710 and select the following parameters:

1. Switch S5, Tube selector . . . . Set switch S5 to the anode material of the x-ray tube in your system.
2. Switch S4, ATT selector . . . . Switch S4 to the 9th position = 2.
3. Switch S6, Detector sel . . . . Switch S6 to left or right position. (GAS or SCINT : PW1711 or PW1964)
4. Detector H.V. . . . . R17 and R20. Do not adjust at this time.
5. Hardware settings . . . . Set the 8 slide switches according to the hardware configeration of the system, and according to table 2.9.

Table 2.9 Hardware Switch Position

HWS SW	SWITCH POSITION "0"	SWITCH POSITION "1"
0	Sample Changer PW1775	Sample Changer PW1170
1	2k byte RAM	4k byte RAM
2	Perform Memory Test (during initialization)	Skip Memory Test
3	NO second counting channel	Second counting channel (PW1748) present .
4	SPARE	
5	Printing recorder PM8210/31 present.	Recorder PM8203A present.
6	NO one-theta drive	One-theta drive PW1747 present.
7	NO two-theta drive	Two-theta drive present.

2.8.1.2 First-time Switching ON

IT IS ASSUMED THAT THE X-RAY GENERATOR HAS BEEN INSTALLED AND CHECKED OUT. ALSO THAT THE GONIOMETER HAS BEEN INSTALLED AND MECHANICALLY PRE-ALIGNED.

1. Switch on the generator. Select minimum KV and mA.

2. Connect the PW1710 POWER MODULE to the mains via the mains cord. One end of the mains cord is connected to the rear panel of the module, and the other should be plugged into the generator mains socket (or a separate 220 V mains socket).

   Observe the following:

   - A flash will appear on the screen (this is actually difficult to observe), the BUSY, ASSEMBLY and REMOTE LEDs light, the ASSEMBLY and REMOTE LEDs are switched off, the memory test is executed.
   - On the DISPLAY on the PW1710 front panel, and if present, on the VDU or PRINTER the following message appears:

     VS x.x TERMINAL =

     x.x is the version number of the PW1710 software.

IF THESE EVENTS DO NOT OCCUR AS DESCRIBED. SWITCH OFF THE PW1710 POWER MODULE AND REFER TO CHAPTER 6.

3. Next select the communication position:

   - If the switch "ENTER" is pressed on the front panel of PW1710, the front panel keyboard is assigned by the system as input device. The keyboard of the VDU or the PRINTER are then disabled.

   - If as an answer to the message VS x.x TERMINAL= the RETURN key on the keyboard of a VDU (P817) or a PRINTER (PC1409) is pressed, the system will assign that keyboard as the input device.

   After depressing "ENTER" or "RETURN" the goniometer runs to the lower limit switch, calibrates, and then runs to $+5^{\circ}$ above the lower limit, and the message C= appears on the terminal.

AT THIS POINT PW1710 COMMANDS CAN BE ENTERED.

NOTE: If after the message "VS x.x TERMINAL =" another character is typed, (instead of ENTER or RETURN), and if that character is an ASCII code, the display and/or printer will show in the print-out a "Communication Character" at the beginning of the line. To get rid of this character, switch OFF and ON, (PW1710), or use the RESET switch.

4. Check that the safety devices function correctly:

   - Check that the shutter closes in any of the following cases:

     * If the specimen chamber is opened.

     * If the cap of the receiving slit is removed.

     * If the detector and/or monochromator is removed.

     * If the beam exit tube of the radiation shield is removed from the receiving slit assembly.

*NOTE: When a PM8203A has been connected the hardware switch S5 will be set to 1. However it may happen that when asking PAR, the ** 15 RECORDER ERROR appears. In that case PON from the last test might still be in the memory. Set switch S5 back to 0 (PM8210), type POF (+ENTER), then set the switch back to 1 for PM8203A.*

AT THIS POINT, STUDY CHAPTERS I AND II OF THE OPERATING MANUAL, AND PROCEED WITH ....

2.8.2 ADJUSTMENTS

2.8.2.1 Goniometer

Refer to the Installation manual for the Goniometer PW1050.

2.8.2.2 Recorder PM8203A and PM8210/31

If a PM8203A recorder is present, make sure that the pen is properly zeroed for use with the PW1710. To do so:

1. Type : MAN .... The BUSY lamp will flicker.

2. At the recorder, set the ZERO/REC switch to REC.

3. If the pen is not exactly aligned with the left-hand line of the chart paper: Adjust the screwdriver adjuster VAR on the front panel of the recorder until the pen is aligned.

NOTE: REC means that the recorder uses the zero from the PW1710.
ZERO means that the recorder uses its own zero.

4. On the PW1710 front panel, press the STOP button.

2.8.2.3 Detector

1. Type: PAR

The following parameter table will be printed:

(On the PW1710 you must keep pressing "ENTER" to scan through the parameter table).

```
LWL 20                        UPL 0
RFS 5E5
RTC .1                        RSP 0
SPE 0.001                     INT 0.00
STP 0.000                     MXN 0
MXS 0.000                     BGM 0
MXT 0.00                      WAV 0.00000
BGT 0.00
BGA 0.000
SOF        ROF        DOF        POF
ZERO 2T= 0.000
```

The system will print the actual values or status of these parameters.

2.8.2.4 Alignment Check

1. Select 40 kV and 30 mA on the x-ray generator.

2. Type: DPL X (The display will show XI 0, this is the intensity in counts per second).

3. Type SAN 145 ...... Set the 2 θ angle to 145^{o}.

4. Insert a FLUORESCENT disc.

5. Open the shutter.

6. Check the illumination of the FLUORESCENT disc. The illumination should cover the center area symmetrically around the center line.

7. Close the shutter and insert a SILICON sample.

8. Give the following commands:

   SAN 28.45 .... Open the tube shutter and observe the counts, the intensity will be approximately between 10,000 and 20,000 counts per second.

   LWL 49
   UPL 51 .... A window of 2%

   While pressing in the push-button CAL on the secondary control panel, adjust the intensity to a maximum number of counts by adjusting the HT potentiometer R20 (if using a Scintillation detector) or R17 (if using a Gas detector). Refer to figure 2.18.

   Release the push-button CAL. The intensity should not change, if it does so, re-adjust the HT potentiometer until NO change occurs when you release the push-button.

9. Now draw a PHD curve on the recorder, do that as follows:

   If you have Recorder PM8203A give .... RLF

   OR

   If you have recorder PM8210/31 check that the pen is located over a thick line on the graph paper.

   Now give the following commands:

   RFS 1E4 .. This and the next command set the recorder to the correct
   RTC 1 .... scale for the PHD curve.

   PHD ..... Pulse Height Distribution, this will cause a graph to be drawn on the recorder. It takes approximately two minutes for this graph to be drawn. Figure 2.19 shows an example of a typical PHD curve.

10. Use the graph that has just been drawn to work out where to set your upper and lower limits. Do that as follows:

    a. Draw a line through the peak on the chart (A on figure 2.20), on either side of the peak where the curve straightens out draw another line (marked B and C on figure 2.20).

    b. Say that the center line on the graph (A) is at 50%.

    c. Count the number of lines between the center 50% line and the other two lines B and C. Each line represents 1%. Add or subtract these numbers from 50% to obtain your upper and lower levels. In the example in figure 2.19, the upper level works out to 65%, and the lower level 35%.

11. Now give the following commands to set the goniometer to an angle of 28.465°, and adjust the dial accordingly:

```
LWL  33
UPL  65
MXN  10
MXS  0.01
MXT  1
MAX  The system now searches for the peak and sets the
     goniometer accordingly.
CAN  28.45
     (adjust dial)
MES  10
DEC  0
PTR  0  The measuring result will be printed in c/s.
RCT
PTR  0  Total number of counts will be printed.
RIN
PTR  0  Intensity in c/s will be printed.
```

2.8.3 SYSTEM CHECK-OUT/ACCEPTANCE TEST

SUCCESFULL COMPLETION OF THE FOLLOWING TEST PROCEDURES, ENSURES THAT THE PW1710, GENERATOR, GONIOMETER AND PERIRHERALS ARE PERFORMING TO SPECIFICATION.

In the following check-out procedures, commands and the actions they cause are given in the following format:

```
COMMAND .......... ACTION CAUSED, OR COMMENT
```

Press the RESET button behind the PW1710 front panel, or switch OFF and ON.

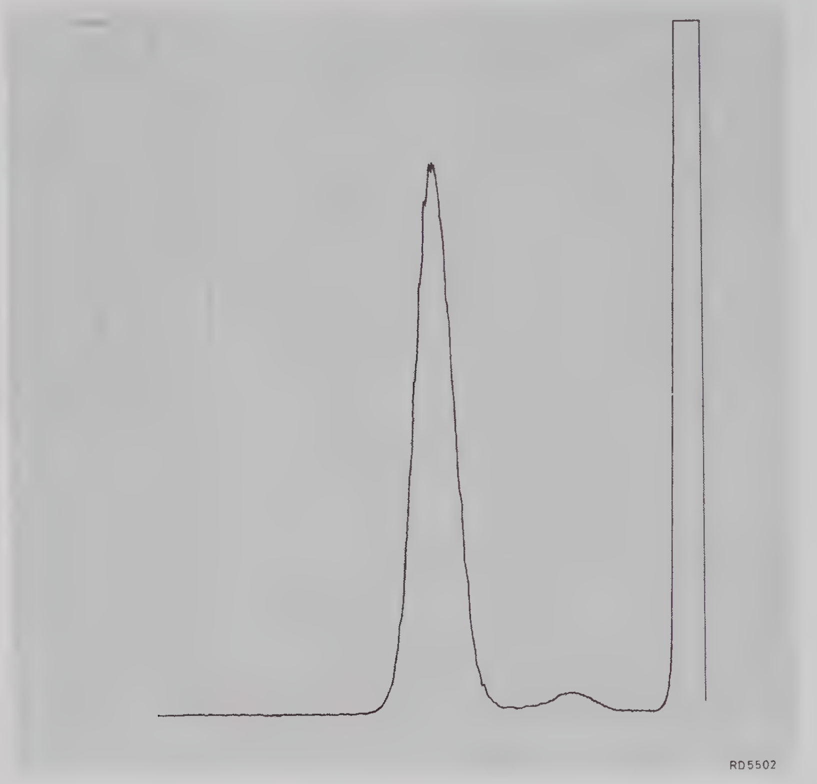


Figure 2.19 Typical PHD Curve

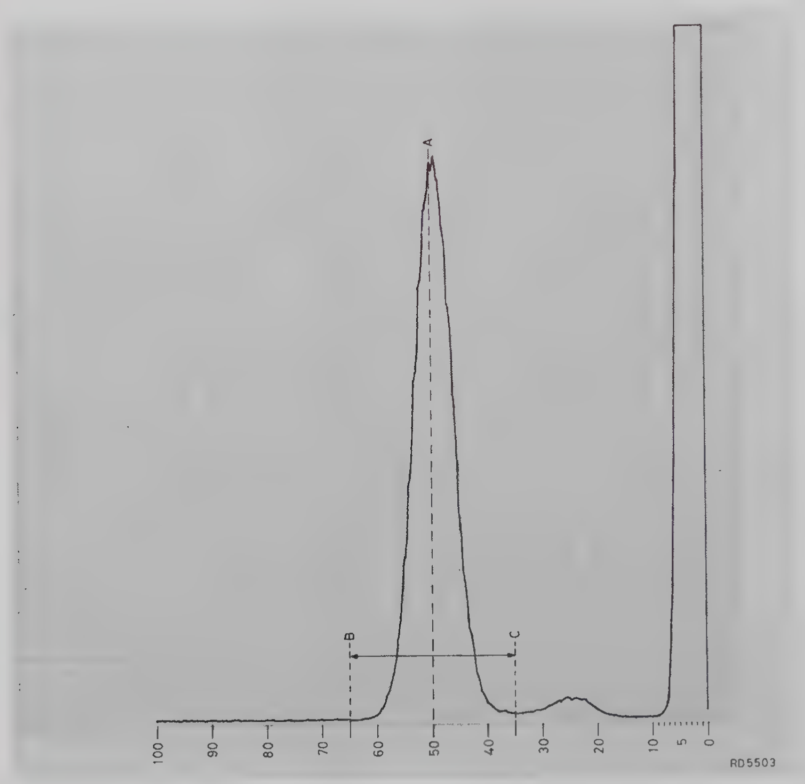


Figure 2.20 PHD Curve with Upper and Lower Levels Marked

2.8.3.1 Display and Front Panel Test

- After "VS x.x TERMINAL" press "ENTER" on the PW1710 front panel.

- Type the letter H 20 times, then STOP
  Type the letter I 20 times, then STOP
  Type the letter X 20 times, then STOP
  Type the . 40 times, then STOP

  IF ALL THESE CHARACTERS CAN BE DISPLAYED ON ALL 20 POSITIONS, THEN ALL THE DISPLAY SEGMENTS ARE O.K.

- Press all the other CHARACTERS on the front panel. (If ENTER is depressed, error message : ** 2 UNKNOWN COMMAND or ** 1 ILLEGAL ARGUM. is displayed).

- Press any character 20 times to fill the display.

- Press CLEAR 20 times to clear the display.

2.8.3.2 Terminal

Press the RESET button behind the PW1710 front panel, or switch OFF and ON.

- If a VDU or other TERMINAL has been connected, the message VS x.x TERMINAL= should appear on this peripheral as well. In this case the connection is correct.

- At the terminal enter CR (carriage return)

- Type HED a heading will appear.

- Type DAT dd mm yy
  TIM hh mm
  IDT PW1710 CHECK
  HED

NOTE: Do not enter a space before these commands.

Output on the terminal will be :
```
PW1710 CHECK dd-mm-yy hh.mm PROGRAM 0
```

2.8.3.3 Recorder

SAN 28.465	(SI reflection, CU tube)
DPL X	Read value of XI and divide by 5, then select for RFS (Recorder Full Scale), the next larger value.
RFS 5E3	(5E3 = a full scale of 5 000).

RON (PON if the printing recorder is present)

RTC S

The recorder should be in REMOTE and REC mode, switched ON and the chart drive set to 10.

PHD	Recorder starts writing for 20 cm or STOP. Keep this diffractogram with the log-book for future reference. Refer also to paragraph 2.8.2.4.
RSP 10	
SAN 25	
SPE 0,05	
INT 0	
CSC 5	Recorder writes 5 cm diffractogram with a peak around 28.465 degrees. Also keep this diffractogram with the log-book for future reference.

NOTE: If a PM8210/32 is installed and you want it to print d-spacings value of 3,138xx (copper tube) at the peak, you must change the command CSC to CSP, and INT0 becomes INT1. In this case make sure that the tube wavelength WAV 1,5418 is in the parameter list.

IF A PRINTING RECORDER PM8210/32 is present, add the following:

PON	
HED	A heading will be printed by the recorder.
POF	
HED	Printhead has been switched off.

2.8.3.4 Check of Second Output Channel

It is assumed that a PW1409/01 has been connected to the second output. This output at the rear panel of the PW1710 Power Module is marked 2.

Press TERM READY on PW1409. The indicator DATA lights.
Select PARITY DOWN, FULL DUPLEX DOWN, 30 CPS UP.

DON	
HED	A heading will be printed.
DOF	
HED	Interface 2 switched off.

2.8.3.5 Goniometer

Press the RESET button through the PW1710 front panel, or switch OFF and ON.

Select PW1710 or Terminal (ENTER or CR), and give the following commands:

ASS 44	
DPL G	The 2 theta angle is displayed on the left-hand part of the display.
SPE 0.5	Goniometer speed of 0.5°/second.
STP 0.1	Step size of 0.1/step.
INT 2.	Interval time of 2 seconds.
ROF	Recorder ratemeter on.
SAN 120	Slew to 120° 2 theta.
MES 5	Measure for 5 seconds at 120°.
SAN 10	Slew to 10° 2 theta.
CSC 10	Continuous scan +10°.
or	
CSP 10	Continuous scan +10° with peak labeling.
SSC 10	Step scan +10°.

2.8.3.6 Sample changer PW1170

HWS switch # 0 on the secondary control panel behind the front panel should be in position 1.

THE SUPPLY VOLTAGE FOR PW1170 SHOULD BE SET TO 48 V a.c. REFER TO SECTION 2.4.

Press the RESET button behind the PW1710 front panel, or switch OFF and ON.

Select PW1710 or Terminal (ENTER or CR), and give the following commands:

DPR S	Sample = cassette position
DPL C	Command
MAG 0	Cassette transport mechanism goes up. When it reaches position zero, the display will show "SAMPLE 0". When it is in position zero, place a cassette module without any sample holders in position on the changer.
MAG 36	** 1 ILLEGAL ARGUM is displayed. (This is a test of the correct positioning of the hardware selection switch). Fix the end stop in the highest position (35). The top of the end stop marks the position.
ENTER	Clears the display ready for the nextcommand.
MAG 1	Adjust the viewing window to show 1.
MAG 35	Display indicates successive positions. If the display shows SAMPLE 35 then all positions have been "seen".
MAG 25	Fix the end stop at position 30.

MAG 35	** 17 CHANGER ERROR SAMPLE 30 is displayed. The end stop has prevented the transport going to position 35.
ENTER	Clears the display ready for the next command.
MAG 4	** 17 CHANGER ERROR is displayed, but the module travels.

while the module is still travelling:

ENTER	The display will show the successive positions of the magazine, down to zero and back to four.
LSM	Loading motor runs and the sample is loaded.
MAG 6	** 18 SAMPLE ERROR. The magazine cannot run while a sample is loaded.
ENTER	
USM	The motor runs and the sample is unloaded.
MAG 6	

Assemble program 117 ......

ASS 117	
DPR S	
DPL C	
RON	
USM	Only if the machine has been stopped.
SCH 1 5	To enter a space via the PW1710 front panel, you must press "." (point) twice.
RLF	Only if P8203A is fitted.
SAN 25	
MES 1	
SAN 15	
NXS	
MAG 1	
/ or STOP	
117	Program 117 (measure 1 second) will be executed for positions 1 to 5.

2.8.3.7 Changer Spinner PW1775

HWS switch S0 on the secondary control panel should be set to 0.

Depending on whether you have thick or thin samples, set the 42-21 switch in the PW1775 Sample Changer (21 = thick samples, 42 = thin samples). Refer to the PW1775 manual.

DPR S	
DPL W	
MAG 1	Magazine goes to lowest position. Display shows SAMPLE 1. Put sample holders in positions 1, 3, 5 and 7. Replace the magazine.
MAG 50	** 1 ILLEGAL ARGUM (for thick samples max 21).
ENTER	Clears the display for the next command.
MAG 21	Magazine goes up; Display follows. When SAMPLE 21 is displayed:
LSM	Goniometer runs to 12 degrees above the calibration point, and loads from an empty position. AS there is no sample, the display will show ** 21 NO SAMPLE, and the shutter should not open.
ENTER	To clear for the next command.
MAG 7	The magazine runs to position 7.
SAN 25	Goniometer runs to 25°.
LSM	Goniometer runs to 12° above the calibration point, loads, the lift goes up, (part of the loading action), and the shutter opens.
SON	Spinner runs (listen for the motor: it clicks when it starts).
SOF	Spinner halts.
USM	Shutter closes, the lift goes down, and the sample is returned to the magazine.
LSM	The sample is loaded again.
MAG 5	The magazine runs to position 5.

When the display shows SAMPLE 5:

USM	** 20 SAMPLE IN MAGAZINE (The sample changer was commanded to unload the sample to an already full position).
ENTER	Clear for the next command.
LSM	** 19 SAMPLE IN GONIOMETER (The sample changer was commanded to load when already loaded).
ENTER	Clear for the next command.
LSS	** 19 SAMPLE IN GONIOMETER (The sample changer was commanded to load when already loaded).
ENTER	Clear for the next command.
USS	Sample unloads to the priority position.

LSM .... Loading from position 5.

USM .... Return the sample to position 5.

MAG 7

LSS .... Loading from priority position.

USM .... Back to position 7.

Assemble program 177 ....

ASS 177

DPR S

DPL C

RON

SCH 0 0

RLF .... Only if PM8203A is present.

SAN 15

MES 3

NXS

/ or STOP

MAG 1

REP 177 5 .... Samples 1, 3, 5 and 7 will be measured for 3 seconds, the magazine then runs to the last position and stops.

2.8.3.8 PW1747 Additional Stepping Motor Control

MOD 3 .... Scan mode 3, which means theta, 2θ fixed.

DPL G .... Display left 2 theta.

DPR T .... Display right theta.

SAN 10.000 .... Set angle of 10°.
SPE 0.20 .... Goniometer speed of 0,2°/second.

RSP 10 .... Recorder paper speed of 10mm/°2θ.

RON .... Switch the ratemeter on.

CSC 4.000 .... A continuous scan of 4° is made. The goniometer stops at $2\theta = 14°$ and theta = 7°.

STH 8.000 .... Set theta to 8°, an offset of 1°.

CSC 4.000 .... A continuous scan of 4° is made. The goniometer stops at $2\theta = 18°$ and theta = 10°.

MOD 1 .... Scan Mode 1 means that 2θ is fixed, and theta can

SAN 45.000 .... Set Angle to 45° 2θ. This means that the 2θ angle is set to 45°, theta will be set to 22.5°.

CSC 2.000 .... The theta drive scans for 2°, stopping at 24.5°. The 2θ drive remains at 45°.

MOD 2 .... Scan Mode 2 means that the theta drive is fixed, and the 2θ drive can scan.

SAN 60.000 .... Set Angle to 60° 2θ. This means that the 2θ angle is set to 60°, theta will be set to 30°.

CSC 4.000 .... The 2θ drive scans 4°, stopping at 64° 2θ. The theta drive remains on 30°.

STH 0.000 .... The theta drive runs to zero. 2θ remains at 64°.

STT 0.000 .... The 2θ drive runs to zero.

2.8.3.9 Programming

Press the RESET button behind the front panel, or switch OFF and ON.

PMM .... If the memory contains programs, the program numbers will be printed. If you have selected the terminal as control device, the number of registers in use will be printed as well.

If the PW1710 is the control device:

ENTER .... The number of registers in use will be displayed.

ENTER .... The free space will be displayed.

ENTER .... Clear the display ready for the next command.

To clear the existing programs and clear the registers:

DLP x .... x = program number

NRG 0

To make program 0, give the following commands:

NLC 23 3

PRP

ASS 0

SAN 10

DPL X

DPR G

Terminal WAV 1.5418 ...... CUKa
OR
PW1710 WAU 1.5418 ...... CUKa

LWL 35

UPL 70

/ or STOP

PRP 0

0 .... Goniometer runs to 10° and the countrate is displayed.

To make (assemble) program 60, give the following commands:

```
ASS 60

SAN 15

RON
RFS 5E4

RTC S

RSP 4

PON

SPE 1

INT 0.05

CSP 75

/ or STOP

PMM ............... 0  60 is displayed.

ENTER ............. NR OF REGISTERS= 0 is displayed.

ENTER ............. FREE SPACE 1473 BYTES is displayed.

ENTER ............. Clear display for next command.
```

To assemble program 66:

```
ASS 66

CLP 0

SAN 28.45

MXN 10

MXS 0.01

MST 1

MAX ............... Read XI and adjust RFS in program 66

/ or STOP

PRP 66 ............ Program 66 will be printed.
```

2.8.3.10 PM4202 Cassette Recorder

If a cassette recorder is present:

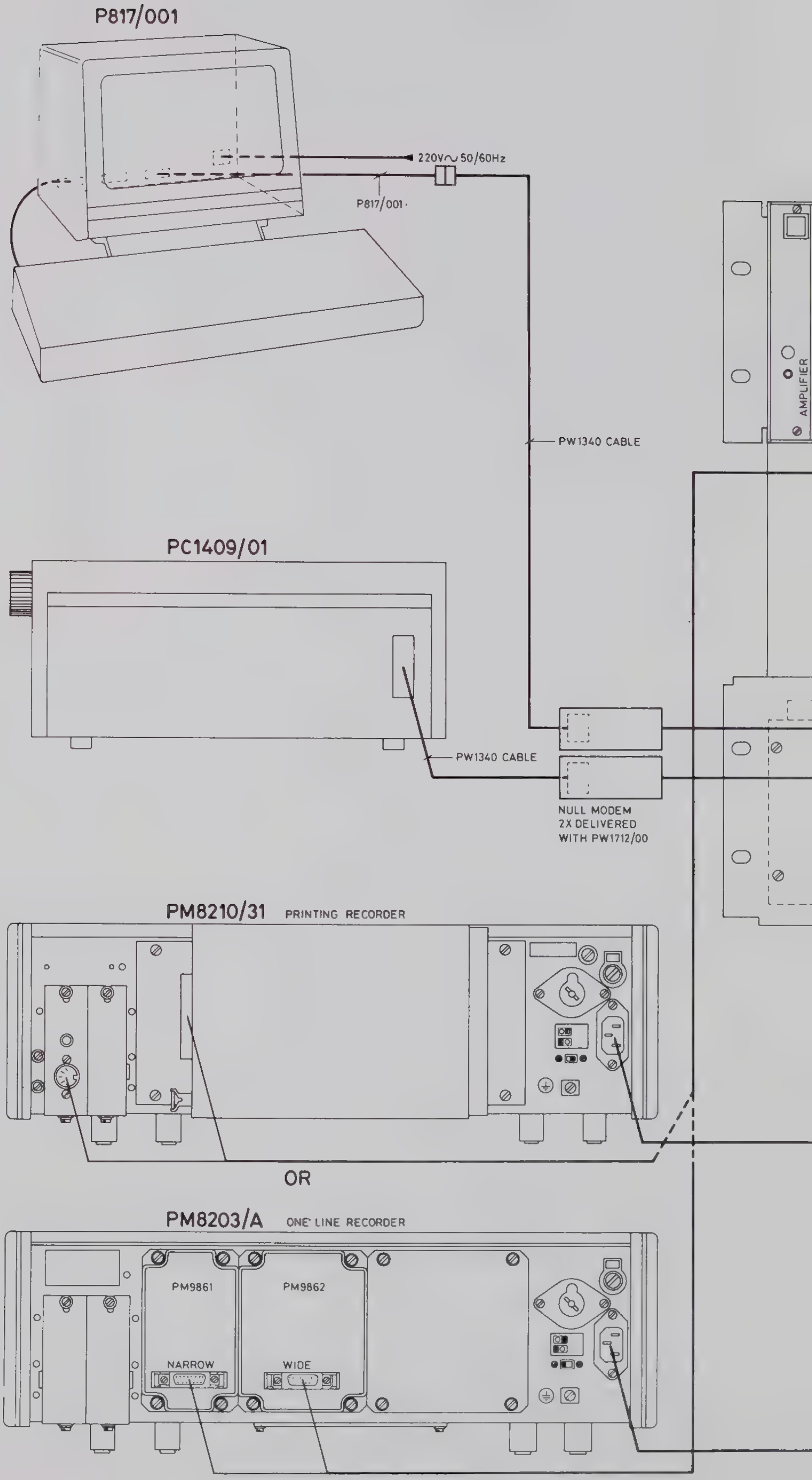
C = WME .... Write RAM contents to cassette. During the write procedure the "WRITE" LED on the PM4202 will be lit. After the contents have been written to the cassette the "WRITE" LED will extinquish and the recorder will switch to standby ("STANDBY" LED will light).

C = DLP xx .... Delete all current programs.

Press REVERSE on the recorder twice. The first time to rewind ("BUSY/END OF TAPE" LED lights) the second time to ensure that the "BUSY/END OF TAPE" was not missed.

C = RME .... Read data from cassette and store it in RAM. During the read procedure the "READ" LED on the PM4202 will be lit. At the end of the data the "END OF DATA" LED will light and the recorder will switch to standby ("STANDBY" LED will light).

C = PRP .... Print all Programs. Verify the program with the original.


P817/001
220V∿ 50/60Hz
P817/001
PW1340 CABLE
AMPLIFIER
PC1409/01
PW1340 CABLE
NULL MODEM
2X DELIVERED
WITH PW1712/00
PM8210/31 PRINTING RECORDER
OR
PM8203/A ONE LINE RECORDER
PM9861
PM9862
NARROW
WIDE

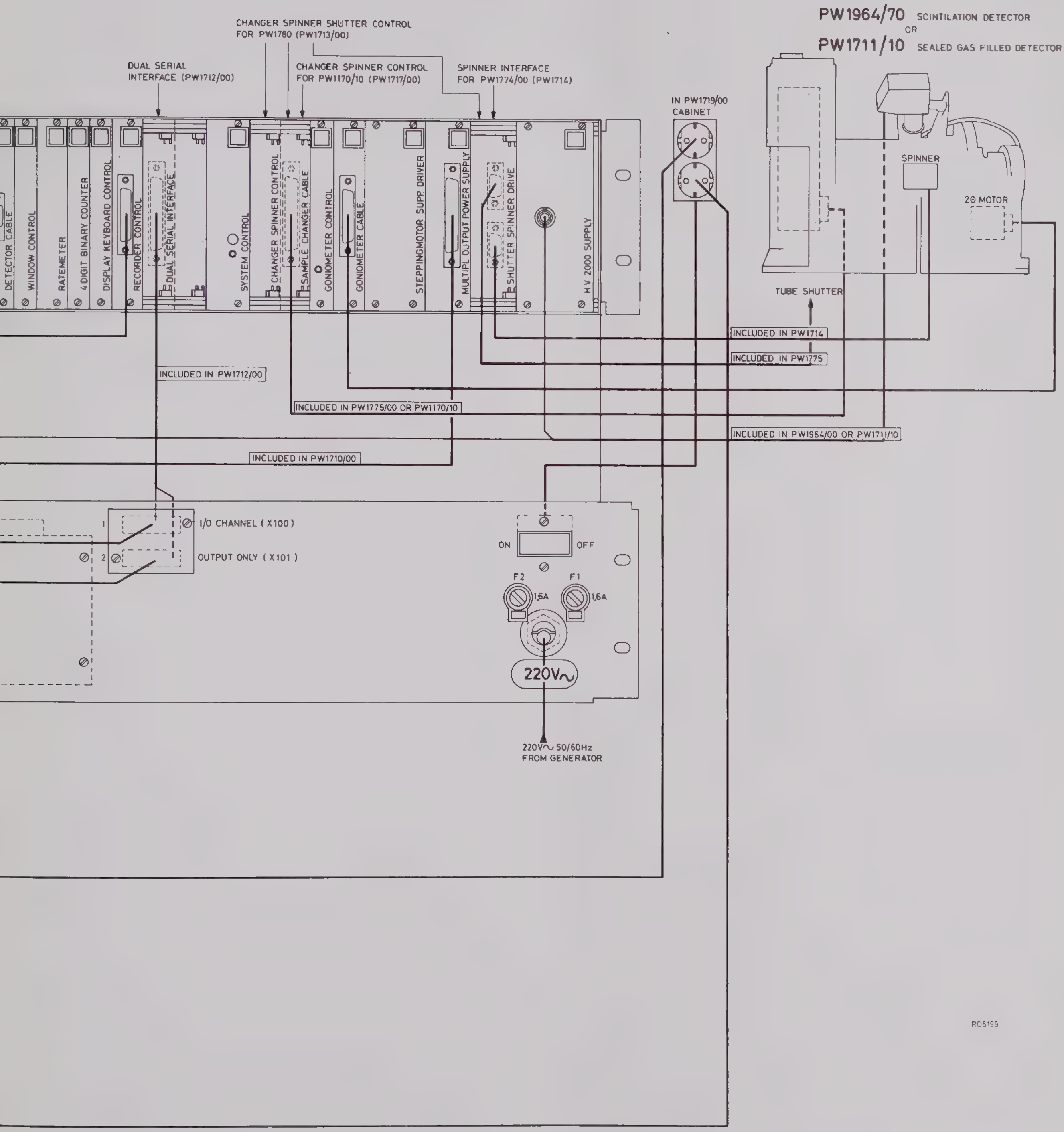

PW1964/70 SCINTILATION DETECTOR
OR
PW1711/10 SEALED GAS FILLED DETECTOR
CHANGER SPINNER SHUTTER CONTROL FOR PW1780 (PW1713/00)
DUAL SERIAL INTERFACE (PW1712/00)
CHANGER SPINNER CONTROL FOR PW1170/10 (PW1717/00)
SPINNER INTERFACE FOR PW1774/00 (PW1714)
IN PW1719/00 CABINET
DETECTOR CABLE
WINDOW CONTROL
RATEMETER
4 DIGIT BINARY COUNTER
DISPLAY KEYBOARD CONTROL
RECORDER CONTROL
DUAL SERIAL INTERFACE
SYSTEM CONTROL
CHANGER SPINNER CONTROL
SAMPLE CHANGER CABLE
GONIOMETER CONTROL
GONIOMETER CABLE
STEPPINGMOTOR SUPP DRIVER
MULTIPL OUTPUT POWER SUPPLY
SHUTTER SPINNER DRIVE
H V 2000 SUPPLY
SPINNER
2θ MOTOR
TUBE SHUTTER
INCLUDED IN PW1714
INCLUDED IN PW1775
INCLUDED IN PW1712/00
INCLUDED IN PW1775/00 OR PW1170/10
INCLUDED IN PW1964/00 OR PW1711/10
INCLUDED IN PW1710/00
1
2
I/O CHANNEL (X100)
OUTPUT ONLY (X101)
ON
OFF
F2
F1
1,6A
1,6A
220V∿
220V∿ 50/60Hz
FROM GENERATOR
RD5199

Figure 2.21 Interconnection Diagram

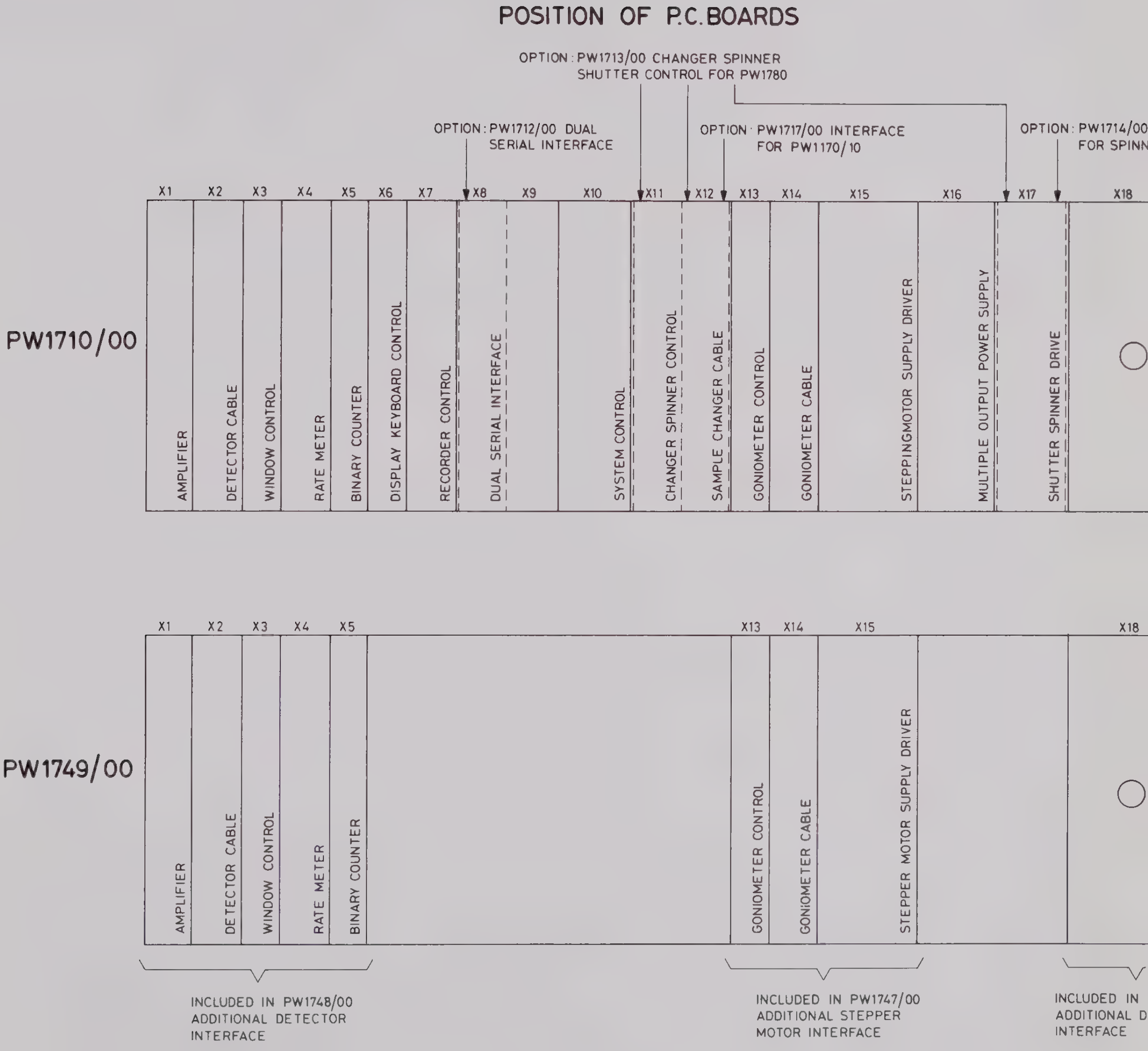
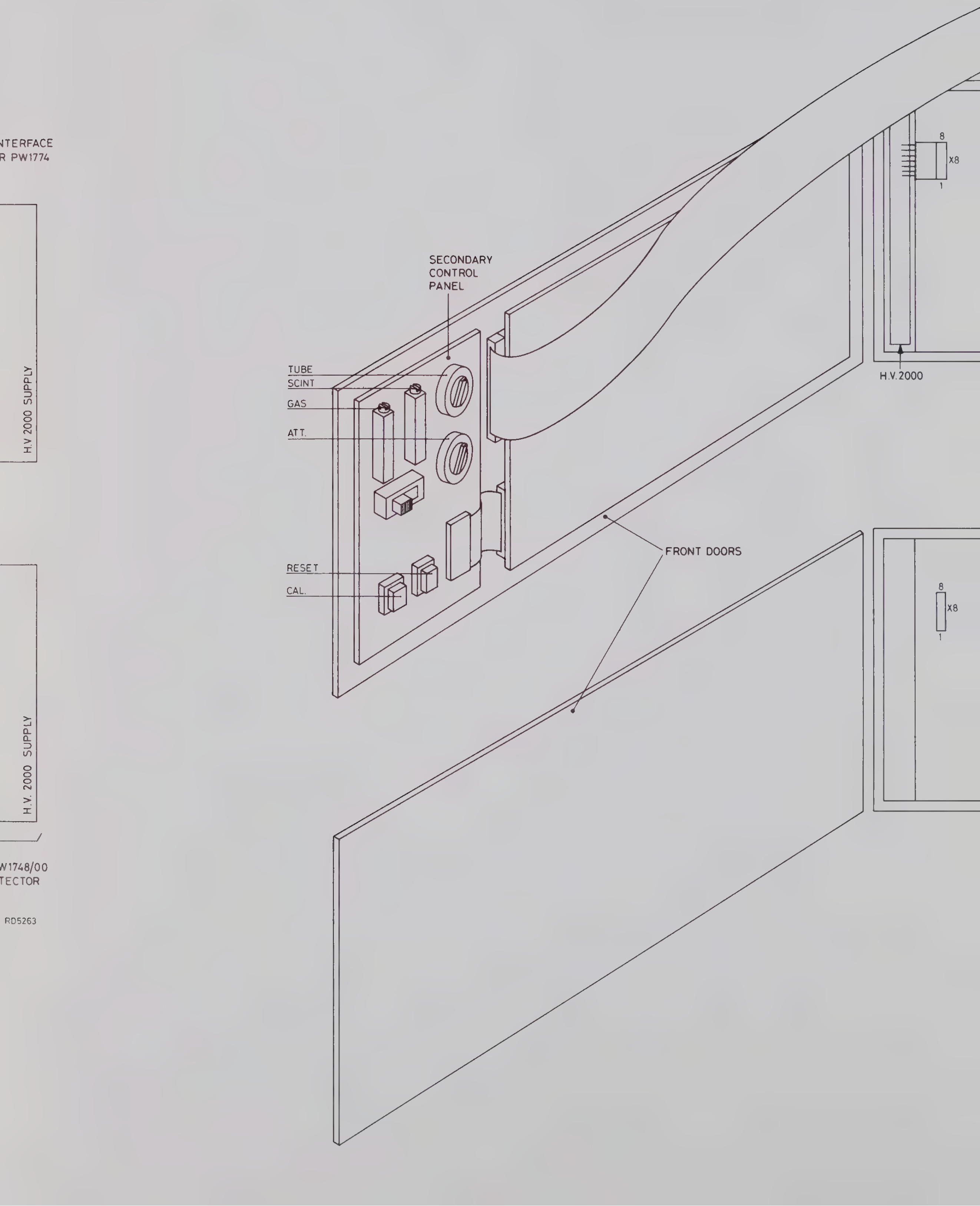

POSITION OF P.C. BOARDS
OPTION: PW1713/00 CHANGER SPINNER SHUTTER CONTROL FOR PW1780
OPTION: PW1712/00 DUAL SERIAL INTERFACE
OPTION: PW1717/00 INTERFACE FOR PW1170/10
OPTION: PW1714/00
FOR SPINN
X1
X2
X3
X4
X5
X6
X7
X8
X9
X10
X11
X12
X13
X14
X15
X16
X17
X18
PW1710/00
AMPLIFIER
DETECTOR CABLE
WINDOW CONTROL
RATE METER
BINARY COUNTER
DISPLAY KEYBOARD CONTROL
RECORDER CONTROL
DUAL SERIAL INTERFACE
SYSTEM CONTROL
CHANGER SPINNER CONTROL
SAMPLE CHANGER CABLE
GONIOMETER CONTROL
GONIOMETER CABLE
STEPPINGMOTOR SUPPLY DRIVER
MULTIPLE OUTPUT POWER SUPPLY
SHUTTER SPINNER DRIVE
PW1749/00
X1
X2
X3
X4
X5
X13
X14
X15
X18
AMPLIFIER
DETECTOR CABLE
WINDOW CONTROL
RATE METER
BINARY COUNTER
GONIOMETER CONTROL
GONIOMETER CABLE
STEPPER MOTOR SUPPLY DRIVER
INCLUDED IN PW1748/00 ADDITIONAL DETECTOR INTERFACE
INCLUDED IN PW1747/00 ADDITIONAL STEPPER MOTOR INTERFACE
INCLUDED IN
ADDITIONAL D
INTERFACE

Figure 2.22 Position of Printed Circuit Boards


NTERFACE
R PW1774
H.V 2000 SUPPLY
H.V. 2000 SUPPLY
W1748/00
TECTOR
RD5263
SECONDARY
CONTROL
PANEL
TUBE
SCINT
GAS
ATT.
RESET
CAL.
FRONT DOORS
8
X8
1
H.V.2000
8
X8
1

WIRING PW1710 - PW1749

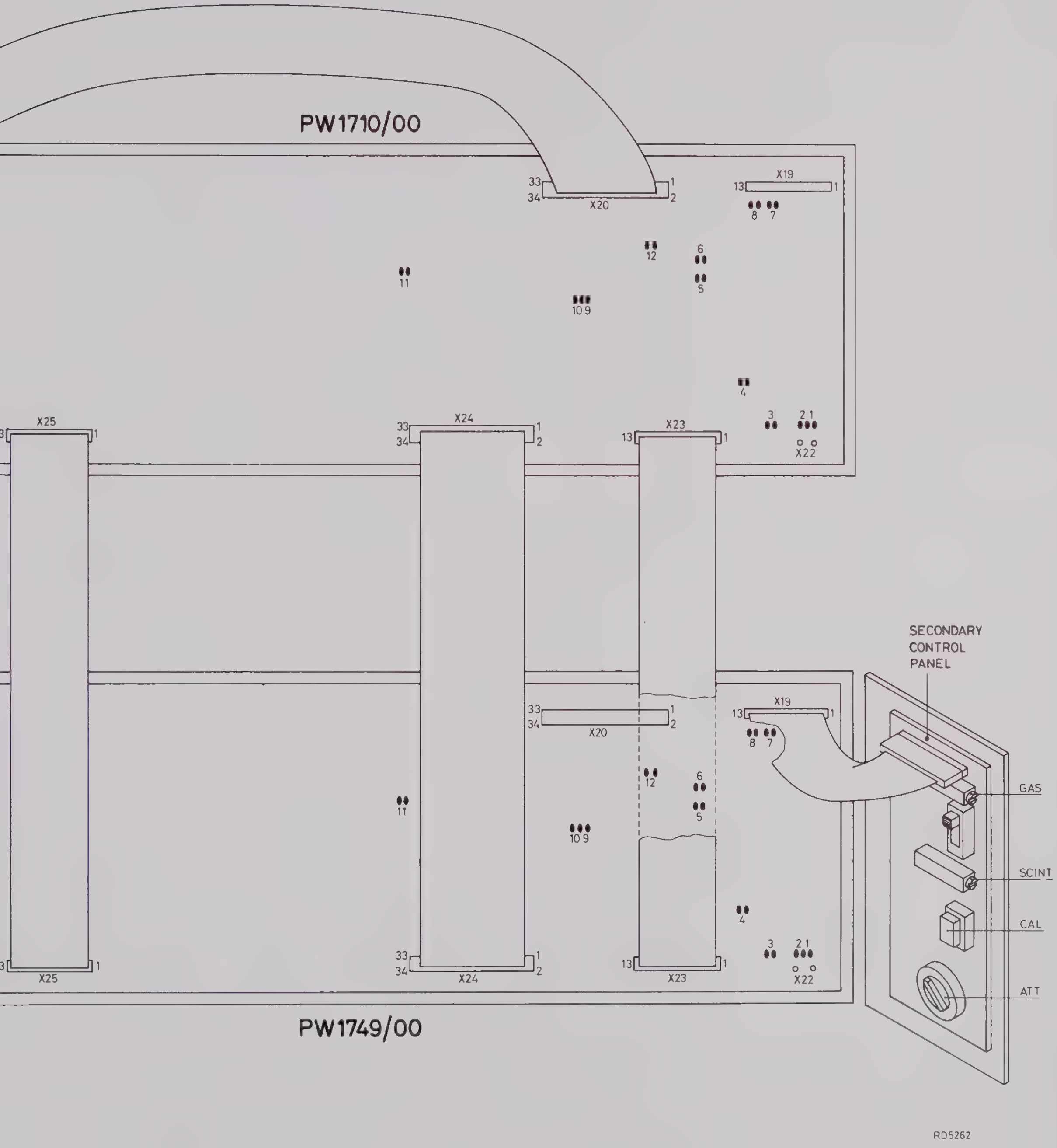

PW1710/00
X19
13
1
8
7
33
34
X20
1
2
12
6
5
11
10 9
4
3
2 1
X22
X25
1
X24
33
34
1
2
X23
13
1
SECONDARY
CONTROL
PANEL
GAS
SCINT
CAL
ATT
PW1749/00
RD5262

Figure 2.23 Wiring between the PW1710/00 and the PW1749/00

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3.1 INTRODUCTION

The PW1710 is an electronic unit, built around a microprocessor, intended to control a diffractometer system (HT-generator, X-ray tube, goniometer, detector and so on). The microprocessor controls a number of hardware and software functions in this unit. The hardware functions are:

* Full control of a goniometer, equipped with one or two stepper motors with shaft encoders, which can be driven independantly or coupled in a two-to-one ratio. The shaft encoder permits short setting times.

* Full control of either, one counting channel, or two channels simultaneously. Controls include the setting of the pulse height selection levels, the full scale value for the counting range and its time constant, and parameters which influence the size of the diffractogram and the additional information to be printed on a strip chart recorder.

* Full control of two types of sample changers.

* Continuous simultaneous display of two user-selected parameters.

* Full control of up to two terminals or a digital cassette recorder with a wide selection of communication parameters.

Furthermore, the ROM-based software considerably facilitates the efficient use of the whole diffractometer and the task of converting raw data into easy-to-read results. Software functions include:

* Conversion of angular values to d-values.

* Labelling of detected peaks for qualitative analysis, either on a printer or on a printing recorder.

* Automated background subtraction (area or peak).

* Programmable calculator functions (four basic functions + square root) plus a user-defined number of registers to hold temporary results and constants.

* User-defined output format to printer or computer.

* Non-volatile storage capacity for user-defined analytical programmes.

* Continuous monitoring of the system´s status, and generation of self-explanatory error messages.

* Versatile test facility to write to and read from random memory locations. Dedicated test programmes to suite special needs, can be written and executed at the customer´s site.

3.2 MEMORY MAP

All the above mentioned functions can be accessed by the microprocessor, therefore, all functions must have a unique address. A survey of all addresses used in the system, is given in figure 3.1.

There are two possible ways of addressing hardware:

* Standard mapped I/O: Cards with I/O functions on them are treated as real I/O ports. This method is not flexible with the 8085 microprocessor as only processor I/O instructions can be used.

* Memory mapped I/O: Cards with I/O functions on them are treated as memory locations. All memory reference instructions can be used, this is a big advantage for the programmer.

In the PW1710, memory mapped I/O is used.

3.3 THE XRA-BUS

All hardware functions are implemented as slaves to the single master (the X-ray Bus Controller). Communication between the master and the slaves is via a bus system, the XRA-bus. This bus, defined within the analytical equipment department in Almelo, is used throughout the whole product range (diffractometers as well as spectrometers). It is a subset of the microprocessor bus. It employs +12V logic to ensure sufficient immunity to noise. The bus consists of five groups of lines:

* Four supply lines
* Eight data lines
* Eight address lines
* Four control lines
* Four interrupt lines

The lines within these groups are as follows:

The four supply lines are:

Stabilized +5V, +12V, -12V and Ground.

The eight data lines are:

IOBU7+ (MSB) to IOBU0+ (LSB) which will be transferred in one cycle. The logic is positive (refer to Chapter 4.0.3.3 "Logic").

(MSB = Most Significant Bit; LSB = Least Significant Bit)

The eight address lines are:

Four module address lines: ADRM3- (MSB) to ADRM0- (LSB) which select one module (card) out of a possible sixteen modules.

Four byte address lines: ADRB3- (MSB) to ADRB0- (LSB) which select, on the selected module, one byte out of a possible sixteen bytes.

The logic is negative.

ROM SPACE	ROM 1	0000 0FFF	
	ROM 2	1000 1FFF	
	ROM 3	2000 2FFF	
	ROM 4	3000 3FFF	
	ROM 5	4000 4FFF	
		5000	
		7000	Switches and test pins on Memory Extension Card
		7FFF	
RAM SPACE		8000 87FF	
	RAM 1	8800 8FFF	
	RAM 2	9000 97FF	
		9800 BFFF	
MEMORY MAPPED I/O SPACE		C000	
		C800	Output (select detectors, spinner, 3MHz)
		D000	READ status + READ/RESET XRA-bus Interrupts
		D7FF	
	XRA- BUS	D800 D80F	
		D810 D81F	Dual Serial Interface Card
		D820 D82F	Recorder Control Card
		D830 D83F	Second Goniometer Control Card
		D840 D84F	Window Control Card
		D850 D85F	Ratemeter Card
		D860 D86F	Four Digit Binary Counter Card
		D870 D87F	Goniometer Control Card
		D880 D88F	Sample Changer Control Card
		D890 D89F	Second Window Control Card
		D8A0 D8AF	Second Ratemeter Card
		D8B0 D8BF	Second Four Digit Binary Counter Card
		D8C0 D8FF	Display keyboard Control Card
		E000 FFFF	WRITE Timer Interrupt Frequency

Figure 3.1 PW1710 Memory Map

The four control lines are:

IORED-	Generated by the XRA-bus controller, this indicates that the address lines, put onto the address bus by the XRA-bus controller, are stable. The selected module must put the requested data on the data lines, to be read by the XRA-bus controller. The logic is negative. A basic READ-cycle is shown in figure 3.2 and 3.3.
IOWRT-	Generated by the XRA-bus controller, this indicates that address and data lines, put onto the address and data bus by the XRA-bus controller, are stable. The selected module can memorise this data. The logic is negative. A basic WRITE-cycle is shown in figure 3.4 and 3.5.
READY+	Optionally pulled down by any module having an access time longer than the IORED and IOWRT signals, this is a mechanism to extend these two signals. Each time the XRA-bus controller senses a LOW on this line, it reacts by continuing to sample the READY line at 0.3 microseconds intervals until the line goes high. (Refer to figures 3.2, 3.3, 3.4 and 3.5).
CLEAR-	Generated by the XRA-bus controller, this can be used as a master RESET signal for the hardware.

The four interrupt lines are:

INTR5- to INTR2- are dedicated interrupt lines. Each device, which can interruptect, has a unique interrupt line.

The logic is negative; a pulse of 0.5 microseconds is sufficient to interrupt the XRA-bus controller.

Physically, the XRA-bus is located on the motherboard. The pinout is given below:

A-row		C-row	
01	+5V d.c.	01	
02	+12V d.c.	02	
03		03	
04	IOBU0+	04	IOBU4+
05	IOBU1+	05	IOBU5+
06	IOBU2+	06	IOBU6+
07	IOBU3+	07	IOBU7+
08	ADRB0-	08	ADRM0-
09	ADRB1-	09	ADRM1-
10	ADRB2-	10	ADRM2-
11	ADRB3-	11	ADRM3-
12	BUSYL-	12	READY+
13	IORED-	13	CLEAR-
14	IOWRT-	14	INTR2-
15	INTR4-	15	INTR3-
16		16	
:		:	
:		:	
30		30	
31	-12V d.c.	31	-12V d.c.
32	ground	32	ground

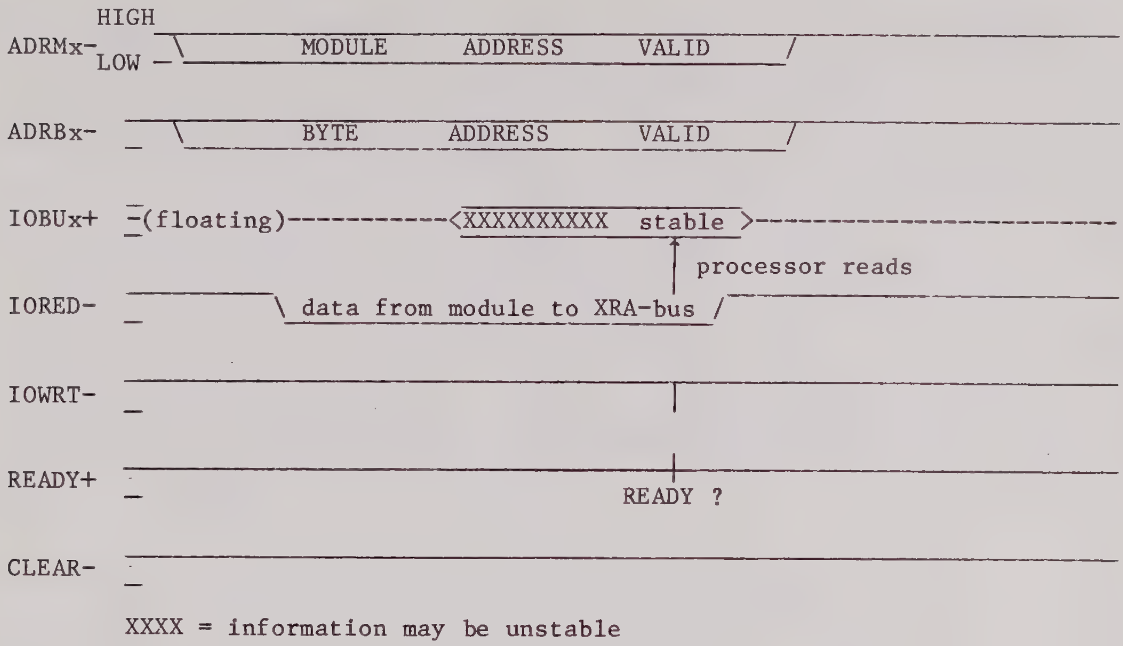

HIGH
ADRMx-
LOW
MODULE ADDRESS VALID
ADRBx-
BYTE ADDRESS VALID
IOBUx+
(floating)
XXXXXXXXXX stable
processor reads
IORED-
data from module to XRA-bus
IOWRT-
READY+
READY ?
CLEAR-
XXXX = information may be unstable

Figure 3.2 Basic XRA-bus READ-cycle without extra WAIT-states

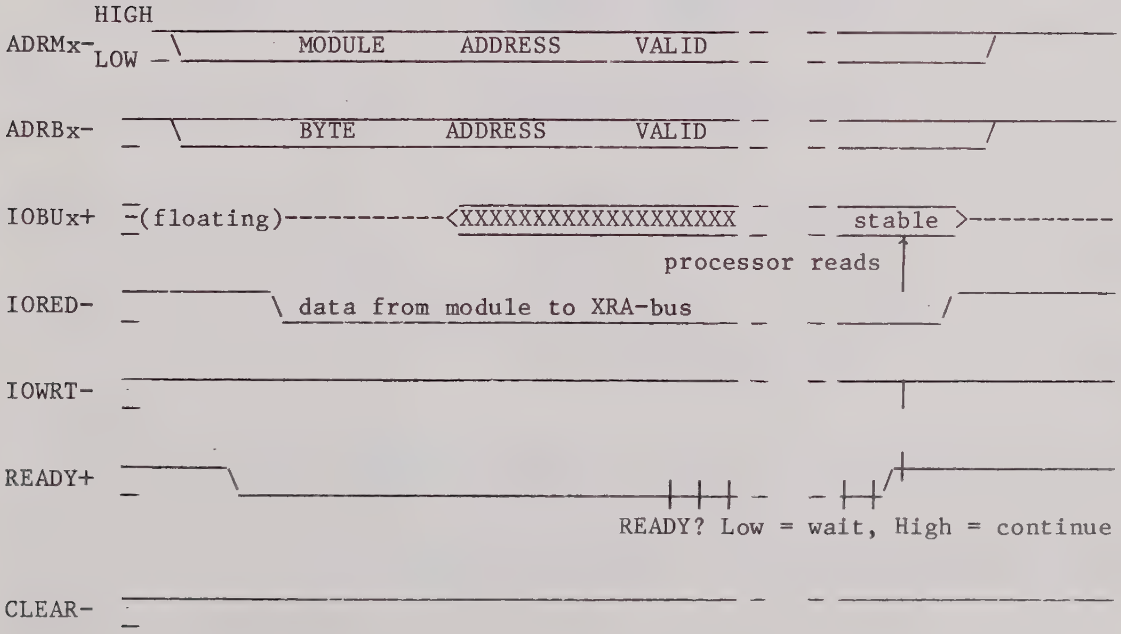

HIGH
ADRMx-
LOW
MODULE ADDRESS VALID
ADRBx-
BYTE ADDRESS VALID
IOBUx+
(floating)
XXXXXXXXXXXXXXXXXXX
stable
processor reads
IORED-
data from module to XRA-bus
IOWRT-
READY+
READY? Low = wait, High = continue
CLEAR-

Figure 3.3 Basic XRA-bus READ-cycle with extra WAIT-states

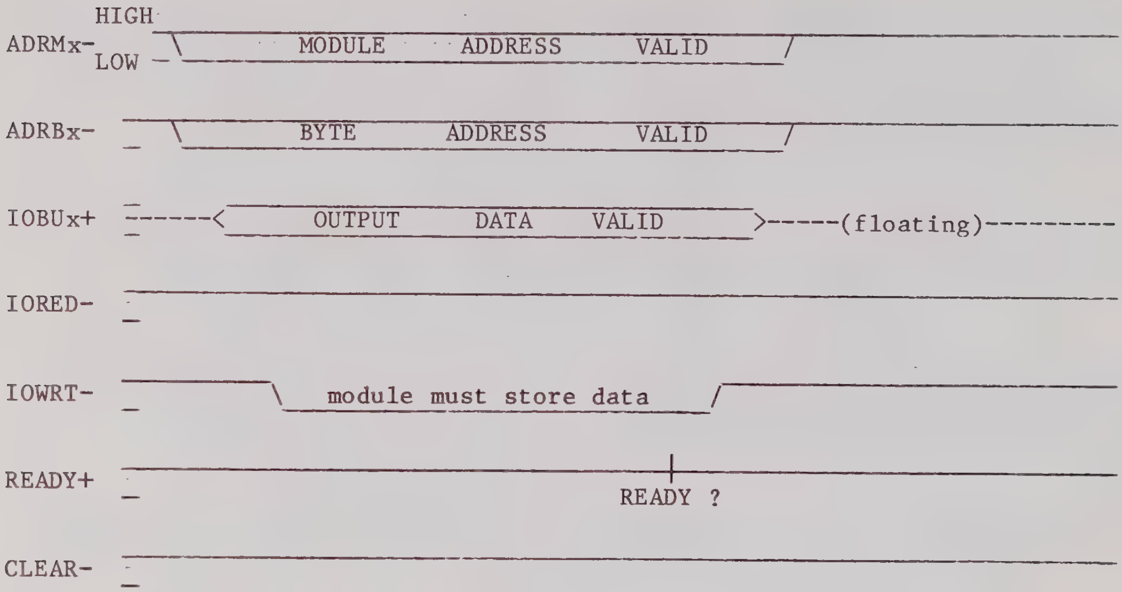

HIGH
ADRMx-
LOW
MODULE ADDRESS VALID
ADRBx-
BYTE ADDRESS VALID
IOBUx+
OUTPUT DATA VALID
(floating)
IORED-
IOWRT-
module must store data
READY+
READY ?
CLEAR-

Figure 3.4 Basic XRA-bus WRITE-cycle without extra WAIT-states

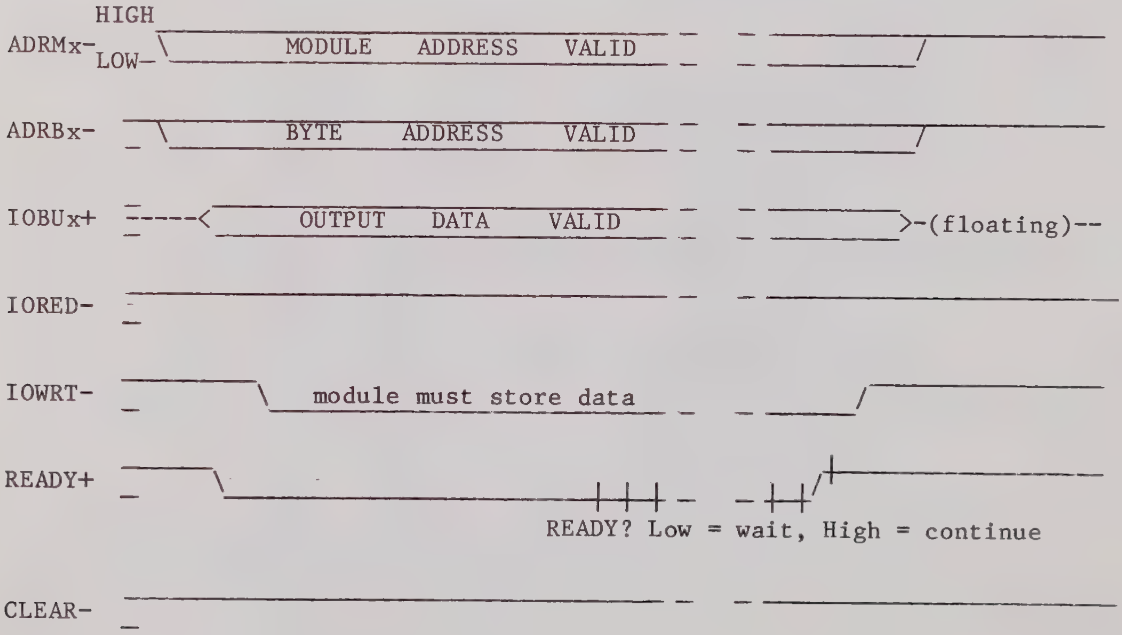

HIGH
ADRMx-
LOW-
MODULE ADDRESS VALID
ADRBx-
BYTE ADDRESS VALID
IOBUx+
OUTPUT DATA VALID
(floating)
IORED-
IOWRT-
module must store data
READY+
READY? Low = wait, High = continue
CLEAR-

Figure 3.5 Basic XRA-bus WRITE-cycle with extra WAIT-states

3.4 THE PW1710 AS A COMBINATION OF HARDWARE FUNCTIONS (refer to figure 3.6)

3.4.1 THE CONTROLLER

This function is performed by a set of two cards, one of them piggy-backed onto the other, the cards are:

SYSTEM CONTROLLER	a microcomputer based XRA-bus controller
MEMORY EXTENSION BOARD	a ROM and RAM memory expansion

The system controller contains all the functions necessary to drive the XRA-bus and to store user data. Therefore it provides the central processing unit (micro-computer), ROM memory (to hold the software), RAM memory (to hold the user parameters and programmes) with battery back-up, XRA-bus driver and receiver circuits and timing circuits.

3.4.2 THE COUNTING (DETECTOR PULSE PROCESSING) CHANNEL

This function is spread over a number of printed circuit boards, which are listed below:

HIGH VOLTAGE 2000	a stabilized 2000V supply
AMPLIFIER ANALYZER	a pulse amplifier and discriminator
CABLE CARD "DET"	connection between motherboard and rear panel
SECONDARY CONTROL PANEL	a card, containing various settings
WINDOW CONTROL	a digital-to-analogue setpoint converter
RATEMETER	a pulse rate-to-analogue converter
RECORDER CONTROL	a signal selector and recorder driver
FOUR DIGIT BINARY COUNTER	a prescaler function

These cards provide sub-functions (facilities) either individually or together with other cards in the group. These sub-functions are:

High voltage

The detector in use requires a high voltage of up to 2000V d.c. This voltage is generated by the HV2000 HIGH VOLTAGE card. The voltage can be adjusted by means of a potentiometer on the back of the PW1710 front cover.

Attenuation

The amplifier on the AMPLIFIER ANALYZER card amplifies, attenuates, separates and reshapes the output pulses from the detector, in order to match the pulse discriminator settings. The amplification has a fixed value, the attenuation setting is done by means of two attenuator switches on the back of the PW1710 front cover (on the SECONDARY CONTROL PANEL). The first switch corrects for the type of x-ray tube in use, the second one has a normal scale of one, square root two, two, and so on.

Discrimination of pulses

The corrected pulses from the amplifier stage of the AMPLIFIER ANALYZER card are applied to the pulse height discriminator stage on the same card. Pulses with a pulse height within the selected window, pass through the discriminator, and can be used for further processing, either in an analogue and/or a digital way.

The window settings are under software control, either immediately by means of a command, or by a command stored in a programme.

Analogue processing

Output pulses from the discriminator are applied to the RATEMETER card, a pulse rate-to-analogue voltage converter. Both the full scale range and the time constant are under software control, either immediately by means of a command, or by a command stored in a programme.

The analogue voltage can be connected to a strip chart recorder by means of the Signal Selector on the RECORDER CONTROL card. The selection is done by the software during the execution of measuring programmes.

The RECORDER CONTROL card provides the necessary hardware to fully control and monitor the strip chart recorder´s functions, either a one-line recorder or a printing one-line recorder.

Digital processing

Output pulses from the discriminator are connected to the FOUR DIGIT BINARY COUNTER card, a prescaler for the microprocessor. At regular time intervals, the microprocessor must read the contents of this counter, and restart counting from zero. Inside the microcomputer, the counts are accumulated and stored in memory for further use.

3.4.3 DISPLAY AND KEYBOARD ON THE FRONT PANEL

This function is spread over two printed circuit boards:

DISPLAY KEYBOARD	20 digit display, keyboard, memory and scanner
DISPLAY KEYBOARD CONTROL	drivers for the Display Keyboard card

The display can show 20 alphanumeric characters. The software divides this display into two parts; therefore two parameters can be shown at the same time. Selection of these parameters is under software control, either immediately by means of a command, or by a command stored in a programme.

The display has an on-board memory, and a self-scanning mechanism. The only task that the processor has to do is to write the requested data (in segment code) for the twenty digits and the three LEDs to this card.

Input of commands to the microprocessor is possible by means of alphanumeric and dedicated keys in front panel mode. The connection between the microprocessor and the DISPLAY KEYBOARD card is the DISPLAY KEYBOARD CONTROL card.

3.4.4 GONIOMETER CONTROL

This function is spread over a set of cards:

GONIOMETER CONTROL	a microcomputer based stepping motor control
STEPPING MOTOR SUPPLY DRIVER	a supply card with power stages for the motor
CABLE CARD "GON"	connection between motherboard and rear panel

The goniometer is driven by a stepping motor with integral incremental shaft encoder. The motor, the encoder, and all their microswitches are controlled and monitored by the Goniometer Control card. All movements (slew and scan) are under software control, either immediately by means of a command, or by a command stored in a programme.

3.4.5 COMMUNICATIONS

As an option, two RS232C/V24 compatible serial ports on the DUAL SERIAL INTERFACE card are available to connect to a variety of terminals.

Initialization and the setting up of communication parameters are software controlled. The user can preselect these parameters and they will be taken into account during initialization.

Both ports have the hardware to act as a full duplex I/O port, but it is determined in the software whether a port will be configured for I/O or output-only.

3.4.6 SAMPLE CHANGERS

A number of optional cards or card sets can be used to control sample changers and/or a spinner. The possible combinations are listed below.

SAMPLE CHANGER SPINNER CONTROL (PW1713)	controls PW1775, PW1774 & shutter
SHUTTER SPINNER DRIVER (PW1713, PW1714)	controls PW1774 and shutter
CABLE CARD "SC" (PW1713)	connection to rear panel
PW1170 INTERFACE (PW1717)	controls the PW1170

Sample transport, spinning and shutter drive are under software control, either immediately by means of a command, or by a command stored in a programme.

3.4.7 OPTIONS RACK PW1749

This 19" electronics rack is identical to the PW1710 rack. It has the same motherboard, but different jumper settings. Connection to the PW1710 is such, that the XRA-bus is expanded completely. All supply voltages are connected to the Options Rack and the XRA-bus controller is informed that the Options Rack is connected.

3.4.8 SECOND STEPPING MOTOR DRIVE

A card set, similar to the one described in paragraph 3.4.4, but with different address settings, is used to drive a second stepping motor.

GONIOMETER CONTROL	a microcomputer based stepping motor control
STEPPING MOTOR SUPPLY DRIVER	a supply card with power stages for the motor
CABLE CARD "GON"	connection between motherboard and rear panel

The cards fit into the same slots of the options rack as the basic card set does in the PW1710.

The same functions are available for the second motor as for the first. All movements (slew and scan) are under software control, either immediately by means of a command, or by a command stored in a programme. In addition, the software can couple the two motors in a 2:1 ratio to perform $2\theta/\theta$ drive.

3.4.9 SECOND COUNTING CHANNEL

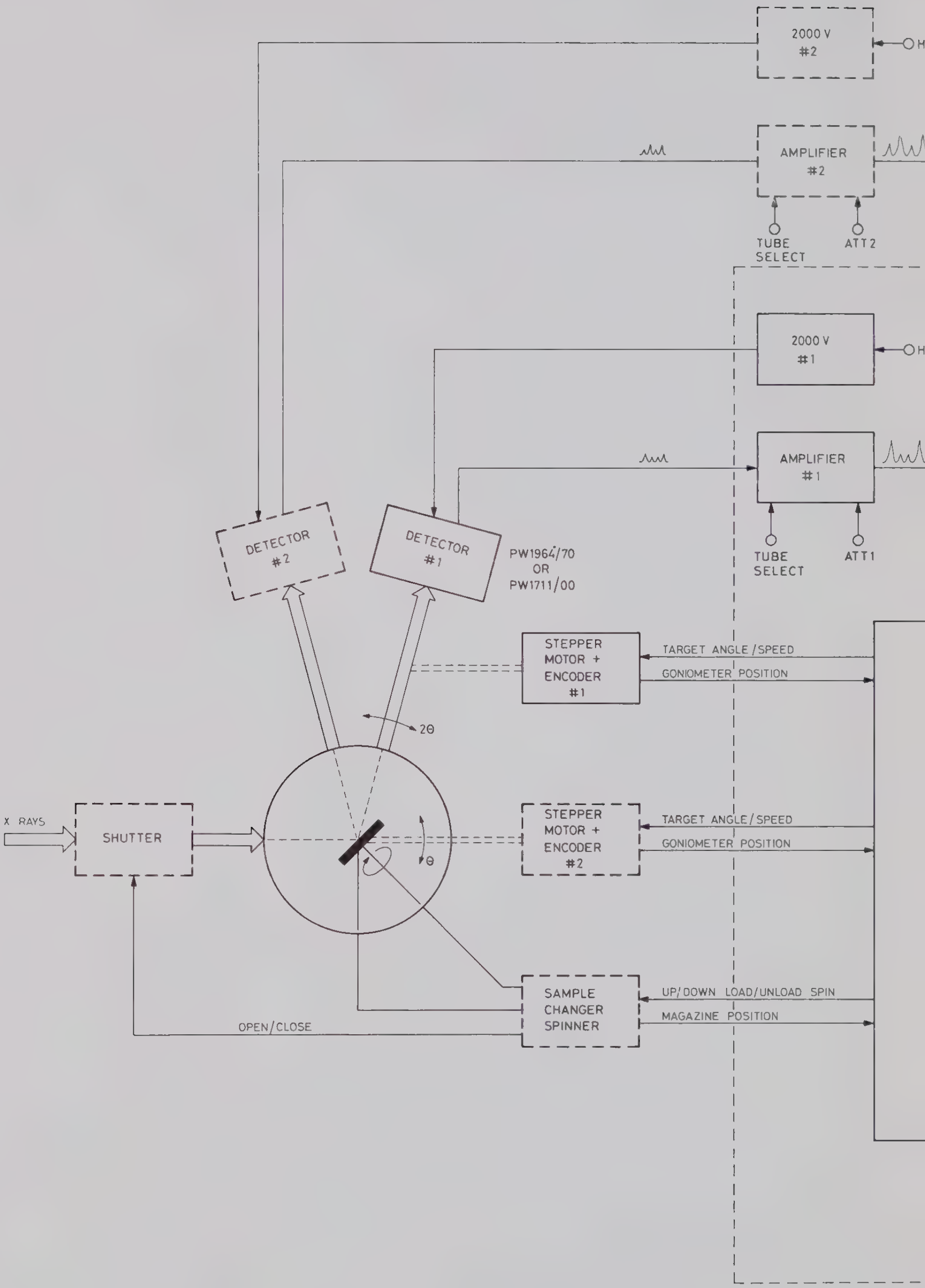
A card set, similar to the one described in paragraph 3.4.2, but with different module address settings and without THE RECORDER CONTROL card, is used to control a second counting channel.

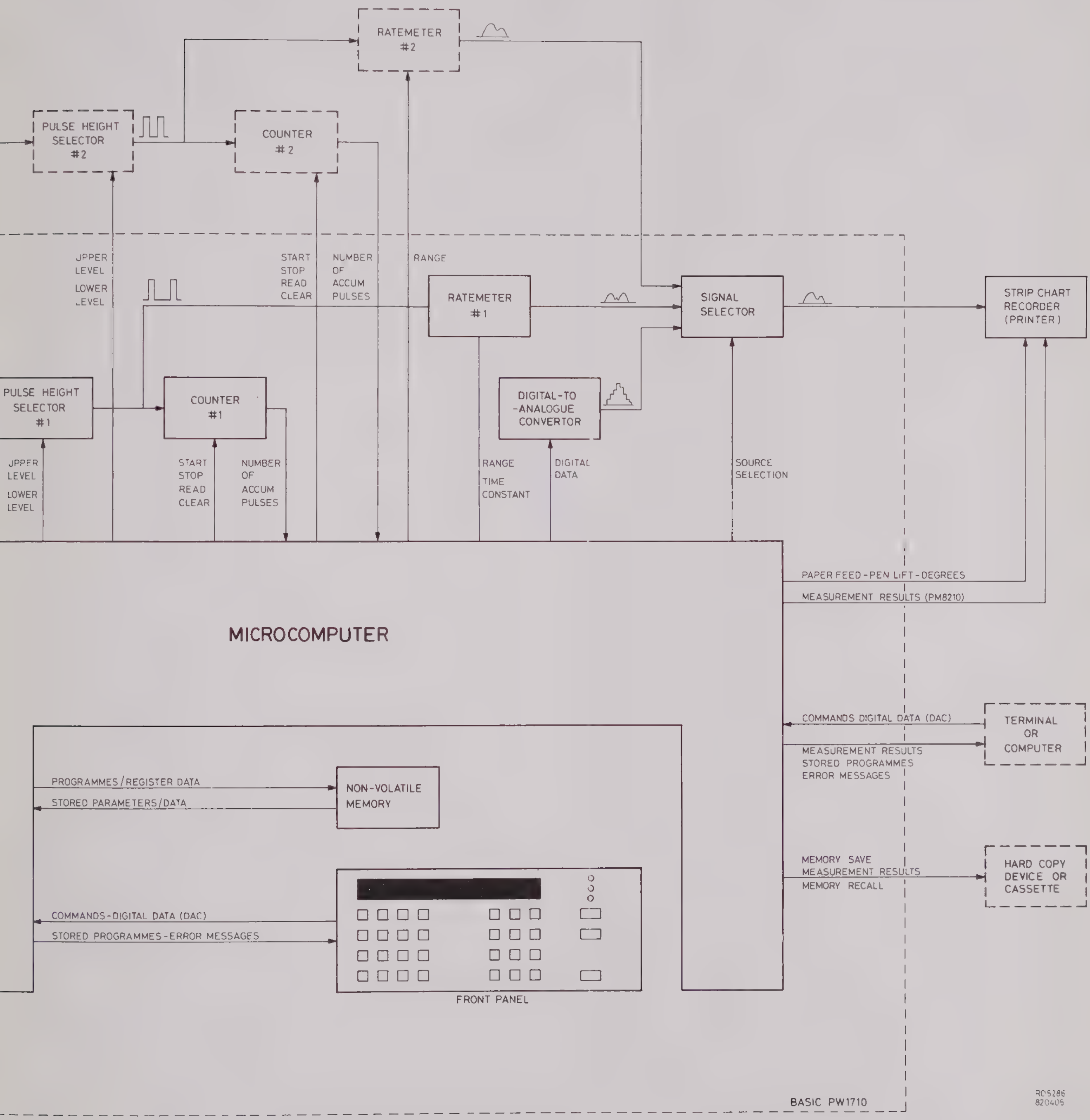
HIGH VOLTAGE 2000	a stabilized 2000V supply
AMPLIFIER ANALYZER	a pulse amplifier and discriminator
CABLE CARD "DET"	connection between motherboard and rear panel
SECONDARY CONTROL PANEL	a card, containing various settings
WINDOW CONTROL	a digital-to-analogue setpoint converter
RATEMETER	a pulse rate-to-analogue converter
FOUR DIGIT BINARY COUNTER	a prescaler function

The cards fit into the same slots of the options rack as the basic card set does in the PW1710.

The same functions are available for the second channel as were for the first channel, except for the time constant setting of the Ratemeter, which is wired to Autoranging with a minimum value of 0.5 s.

The two card sets share the one Recorder Control card. The selection of the detector signal, to be connected to the strip chart recorder, is done in software. Only when recording a Pulse Height Distribution Curve from the second detector, will Ratemeter number 2 be selected. All movements (slew and scan) are under software control, either immediately by means of a command, or by a command stored in a programme.


2000 V
#2
AMPLIFIER
#2
TUBE
SELECT
ATT 2
2000 V
#1
AMPLIFIER
#1
TUBE
SELECT
ATT 1
DETECTOR
#2
DETECTOR
#1
PW1964/70
OR
PW1711/00
STEPPER
MOTOR +
ENCODER
#1
TARGET ANGLE/SPEED
GONIOMETER POSITION
2Θ
X RAYS
SHUTTER
Θ
STEPPER
MOTOR +
ENCODER
#2
TARGET ANGLE/SPEED
GONIOMETER POSITION
SAMPLE
CHANGER
SPINNER
UP/DOWN LOAD/UNLOAD SPIN
MAGAZINE POSITION
OPEN/CLOSE


RATEMETER #2
PULSE HEIGHT SELECTOR #2
COUNTER #2
JPPER LEVEL
LOWER LEVEL
START STOP READ CLEAR
NUMBER OF ACCUM PULSES
RANGE
RATEMETER #1
SIGNAL SELECTOR
STRIP CHART RECORDER (PRINTER)
PULSE HEIGHT SELECTOR #1
COUNTER #1
DIGITAL-TO -ANALOGUE CONVERTOR
JPPER LEVEL
LOWER LEVEL
START STOP READ CLEAR
NUMBER OF ACCUM PULSES
RANGE
TIME CONSTANT
DIGITAL DATA
SOURCE SELECTION
PAPER FEED - PEN LIFT - DEGREES
MEASUREMENT RESULTS (PM8210)
MICROCOMPUTER
COMMANDS DIGITAL DATA (DAC)
TERMINAL OR COMPUTER
MEASUREMENT RESULTS
STORED PROGRAMMES
ERROR MESSAGES
PROGRAMMES / REGISTER DATA
STORED PARAMETERS / DATA
NON-VOLATILE MEMORY
MEMORY SAVE
MEASUREMENT RESULTS
MEMORY RECALL
HARD COPY DEVICE OR CASSETTE
COMMANDS - DIGITAL DATA (DAC)
STORED PROGRAMMES - ERROR MESSAGES
FRONT PANEL
BASIC PW1710
RD5286
820405

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4.1 INTRODUCTION

In all of the following card/module descriptions there are some methods of description and or layout which are used throughout this chapter, they are:

4.1.1 SCHEMATIC REFERENCES

The reference in square brackets is a reference to the location of that function on the schematic diagram. The schematic diagrams are all situated together with the card layouts at the rear of this chapter, they have been printed so that it is possible for you to fold the drawing out and look at it at the same time as the relevant text.

4.1.2 SOFTWARE BYTES

All of the software WRITE and READ bytes are laid out as follows:

(MSB)							(LSB)
BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

If more than one bit is used for a particular function, the left-most bit in the group of bits for that function is the Most Significant Bit (MSB) of that group.

4.1.3 CONNECTORS, WIRING AND SIGNAL NAMES

4.1.3.1 Connector Numbering

Most of the cards have a connector which fits into a connecting socket on the mother board, and some of them have additional connectors on their front panels. The connectors on the front panels are for connecting to cables to other parts of the system. The way that these connectors are numberred is as follows:

> On the cards themselves, the connectors are numberred XA, XB, XC and so on in sequence. If there is a connector to the mother board, it is always XA.
>
> In the system description, the overall wiring diagram, and any "system" references they are referred to as XxxA, XxxB or XxxC (the xx being replaced by the position number of the card on the mother board).

An example of this could be the CASHI signal on pin C19 of the motherboard connector on the Recorder Control Card in position 7:

> On the card this is referred to as XA-C19.
>
> On the system wiring it is referred to as X07A-C19.

4.1.3.2 System Wiring

The system wiring is shown in an over-all wiring diagram in Appendix A at the rear of this manual. The signal names and mnemonics used in that diagram and in all the descriptions contained in this chapter are shown in para 4.1.3.4.

4.1.3.3 Logic

If a signal is marked with a +, this indicates positive logic ---- The signal is active (true) when "high", and passive (false) when "low".

If a signal is marked with a -, this indicates negative logic ---- The signal is active when "low".

4.1.3.4 Signal Names/mnemonics

A*-	Microcomputer address bus bit * (* = 0 to 15)
AD*-	Microcomputer multiplexed addr/data bus bit * (* = 0 to 7)
ADBB*	* = 0 TO 3. Byte address buffered
ADMB*	* = 0 to 3. Module address buffered
ADRB*	Equipment byte address bus bit * (* = 0 to 3)
ADRM*	Equipment module address bus bit * (* = 0 to3)
ALE	Address latch enable
AMPOT	Amplifier out
ANGT3	2θ Angle greater than 3^{o}
ANLE3	2θ Angle less than or = 3^{o}
ANPOL	Analogue pen-on-line
ARDOC-	Arm decoupling or coupling
ATTOT	Attenuator output voltage
ATTRV	Attenuator reference voltage
ATTVR	Attenuation voltage reference
ATTVT	Attenuator output voltage
BLANK	Display blank
BUSYL	Busy line
CALIB	Calibrate switch
CALBR	Calibration
CASHI	Cassette position high
CASLS	Last cassette position for PW1170 (last sample)
CASMD	Cassette motor down
CASMU	Cassette motor up
CASPO	Cassette in position
CASRV	Cassette reference voltage
CASZR	Cassette zero position for PW1170
CLEAR	Clear Signal for equipment bus
CL	Clock
CLIN	Clock in
CLKOUT	Clock output
CLOCK	Clock.
CTSR	Clear to send data for recorder PM8210/31
CTS1	Clear to send data for Serial Interface 1
CTS2	Clear to send data for Serial Interface 2

DCDR	Data carrier detected for recorder PM8210/31
DCD1	Data carrier detected interface 1
DCD2	Data carrier detected interface 2
DDAT*	* = 1 to 4. Display data bit *
DEGMS	Degree marker signal
DEGRM	Degree marker
DESL*	* = 1, 2, and 4. Digit select
DETS1	Detector 1 selected
DIGS*	* = 1 or 2. Digital data bit selection
DISB*	* = 1, 2, 4, and 8. Display bit * (BCD)
DISPA	Display angle
DSIPR	Dual serial interface present
DSRR	Data set ready for recorder PM8210/31
DSR1	Data set ready for Serial Interface 1
DSR2	Data set ready for Serial Interface 2
DTR1	Data terminal ready from Serial Interface 1
DTR2	Data terminal ready from Serial Interface 2
DTRR	Data terminal ready for recorder PM8210/31
ECHO1	ECHO yes/no bit for Serial Interface 1
ECHO2	ECHO yes/no bit for Serial Interface 2
EOPAP	End of paper
EOPHD	End of pulse height distribution
ERROR	Error
FORWD	Paper forward
FRAME	Frame
GND	Ground
GND.MS	Ground micro switch
GND.SE	Ground for shaft encoder
GND.SEP	Ground for shaft encoder power
GND.SES	Ground for shaft encoder signal
GPIB*	General purpose input bit * (* = 0 to 3)
GPOB*	General purpose output bit * (* = 0 to 4)
GRBGO	Grab in goniometer position
GRBMA	Grab in magazine position
GRBPU	Grab motor command "pick-up" cycle
GRBRG	Grab rotation motor command "Rotate towards goniometer"
GRBRM	Grab rotation motor command "Rotate towards magazine"
GRBSD	Grab motor command "set-down" cycle
GRBSS	Grab in single sample position
GRBWC	Grab withdrawn, closed
GRBWO	Grab withdrawn, open
HLDA	Hold acknowledged
HOLD	Hold
HVOUT	High voltage output
HVREF	High voltage reference
HVSET	High voltage setpoint
INTA	Interrupt acknowledged
INTR	Interrupt request
INTR*	Interrupt request from device * (* = 2 to 5)
IO/M	I/O-Memory reference selector
IOBB*	* = 0 to 7. Buffered data bus bit *
IOBS*	* = 0 to 7. Data bus bit *
IOBU*	Equipment data bus bit * (* = 0 to 7)
IORED	Equipment bus read signal
IOWRT	Equipment bus write signal

LIFMD	Lift motor command "down"
LIFMU	Lift motor command "up"
LLREC	Lower level output to recorder
LOCAL	"local" (front panel) control mode in PM8203A
LOLIM	Lower limit switch in goniometer
LWLEV	Lower level voltage (= LOWLV)
MAGHI	Magazine position high
MAGMD	Magazine motor command "down"
MAGMU	Magazine motor command "up"
MAGPO	Magazine position bit 0 (magazine exactly in position)
MAGP*	* = 1 to 7. Magazine position bit in BCD (7=MSB)
MAG21	Magazine for 21 thick sample holders (switch selected)
MCOL*	* = A,B,C,D. Motor coil drive signal
MOTHV	Motor high voltage
MOTOR~	Motor ac supply
MOTOR	Motor dc supply -20 V
OPTPR	Options rack present
PENLU	Pen lift-up
PGND1	Power ground 1
PGND2	Power ground 2
PHDIV	Pulse height division (suppress pulse shift corr.)
PON	Power within two limits
RAD.SHIELDING	Radiation shielding safety switches
RAMSU	RAM supply voltage
RCPLS	Recorder paper transport pulse (=RECCH)
RD	Read signal from microcomputer
RDDIS	Read display
RDSW1	Read keybord switches
RDSW2	Read hardware status switches
READY	Handshake signal for data exchange
RECHI	"High" of signal to recorder
RECLO	"Low" of signal to recorder
RECOF	Recorder "off"
RECON	Recorder "on"
REMWW	Remote window
RESET	Reset input for microcomputer
RESOUT	Reset output from microcomputer
RIN1	Receiver in 1 (current loop)
RIN2	Receiver in 2 (current loop)
RMAUR	Ratemeter range manually selected: autoranging
RMFTA	Ratemeter range manually selected: factor bit A
RMFTB	Ratemeter range manually selected: factor bit B
RMPWC	Ratemeter range manually selected: power bit C
RMPWD	Ratemeter range manually selected: power bit D
RMPWE	Ratemeter range manually selected: power bit E
ROUT1	Receiver out 1 (current loop)
ROUT2	Receiver out 2 (current loop)
RRAUT	Ratemeter is autoranging
RRFTA	Ratemeter range factor bit A
RRFTB	Ratemeter range factor bit B
RRPWC	Ratemeter range power bit C
RRPWD	Ratemeter range power bit D
RST55	RST 5.5 (Interrupt vector)
RST65	RST 6.5 (Interrupt vector)
RST75	RST 7.5 (Interrupt vector)

RTCAU	Ratemeter time constant automatic
RTC*	* = .2 to 10. Ratemeter time constant
RTMHI	Ratemeter high
RTMH1	Ratemeter high 1
RTMH2	Ratemeter high 2
RTS1	Request to send from Serial Interface 1
RTS2	Request to send from Serial Interface 2
RxDR	Receiver data from recorder
RxD1	Receiver data 1
RxD2	Receiver data 2
S*	Cycle identification bit * (* = 0 or 1)
SAMCA	Sample in cassette
SAMGO	Sample in goniometer (measuring position)
SAMMA	Sample in actual magazine position
SAMML	Sample motor load
SAMMU	Sample motor unload
SCHPR	Sample changer present
SECHA	Shaft encoder channel A
SECHB	Shaft encoder channel B
SECHC	Shaft encoder channel C
SGND1	Signal ground 1
SGND2	Signal ground 2
SHIELDING	Radiation shielding for PW1771/00
SHUTC	Shutter is closed
SHUTE	Shutter is enabled to be opened
SHUTO	Shutter command "open"
SID	Serial input data
SLBUS	Select equipment bus
SLDT1	Select detector 1
SLDT2	Select detector 2
SLINT	Select interrupt circuitry
SLRA1	Select RAM 1
SLRA2	Select RAM 2
SLRAM	Select RAM
SLRO1	Select ROM 1
SLRO2	Select ROM 2
SLRO3	Select ROM 3
SLRO4	Select ROM 4
SOD	Serial output data
SPINH	Spinner motor high speed
SPINM	Spinner motor command (on/off)
SPNBY	Spinner motor busy
SRVON	Servo system on
TESTM	Sample changer in test mode
TIN1	Transmitter 1 input (current loop)
TIN2	transmitter 2 input (current loop)
TOUT1	Transmitter 1 output (current loop)
TOUT2	Transmitter 2 output (current loop)
TRAP	TRAP. Non-maskable interrupt (RST 4.5)
TUBOB	Tube selector output voltage buffered
TUBOT	Tube selector output voltage
TxDR	Transmit data to recorder
TxD1	Transmit data 1
TxD2	Transmit data 2

UPLEV	Upper level voltage (=UPPLV)
UPLIM	Upper limit switch in goniometer
V~f1	Filament voltage display
V~f2	Filament voltage display
WR	Write signal from microcomputer
WRDIS	Write display
WRLED	Write LEDs (busy, assembly, remote)
WWINF	Window infinite
WWOUT	Window output (output from discriminator)
+CL	Current loop voltage
-CL	Current loop voltage
+CLIN	Current loop input voltage
-CLIN	Current loop input voltage
30kHz	30 KiloHertz signal
10/30kHz	10 or 30 KiloHertz signal
0V	0 volt (ground)
0VPA	0 volt (ground) for pre-amplifier
0V (SH)	0 volt (ground) for shutter circuit
+5V	Logic +5 volt supply
+5VCTRL	Control signal for logic +5V supply
+5VIN	Coarse supply voltage for +5V
5VM~1	5 V a.c. for motor circuit (Terminal 1)
5VM~2	5 V a.c. for motor circuit (Terminal 2)
+5VSE	+5 V d.c. supply for shaft encoder
9V~1	9 V a.c. supply (Terminal 1)
9V~2	9 V a.c. supply (Terminal 2)
+12V	+12 volt supply
+12VIN	Coarse supply voltage for +12 V supply
-12V	-12 volt supply
-12VIN	Coarse supply voltage for -12 V supply
20VM~1	20 V a.c. for motor circuit (Terminal 1)
20VM~2	20 V a.c. for motor circuit (Terminal 2)
+24V	+24 volt supply
+24VIN	Coarse supply voltage for +24 V supply
+24VPA	+24 volt supply for pre-amplifier
40V~1	40 V a.c. supply (Terminal 1)
40V~2	40 V a.c. supply (Terminal 2)
42V SH	42 volt supply for shutter circuit
48V~1	48 V a.c. supply (Terminal 1)
48V~2	48 V a.c. supply (Terminal 2)
300V SH	300 volt supply for shutter circuit

4.2 SYSTEM CONTROL CARD + MEMORY EXTENSION

4.2.1 INTRODUCTION

The SYSTEM CONTROL CARD in conjunction with the MEMORY EXTENSION CARD controls the XRA-bus and thus the PW1710. Control is achieved by the use of control signals and the sending and receiving of data. The MEMORY EXTENSION card is plugged onto the SYSTEM CONTROL card´s CPU socket via a 40-pin adaptor. Without the MEMORY EXTENSION CARD the SYSTEM CONTROL CARD could function as stand-alone, provided the CPU is inserted in the CPU socket.

The following functions are provided by the System Control card together with the Memory Extension card:

* 6 MHz 8-bit 8085A CPU
* All locations memory mapped
* Sockets for ROM. See paragraph 4.2.1.1 following.
* Sockets for RAM. See paragraph 4.2.1.1 following.
* Wait states generator
* Power-up reset and power fail interrupt
* Programmable timer interrupt 2 to 300 Hz
* Battery backup for RAM for more than 500 hours @ 8kbytes
* 5 General purpose output bits
* 4 General purpose input bits
* 3 MHz interruptable clock
* 8 General purpose slide switches
* 4 General purpose programmable test pins
* Full XRA bus support:
    - 8 Address lines
    - 8 Bidirectional data lines
    - 4 Control lines
    - 4 Interrupt request lines
    - 1 Clock line 30kHz

The schematic diagrams and card layout diagrams for these cards are contained in figures 4.6 to 4.14.

4.2.1.1 Memory Versions

There are four possible combinations of the System Control card and the Memory Extension Card, as there are two versions of both cards. An "old" version and a "new" version. The combinations are as follows:

1. An "old" System Control Card and an "old" Memory Extension; this provides:

   2K of RAM (4 chips on SC)
   20K of ROM (4 chips on SC and 1 chip on ME)

2. A "new" System Control Card and an "old" Memory Extension; this provides:

   2K of RAM (1 chip on SC)
   20K of ROM (4 chips on SC and 1 chip on ME)

3. From DY744 onwards. A "new" System Control Card and an "old" Memory Extension; this provides:

   4K of RAM (1 chip on SC and 1 chip on ME)
   20K of ROM (4 chips on SC and 1 chip on ME)

4. A "new" System Control Card and an "new" Memory Extension; this provides:

   4K of RAM (1 chip on SC and 1 chip on ME)
   20K of ROM (4 chips on SC and 1 chip on ME)

   This provides the same as combination 3, the difference is physical:

   The ROM sockets are larger (suitable for 8K ROMs)
   There are switches to allow for 4K or 8K ROM.

4.2.2 MEMORY MAP

All data can be transferred from and to the CPU by means of MEMORY WRITE and MEMORY READ cycles; all locations are memory mapped and I/O instructions are not used. ICs D14 on the SYSTEM CONTROL CARD and D5 on the MEMORY EXTENSION CARD decode the most important address bits A15, A14, A13, A12 and (where applicable) A11 into dedicated selection lines. Table 4.1 gives the address with the corresponding selection line.

Table 4.1 Address to Selection line Decoding

ADDRESS IN HEXADECIMAL CODE	SEL.LINE	AREA
ROM type 2732 (2764)		
0000H - 0FFFH	SLROM1	Programme memory
1000H - 1FFFH	SLROM2	Programme memory
2000H - 2FFFH	SLROM3	Programme memory
3000H - 3FFFH	SLROM4	Programme memory
4000H - 4FFFH (4000H - 5FFFH)	SLROM5	Programme memory
5000H - 5FFFH (6000H - 7FFFH)	SLROM6	Programme memory
7000H (F000H)	TEST	Test switches + pins
8000H - 87FFH	SLRAM0	Data memory
8800H - 8FFFH	SLRAM1	Data memory
9000H - 97FFH	SLRAM2	Data memory
9800H - 9FFFH	SLRAM3	Data memory
C800H	SLOUT	Output
D000H	SLINT	Input + Interrupts
D800H - D8FFH	SLBUS	XRA bus
E000H	SLTIM	Timer interrupt

4.2.3 THE CPU

The CPU is a single chip microprocessor with:

- 16 address lines
- 8 bi-directional data lines
- 7 data exchange control lines
- 6 interrupt control lines
- 2 direct memory access control lines

The lower 8 address lines and the data lines share the same pins and are time-multiplexed.

An INPUT machine cycle (1 wait state via wait state generator) is:

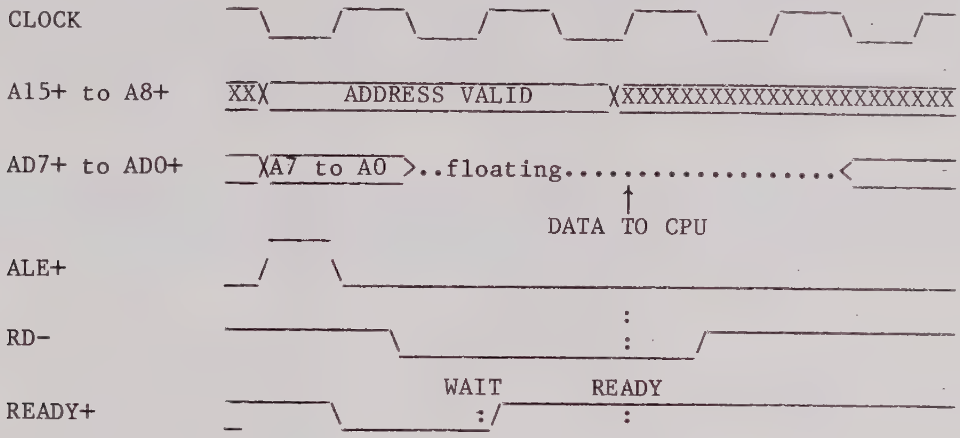

CLOCK
A15+ to A8+
XX
ADDRESS VALID
XXXXXXXXXXXXXXXXXXXXXXXX
AD7+ to AD0+
A7 to A0
..floating...................
DATA TO CPU
ALE+
RD-
WAIT
READY
READY+

Figure 4.1 Input machine Cycle

An OUTPUT machine cycle (1 wait state via wait state generator) is:

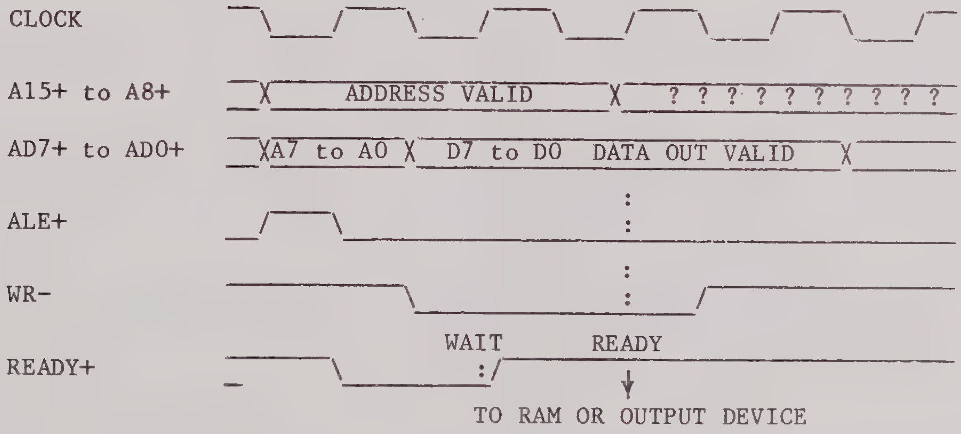

CLOCK
A15+ to A8+
ADDRESS VALID
? ? ? ? ? ? ? ? ? ?
AD7+ to AD0+
A7 to A0
D7 to D0 DATA OUT VALID
ALE+
WR-
WAIT
READY
READY+
TO RAM OR OUTPUT DEVICE

Figure 4.2 Output Machine Cycle

ICs D10 and D11 buffer the address bits (ALE is the latching signal) to demultiplex the address bus and to provide a proper address, even during undefined cycles.

The processor speed is derived from a 6MHz crystal, resulting in a 3 MHz internal clock frequency with a cycle time of 320 ns.

For more details refer to the 8085A User´s Manual from INTEL or AMD.

4.2.4 RESET

The circuitry around transistor V5 [F1 B-2] ensures a proper power-up and power-down behaviour of the card. At power-up (or after a manual RESET) the signal TRAP is immediately pulled low. Between RESET going low and RESIN going high there must be a time delay of at least 1 ms to ensure proper functioning of the internal clock and internal bias generator of the processor.

At power-down TRAP goes high immediately, causing a non-maskable interrupt (RST4.5) to the processor. After a delay of at least 300 μs RESIN goes low. During this delay an interrupt service routine can save valuable information in RAM, send a message to the display and put the processor in the HALT mode in order to avoid unwanted RAM access.

4.2.5 DATA RETENTION

Data retention in RAM is achieved by the use of a rechargeable NiCd battery.

During power-on, the RAM [F1 G,K-8] is supplied via transistor V3 [F2 J-4]. The maximum allowable voltage drop across V3 is 300 mV, otherwise for the RAM during operation the Vcc will be out of specification.

When the +5V drops, at about +3V, transistors V4 and V3 will switch off and supply of the RAM is taken over by the battery.

For ultra-low power consumption of the RAM in standby state, the address pins must have well defined levels, either HIGH or LOW, this is achieved as follows:

OE (RD) and WE (WR) are pulled LOW by resistors R12 and R13.

CE lines are pulled HIGH by D26, which is powered by the same battery.

D26´s input is pulled LOW by Low Power Schottky ICs which in the standby mode show a low-ohmic path to ground.

While power is on, the battery is charged via resistor R17 which determines the charge current. The charge current is about 7 mA, this level is permissable continuously. Charging time is about 20 hours.

4.2.6 TEST

The SID (serial input) line is connected to a switch on the printed circuit board´s text plate. The CPU can read it with the instruction RIM.

The SOD (serial output) line is connected to a LED on the printed circuit board´s text plate. The CPU can write to it with the instruction SIM.

Both elements can be used for test purposes with very few hardware overheads.

READ "IM" (RIM): test switch + interrupt status

1=TEST	INT7.5 FF	INT6.5	INT5.5	INT ENABLE	MASK7.5	MASK6.5	MASK5.5

WRITE "IM" (SIM): test LED + interrupt masks

TESTLED 1 = ON	TESTLED 1=ENABL	X	INT7.5F 1=RESET	MASKSET 1=ENABL	MASK7.5 1=MASK	MASK6.5 1=MASK	MASK5.5 1=MASK

4.2.7 WAIT STATES

Normally the 6 MHz CPU can run at full speed with a maximum memory access time of less than 450 ns. To allow slower memories to be connected, one wait state (1 cycle = 320 ns) is added to each memory access cycle, resulting in a maximum permissable access time of 770 ns.

D5 [F1 E-2] forms the single wait state generator. READY+ is normally HIGH because the 3 MHz continuously clocks "0"s into the flip-flop. For every machine cycle, the ALE+ signal clocks a "1" into the flip-flop which drives READY+ LOW for 320 ns. During this 320 ns the processor samples the READY line and inserts one wait state.

Additional wait states can be added if necessary by pulling D5-4 LOW. During XRA data transfers at least 8 wait states are required, these are generated by D18 [H-4] and D19 [H-2] (3 MHz is divided by 2 and by 4). More than 8 wait states are possible by pulling the XRA bus READY pin (C12) LOW; now the wait situation can be extended as long as required.

Switching C12 can be done asynchronously, D5 will re-synchronize READY to the processor clock.

4.2.8 ROM

The card combination provides 6 sockets for ROMs, PROMs or EPROMs.

The four 24-pin sockets on the SYSTEM CONTROL card accomodate 4K x 8 ROMs of for instance the 2732 type. Two-line control avoids possible bus contention; only when both CE and OE of a ROM are TRUE will the data output buffers become active.

A typical READ cycle of a ROM is:

```
A11/12+ to A0+  XXXX    ADDRESS VALID            XXXXXXXXXXXXXXXXXXXXX
                   <-address access time->
                                         :
                ______                                 ___________________
CE-                   \__________________:________/
                     <--CE access time--->
                                         :
                _________                              ___________________
OE-                      \_______________:________/
                        <--OE acc.time--->
                                         :
AD7+ to AD0+    .......(floating)........< OUTPUT DATA VALID    >....
```

Figure 4.3 ROM Read Cycle

The two 28-pin ROM sockets of the MEMORY EXTENSION card can accomodate either 4K x 8 ROMs (2732) or 8K x 8 ROMs (2764), selected by a switch marked 4K/8K. When 2732s are used, they have to be inserted in such a way that the two busses per row at the left hand side are left free (observe the 4/8 mark).

4.2.9 RAM

As described in paragraph 4.2.8, four sockets are provided on the card combination to fit 2K x 8 CMOS RAMs of the 6116 type. Use of the 6116 type ensures ultra-low stand-by power consumption. RAM on the MEMORY EXTENSION card is powered by a separate flexible connection (RAMSU+) to allow the two boards to be taken apart for repair activities without losing memory contents.

Reading from RAM is performed in the same way as it is from ROM (two line control OE and CE). A typical READ cycle is:

```
A10+ to A0+     XXXX     ADDRESS VALID          XXXXXXXXXXXXXXXXXXXXX
                   <-address access time->
                                          :
CE-             ______                    :                ____________
                      \___________________:_______________/
                      <--CE access time--->
                                          :
OE-             __________                                 ____________
                          \_______________:_______________/
                          <--OE acc.time--->

WE-             ___________________________________________________________
                                          :
                                          :
AD7+ to AD0+    .......(floating)........<  OUTPUT DATA VALID  >....
```

Figure 4.4 RAM Read Cycle

Writing to RAM is done similarly to reading, except that WE- is used instead of OE-. A typical WRITE cycle is:

```
A10+ to A0+     XXXX     ADDRESS VALID          XXXXXXXXXXXXXXXXXXXXX
                   <-address access time->
                                          :
CE-             ______                    :                ____________
                      \___________________:_______________/
                      <--CE access time--->

OE-             ___________________________________________________________
                                          :
                                          :
WE-             __________                                 ____________
                          \_______________:_______________/
                          <--WE acc.time--->
                                          :
AD7+ to AD0+    .......(floating)........:...........................
                                          ↑
                                     DATA TO RAM
```

Figure 4.5 RAM Write Cycle

4.2.10 INTERRUPTS

The CPU has 5 interrupt inputs:

TRAP
RST5.5
RST6.5
RST7.5
INTR (not used)

* TRAP is a non-maskeable interrupt (DI and EI cannot disable or enable its acknowledgement). A high level (or even a pulse) on this input causes the processor to suspend the normal programme flow, and to call an interrupt service routine starting at address 24H.

* RST5.5 is a maskable interrupt. The instruction EI and DI and SIM (set interrupt mask) enable or disable it. RST5.5 goes high when any card on the XRA bus is requesting service. It is an OR-function of XRA bus interrupt requests INTR5 to INTR2, which are latched in D31. The processor can determine which device requested service by reading the pending interrupt requests buffer D32, bits AD3 to AD0 (SLINT) (refer to parallel input). The interrupt service routine must contain instructions to reset the appropriate interrupt bit of D31 via D30 (SLINT).

WRITE BYTE D000H: reset bus interrupt requests

X	X	X	X	1=RESET INTR5	1=RESET INTR4	1=RESET INTR3	1=RESET INTR2

A high level on RST5.5 causes the processor to suspend normal programme flow, and to call an interrupt service routine starting at address 2CH.

* RST6.5 is a maskable interrupt. The instruction EI and DI and SIM (set interrupt mask) enable or disable it. It goes high when pin C22 (normally connected to the common interrupt of the DUAL SERIAL INTERFACE CARD) goes high. A high on RST6.5 causes the processor to suspend normal programme flow, and to call an interrupt service routine starting at address 34H. In this routine the processor has to check with the DUAL SERIAL INTERFACE CARD to determine the device which requested service. Measures should be taken to reset the interrupt request (for instance, by reading the input character, or disabling the transmitter).

* RST7.5 is a maskable interrupt, connected to the programmable timer. The instruction EI and DI and SIM (set interrupt mask) enable or disable it. A pulse on RST7.5 causes the processor to suspend the normal programme flow, and to call an interrupt service routine starting at address 3CH.

4.2.11 PROGRAMMABLE TIMER INTERRUPT

ICs D15, D16 and D17 [F2 F,K-10,11] form a programmable frequency source. D19 [F1 D-5] provides 30 kHz, which is divided by a number between 2 and 15 in the divide-by-n D15. Additional division is performed in D17. Part of the divider is contained in bits AD3 to AD1 when clocked into D16. The remaining bit AD0 selects inside D17 a divider of either 100 or 1000, resulting in a large number of possible dividers.

Useful dividers, the appropriate frequencies and the selection codes are given in table 4.2 below:

Table 4.2 Timer Interrupt Frequencies and Dividers

AD3	AD2	AD1	AD0	RST7.5 f_{int}(Hz)	divider
1	1	1	0	2	15000
0	0	1	0	3	10000
0	1	0	0	5	6000
1	0	0	0	10	3000
0	0	0	0	15	2000
1	1	1	1	20	1500
0	0	1	1	30	1000
0	1	0	1	50	600
1	0	0	1	100	300
0	0	0	1	150	200

WRITE BYTE E000H: timer interrupt frequency

X	X	X	X	BIT 3	BIT 2	BIT 1	BIT 0

4.2.12 PARALLEL INPUTS

Four input are provided, They are:

SPNBY - Spinner motor busy
OPTPR - Options rack present
SCHPR - Sample changer present
DSIPR - Dual Serial Interface present

The inputs are converted into 5V logic by D40 and are connected to D32 bits AD7 to AD4 (SLINT).

READ BYTE D000H: input + bus-interrupt requests

SPNBY 1=PRESNT	OPTPR 0=PRESNT	SCHPR 1=PRESNT	DSIPR 1=PRESNT	INTR5 1 = ON	INTR4 1 = ON	INTR3 1 = ON	INTR2 1 = ON

4.2.13 PARALLEL OUTPUTS

Output bits are written to D33 during a SLOUT cycle:

Bit AD5 is used to gate the 4MHz. output clock.

Bits 4 + 3 are not used.

Bits 2 to 0 are buffered by D41, a "1" results in a conducting open collector transistor in D41, capable of sinking 40 mA at maximum 30V. They are output with the following signal names:

AD2 - SPINM - Spinner motor command On/Off.
AD1 - SLDT2 - Select Detector 2
AD0 - SLDT1 - Select Detector 1

WRITE BYTE C800H: parallel output

X	X	3MHz 1 = ON	GPOB4 1 = ON	GPOB3 1 = ON	SPINM 0 = ON	SLDT2 1 = ON	SLDT1 1 = ON

4.2.14 SLIDE SWITCHES

Eight slide switches are provided on the MEMORY EXTENSION CARD. The CPU can read these switches (TEST) via data buffer D4. The address of TEST is dependent on the type of ROM selected (switch 4K/8K).

READ BYTE 7000H: (slide switches)

SW 7	SW 6	SW 5	SW 4	SW 3	SW 2	SW 1	SW 0

4.2.15 TEST PINS

Four programmable test pins TPIN5 to TPIN2 are provided on the MEMORY EXTENSION CARD, connected to the addressable latch. Each pin has its own address and can accept levels contained in data bit AD0 (TEST). The address of TEST is dependent on the type of ROM selected (4K/8K switch).

WRITE BYTE 7000H: (addressable latch; bit 0)

X	X	X	X	X	X	X	TPIN2+

WRITE BYTE 7001H: (addressable latch; bit 1)

X	X	X	X	X	X	X	TPIN3+

WRITE BYTE 7002H: (addressable latch; bit 2)

X	X	X	X	X	X	X	TPIN4+

WRITE BYTE 7003H: (addressable latch; bit 3)

X	X	X	X	X	X	X	TPIN5+

4.2.16 XRA BUS

This bus is a subset of the demultiplexed 8085A CPU bus. The differences are:

- The logic swing (12V in place of 5V)
- The type of logic (negative logic for address bus)
- Address bus width (8 instead of 16 lines)
- The number of wait states to be inserted (8 instead of 1).

When the bus is not being accessed, the outputs of the 5V-to-12V level converters D34, D35, D36 and D37 are tri-stated; D29 is also tri-stated. Data lines are pulled LOW and address lines are pulled HIGH by resistor networks, resulting in an address zero (negative logic), which will not activate any card on the bus.

During a bus WRITE cycle the signal SLBUS (select bus) enables D36 and D37 to drive the address bus. SLBUS and S1+ (advanced bus control signal, LOW for write) together activate D34 and D35 to put data onto the data bus. IOWRT (bus write) controls the data transfer.

During a bus READ cycle SLBUS enables D36 [Fl H-13] and D37 [Fl J-13] to drive the address bus. S1+ is HIGH during read, so D34 and D35 remain floating. IORED enables the addressed module to put data onto the bus. This data is converted from 12V into 5V by D27 and D28 [Fl C,D-14], and the signal RD from D23 [Fl F-12] causes D29 to route this data to the CPU.

Interrupt lines are converted to 5V by D39. Only a pulse of >0.5 us is required to set the appropriate set/reset flip-flop in D31. Refer to interrupt.

A master clear signal (CLEAR-) is provided, derived from the RESOUT pin of the CPU. During power-up or manual RESET, CLEAR is active (=LOW).

A 30 kHz square wave signal is available. For timing diagrams refer to "CPU".

READ/WRITE BYTE D8mbH: bus data (m = module address, b = byte address)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

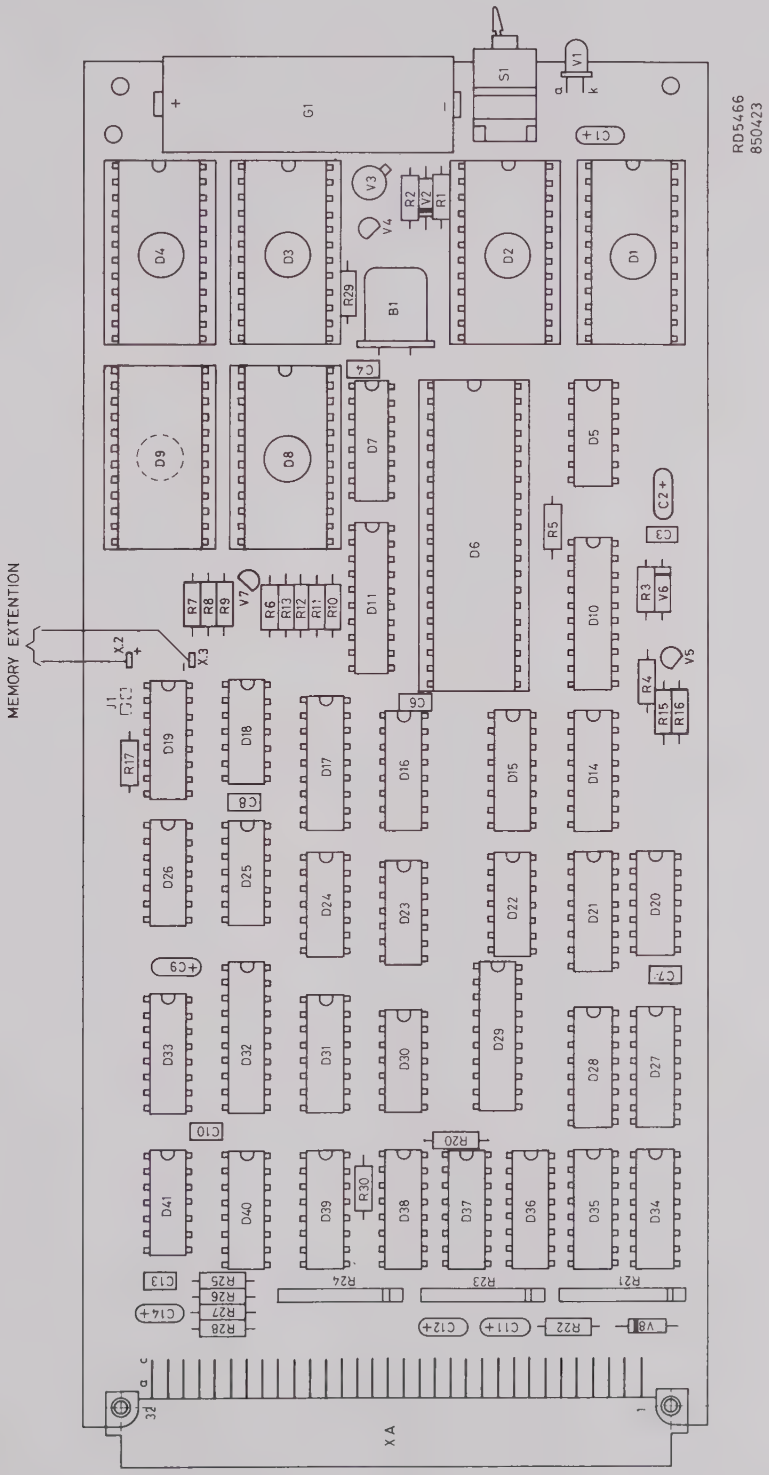
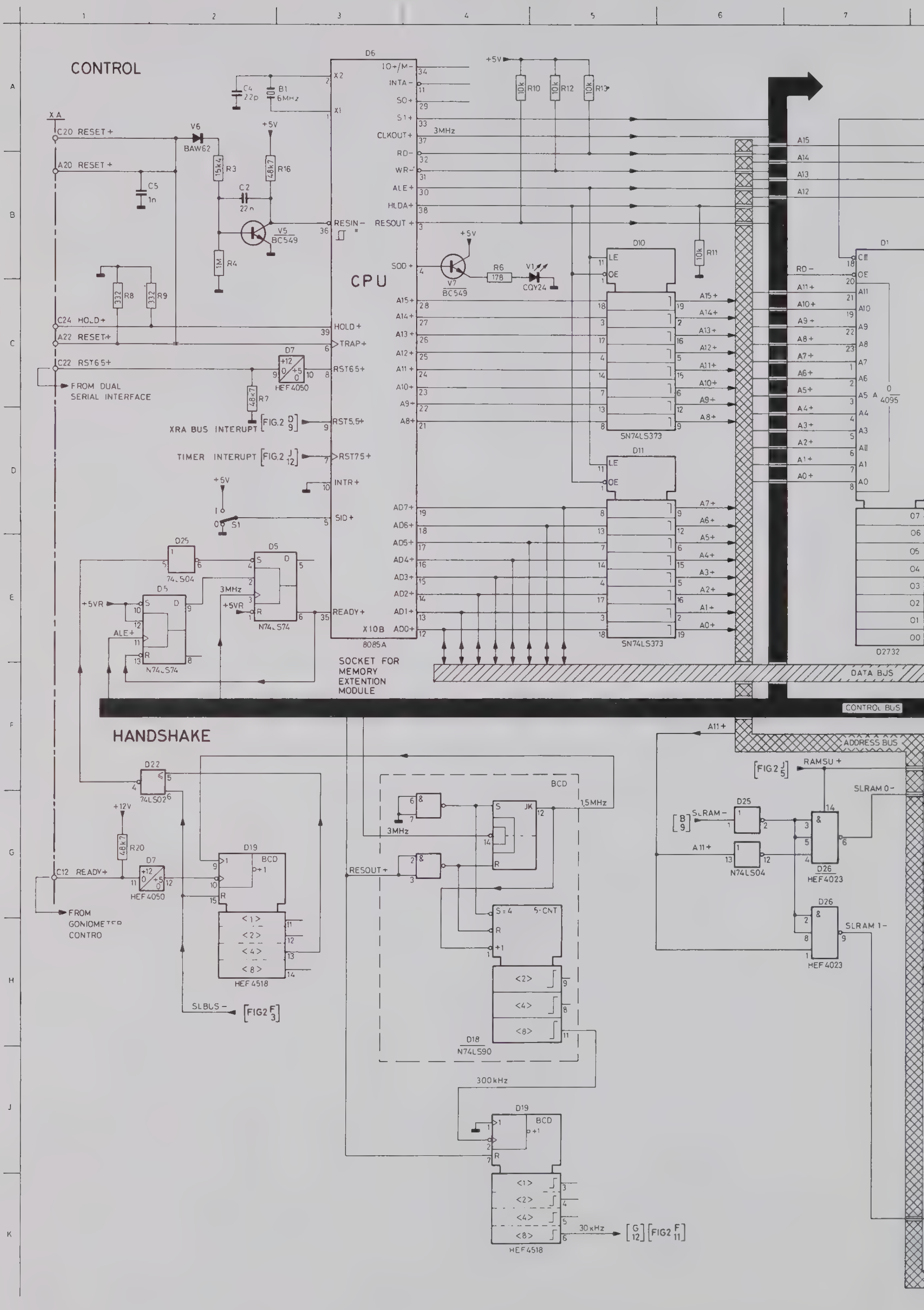

RD5466
850423
MEMORY EXTENTION
G1
S1
V1
a
k
C1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
B1
V2
V3
V4
V5
V6
V7
V8
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R15
R16
R17
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
C2
C3
C4
C6
C7
C8
C9
C10
C11
C12
C13
C14
X2
X3
J1
XA
32
1
a
c

Figure 4.6 System Control Card, Layout


CONTROL
CPU
D6
8085A
X10B
IO+/M-
INTA-
SO+
S1+
CLKOUT+
3MHz
RD-
WR-
ALE+
HLDA+
RESOUT+
RESIN-
X1
X2
C4 22p
B1 6MHz
SOD+
V7 BC549
R6 178
V1 CQY24
+5V
R10 10k
R12 10k
R13 10k
R11 10k
XA
C20 RESET+
A20 RESET+
C5 1n
V6 BAW62
R3 15k4
R16 48k7
C2 22n
V5 BC549
R4 1M
R8 332
R9 332
C24 HOLD+
A22 RESET+
C22 RST65+
FROM DUAL SERIAL INTERFACE
HOLD+
TRAP+
RST6.5+
D7 HEF4050
R7 48k7
XRA BUS INTERUPT [FIG.2 D 9]
RST5.5+
TIMER INTERUPT [FIG.2 J 12]
RST7.5+
INTR+
SID+
S1
A15+ A14+ A13+ A12+ A11+ A10+ A9+ A8+
AD7+ AD6+ AD5+ AD4+ AD3+ AD2+ AD1+ AD0+
READY+
D25 74LS04
D5 N74LS74
+5VR
ALE+
SOCKET FOR MEMORY EXTENTION MODULE
D10 SN74LS373
D11 SN74LS373
LE
OE
A15 A14 A13 A12
A7+ A6+ A5+ A4+ A3+ A2+ A1+ A0+
D1 D2732
0 4095
CE
RD-
O7 O6 O5 O4 O3 O2 O1 O0
DATA BUS
CONTROL BUS
ADDRESS BUS
HANDSHAKE
D22 74LS02
+12V
R20 48k7
C12 READY+
D7 HEF4050
FROM GONIOMETER CONTRO
D19 BCD HEF4518
<1> <2> <4> <8>
SLBUS- [FIG2 F 3]
BCD
3MHz
1,5MHz
RESOUT+
JK
S=4 5-CNT
D18 N74LS90
300kHz
D19 BCD HEF4518
30kHz [G 12] [FIG2 F 11]
A11+
[FIG2 J 5] RAMSU+
SLRAM 0-
[B 9] SLRAM-
D25 N74LS04
A11+
D26 HEF4023
SLRAM 1-

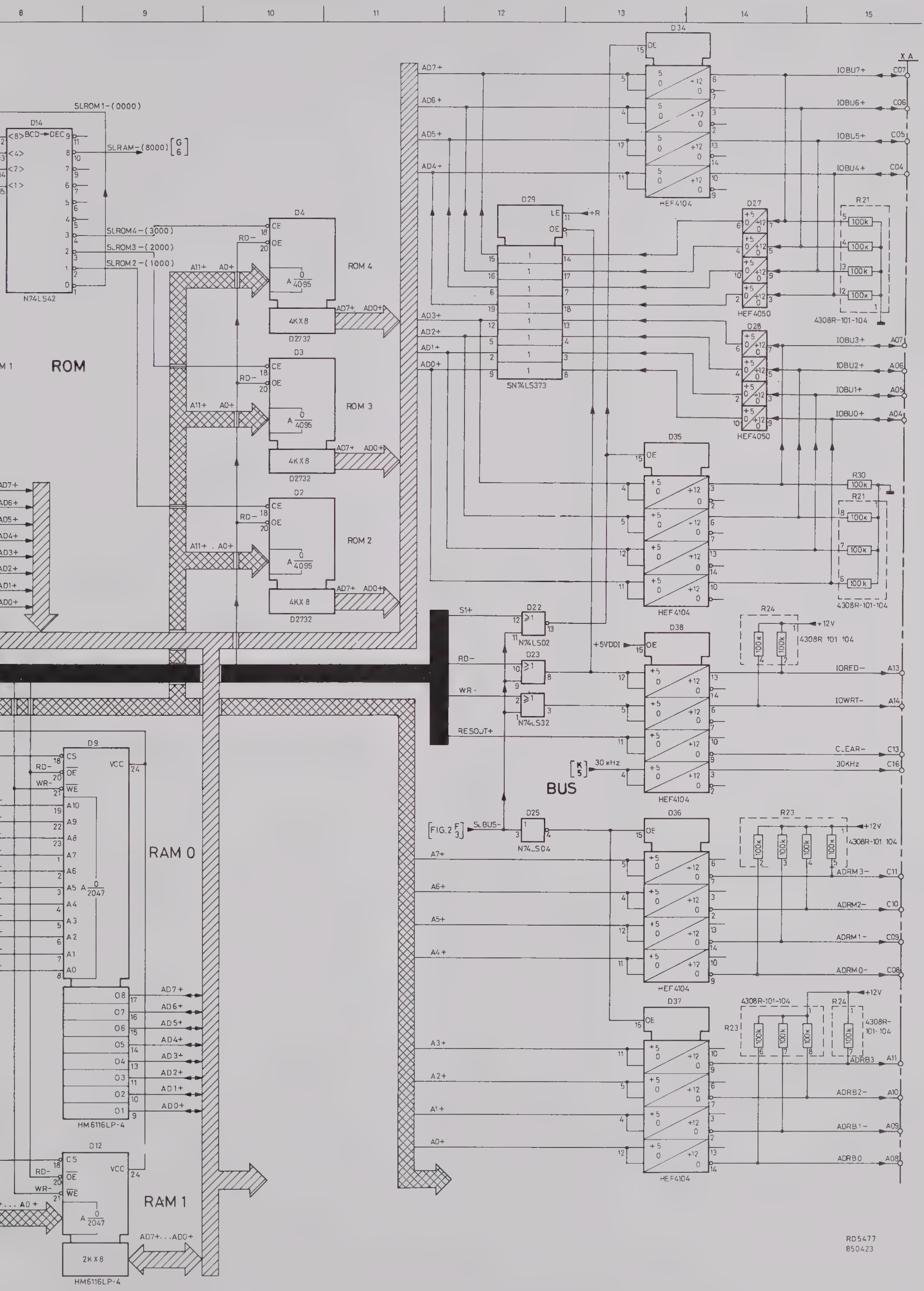

8
9
10
11
12
13
14
15
D34
OE
HEF4104
X A
IOBU7+
IOBU6+
IOBU5+
IOBU4+
C07
C06
C05
C04
AD7+
AD6+
AD5+
AD4+
SLROM1-(0000)
D14
BCD→DEC
N74LS42
SLRAM-(8000) [G 6]
SLROM4-(3000)
SLROM3-(2000)
SLROM2-(1000)
D4
CE
OE
RD-
A11+ A0+
ROM 4
4KX8
D2732
AD7+ AD0+
D29
LE
OE
+R
SN74LS373
D27
HEF4050
R21
100k
4308R-101-104
AD3+
AD2+
AD1+
AD0+
D28
IOBU3+
IOBU2+
IOBU1+
IOBU0+
A07
A06
A05
A04
ROM
D3
ROM 3
D2
ROM 2
A 0/4095
D35
HEF4104
R30
4308R-101-104
S1+
RD-
WR-
RESOUT+
D22
N74LS02
D23
N74LS32
+5VDDI
D38
R24
+12V
4308R 101 104
IORED-
IOWRT-
CLEAR-
30KHz
A13
A14
C13
C16
[K 5] 30 kHz
BUS
[FIG.2 F 3]
SLBUS-
D25
N74LS04
D36
R23
4308R-101 104
A7+
A6+
A5+
A4+
ADRM3-
ADRM2-
ADRM1-
ADRM0-
C11
C10
C09
C08
D37
A3+
A2+
A1+
A0+
ADRB3
ADRB2-
ADRB1-
ADRB0
A11
A10
A09
A08
D9
CS
OE
WE
VCC
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
A 0/2047
RAM 0
O8
O7
O6
O5
O4
O3
O2
O1
HM6116LP-4
D12
RAM 1
2KX8
AD7+...AD0+
... A0+
RD5477
850423

Figure 4.7 System Control Card (new version), Schematic Figure 1

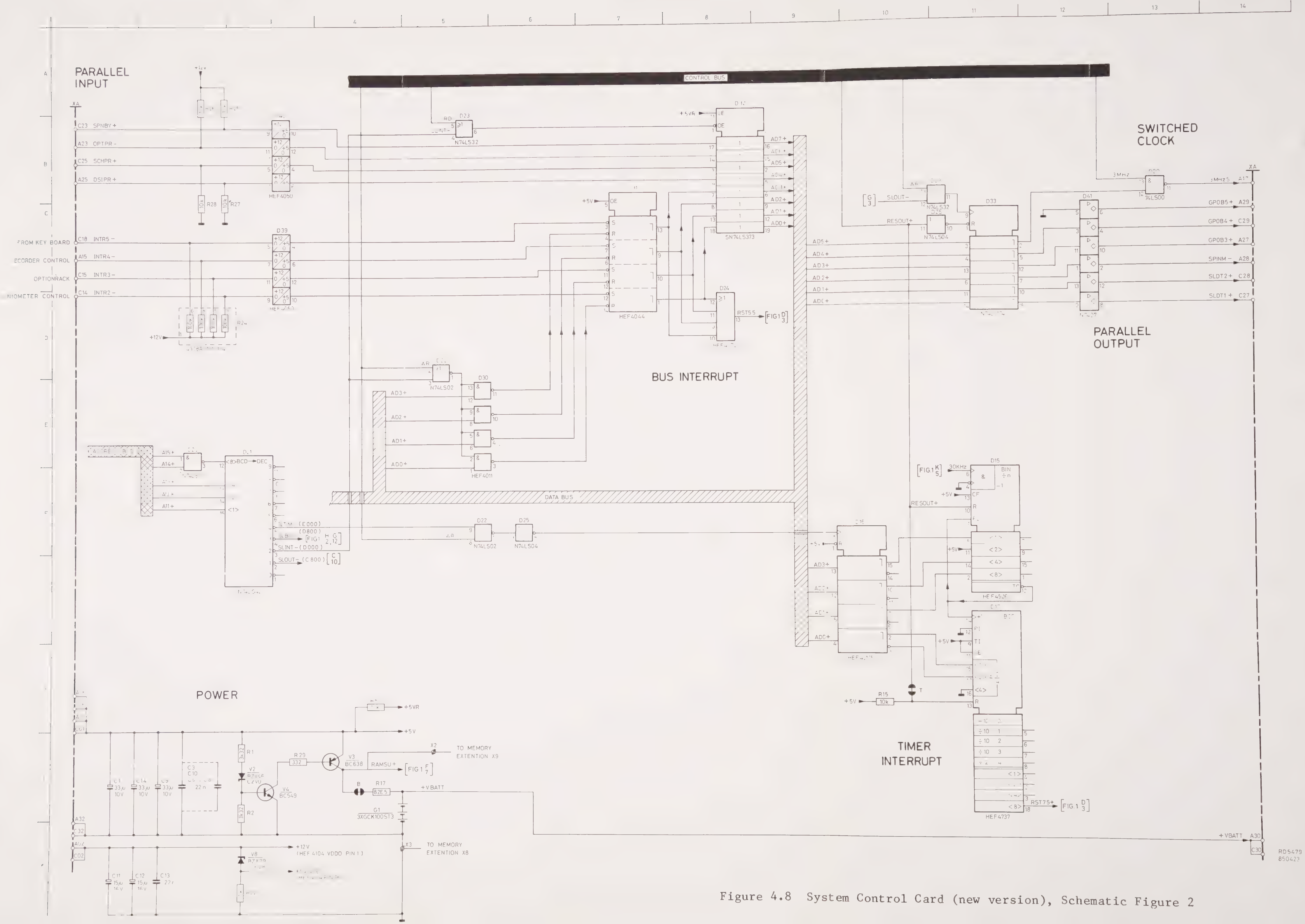

PARALLEL INPUT
CONTROL BUS
SWITCHED CLOCK
BUS INTERRUPT
PARALLEL OUTPUT
DATA BUS
POWER
TIMER INTERRUPT
C23 SPNBY+
A23 OPTPR-
C25 SCHPR+
A25 DSIPR+
HEF4050
R28
R27
FROM KEY BOARD
ECORDER CONTROL
OPTIONRACK
NIOMETER CONTROL
C18 INTR5-
A15 INTR4-
C15 INTR3-
C14 INTR2-
D39
+12V
N74LS32
SN74LS373
HEF4044
D24
RST5.5
FIG1
N74LS02
D30
AD3+
AD2+
AD1+
AD0+
HEF4011
D22
D25
N74LS04
D1
BCD DEC
(E000)
(D800)
SLINT-(D000)
SLOUT-(C800)
AD7+
AD6+
AD5+
AD4+
AD3+
AD2+
AD1+
AD0+
3MHz
D50
74LS00
3MHzS A17
SLOUT-
RESOUT+
N74LS32
N74LS04
D33
D41
GPOB5+ A29
GPOB4+ C29
GPOB3+ A27
SPINM- A28
SLOT2+ C28
SLOT1+ C27
XA
D15
30KHz
BIN
+5V
RESOUT+
HEF4520
HEF4737
R15
10k
RST7.5+
+VBATT A30
C30
+5VR
+5V
R1
R2
R29
V2
V3
BC638
V4
BC549
RAMSU+
TO MEMORY EXTENTION X9
R17
+VBATT
G1
3XGCK100ST3
A32
C32
+12V
TO MEMORY EXTENTION X8
V8
C1
C14
C9
C11
C12
C13
RD5479
850423

Figure 4.8 System Control Card (new version), Schematic Figure 2

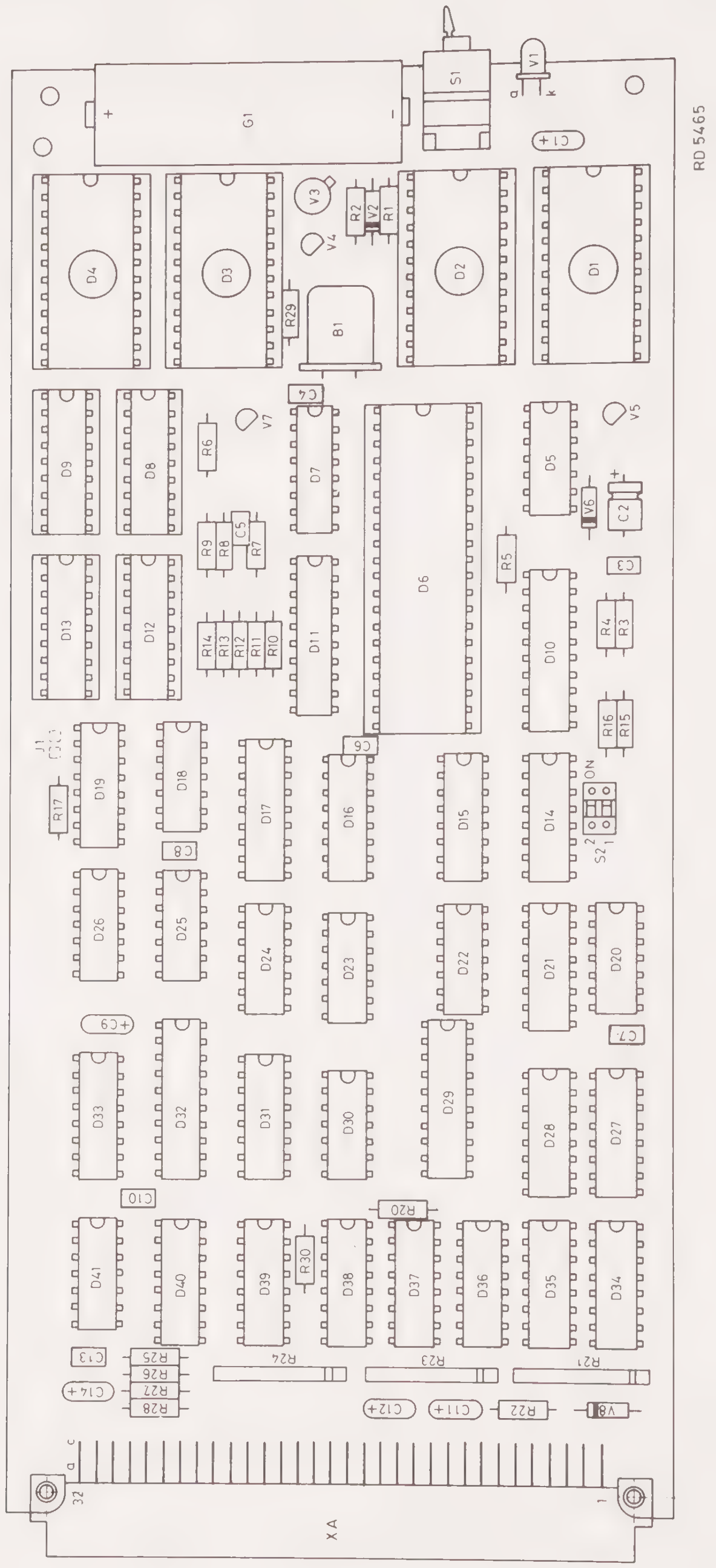

RD 5465
G1
S1
V1
C1
D1
D2
D3
D4
B1
R29
C4
V7
V5
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
D27
D28
D29
D30
D31
D32
D33
D34
D35
D36
D37
D38
D39
D40
D41
S2
ON
XA
32
1

Figure 4.9 System Control Card (old version), Layout

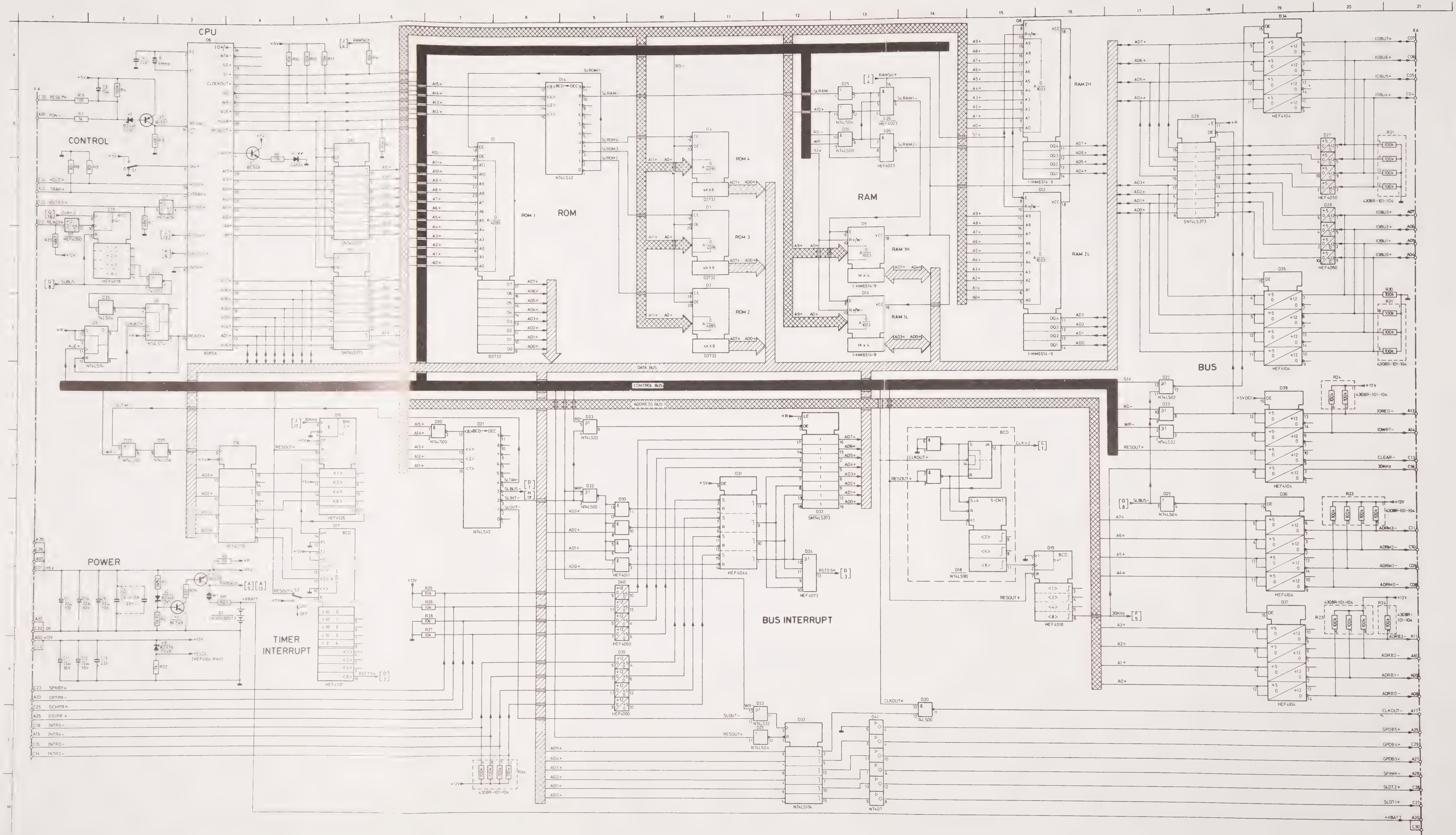

CPU
8085A
CONTROL
POWER
TIMER INTERRUPT
ROM
ROM 1
ROM 2
ROM 3
ROM 4
D2732
RAM
RAM 1H
RAM 1L
RAM 2H
RAM 2L
1-HM6514-9
DATA BUS
CONTROL BUS
ADDRESS BUS
BUS
BUS INTERRUPT
N74LS42
SN74LS373
HEF4104
HEF4050
HEF4044
HEF4011
HEF4072
HEF4518
HEF4526
HEF4737
N74LS90
N74LS174
N7407
4308R-101-104

Figure 4.10 System Control Card (old version), Schematic

RD5478

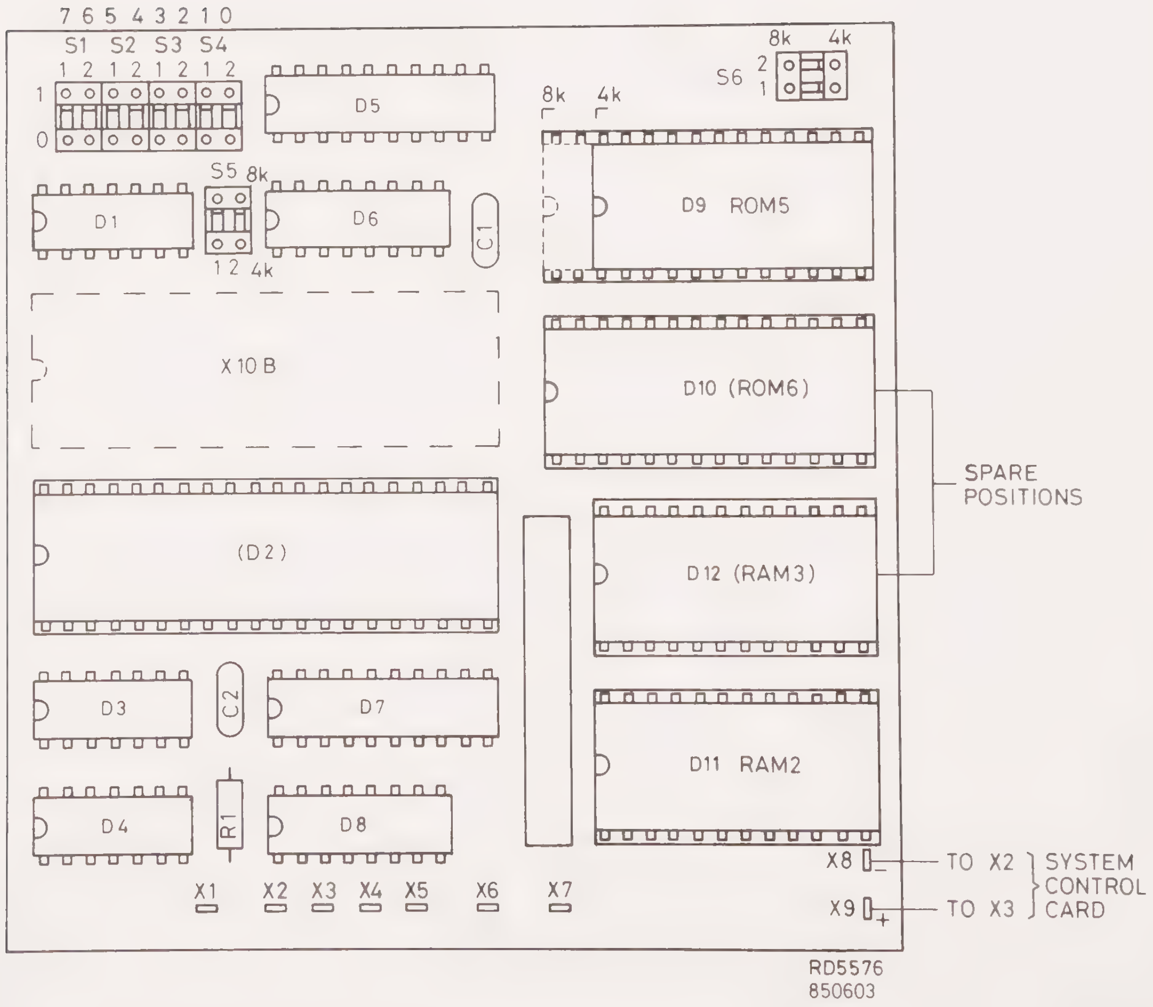

7 6 5 4 3 2 1 0
S1 S2 S3 S4
1 2 1 2 1 2 1 2
1
0
D5
8k 4k
S6
2
1
8k 4k
S5 8k
D1
D6
C1
1 2 4k
D9 ROM5
X 10 B
D10 (ROM6)
SPARE POSITIONS
(D2)
D12 (RAM3)
D3
C2
D7
D11 RAM2
D4
R1
D8
X1 X2 X3 X4 X5 X6 X7
X8 — TO X2
X9 + TO X3
SYSTEM CONTROL CARD
RD5576
850603

Figure 4.11 Memory Extension Card (8/4K), Layout

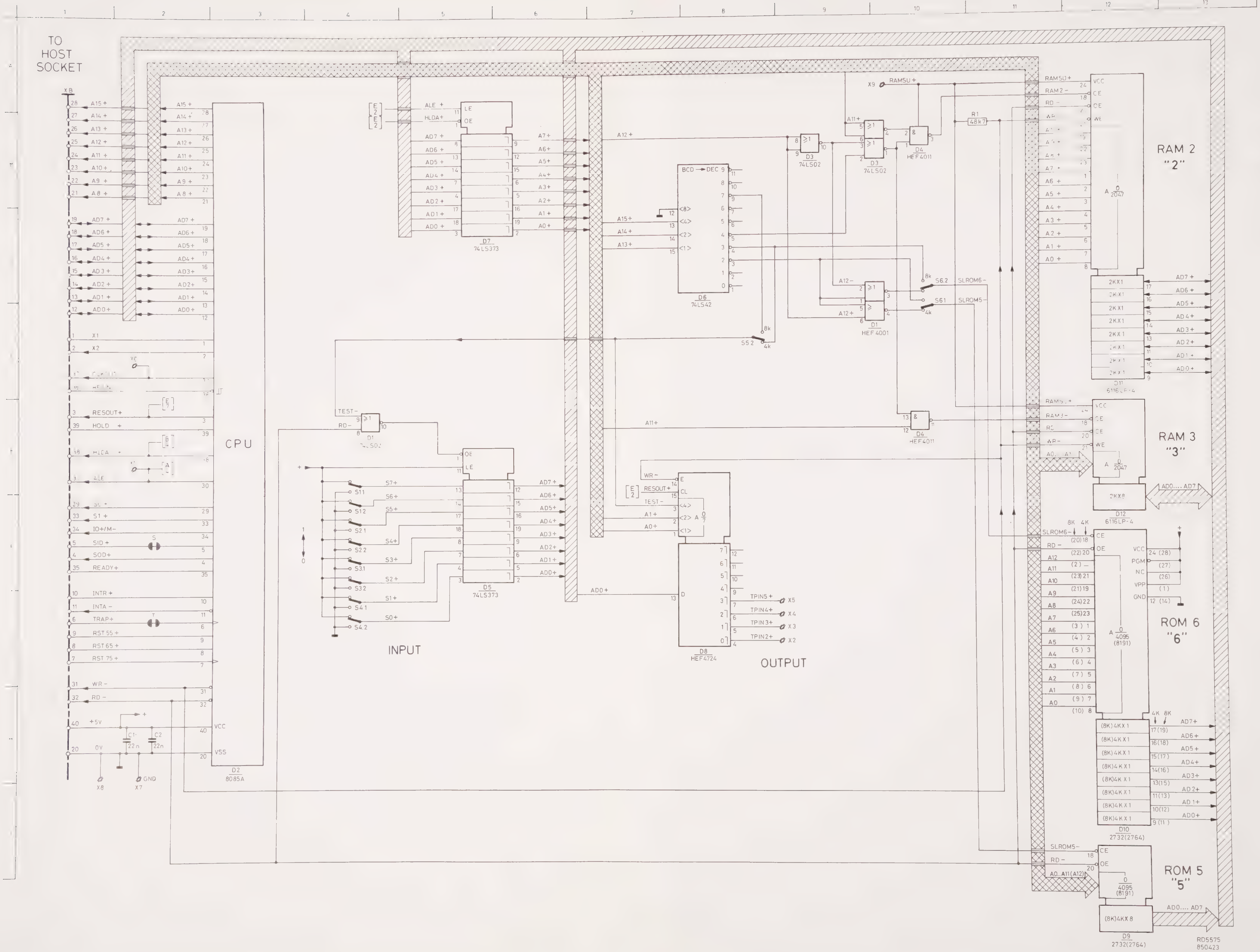

TO HOST SOCKET
XB
A15+
A14+
A13+
A12+
A11+
A10+
A9+
A8+
AD7+
AD6+
AD5+
AD4+
AD3+
AD2+
AD1+
AD0+
X1
X2
RESOUT+
HOLD+
HLDA+
ALE
S1+
IO+/M-
SID+
SOD+
READY+
INTR+
INTA-
TRAP+
RST 55+
RST 65+
RST 75+
WR-
RD-
+5V
0V
C1 22n
C2 22n
X8
GND
X7
VCC
VSS
CPU
D2
8085A
ALE+
HLDA+
LE
OE
D7
74LS373
A7+
A6+
A5+
A4+
A3+
A2+
A1+
A0+
A12+
A15+
A14+
A13+
BCD → DEC
D6
74LS42
D3
74LS02
D4
HEF4011
A11+
X9
RAMSU+
R1
48k7
A12-
S6.2
S61
SLROM6-
SLROM5-
D1
HEF4001
S52
8k
4k
TEST-
RD-
D1
74LS02
OE
LE
S7+
S6+
S5+
S4+
S3+
S2+
S1+
S0+
S11
S12
S21
S22
S31
S32
S41
S42
D5
74LS373
INPUT
WR-
RESOUT+
TEST-
A1+
A0+
E
CL
AD0+
D
TPIN5+
TPIN4+
TPIN3+
TPIN2+
X5
X4
X3
X2
D8
HEF4724
OUTPUT
RAMSU+
RAM2-
RD-
WR-
VCC
CE
WE
A 0/2047
2KX1
D11
6116LP-4
RAM 2 "2"
RAM 3 "3"
A0...A11
2KX8
AD0....AD7
D12
6116LP-4
8K 4K
CE
OE
PGM
NC
VPP
GND
A 0/4095 (8191)
(8K)4KX1
D10
2732(2764)
ROM 6 "6"
SLROM5-
A0...A11(A12)
0/4095 (8191)
(8K)4KX8
D9
2732(2764)
ROM 5 "5"
RD5575
850423

Figure 4.12 Memory Extension Card (8/4K), Schematic

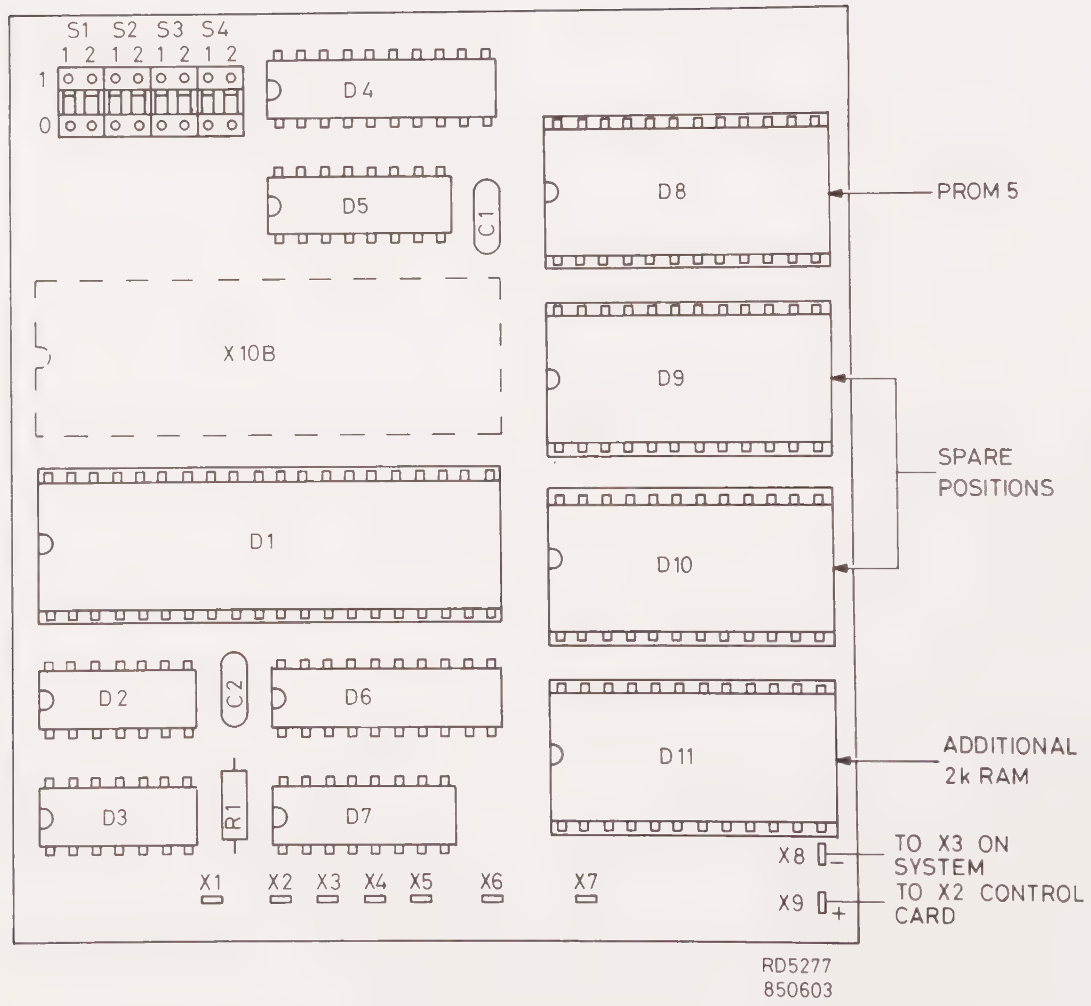

S1 S2 S3 S4
1 2 1 2 1 2 1 2
1
0
D4
D5
C1
D8
PROM 5
X10B
D9
SPARE POSITIONS
D10
D1
D2
C2
D6
D11
ADDITIONAL 2k RAM
D3
R1
D7
X1 X2 X3 X4 X5 X6 X7
X8
X9
TO X3 ON SYSTEM
TO X2 CONTROL CARD
RD5277
850603

Figure 4.13 Memory Extension Card (4K), Layout

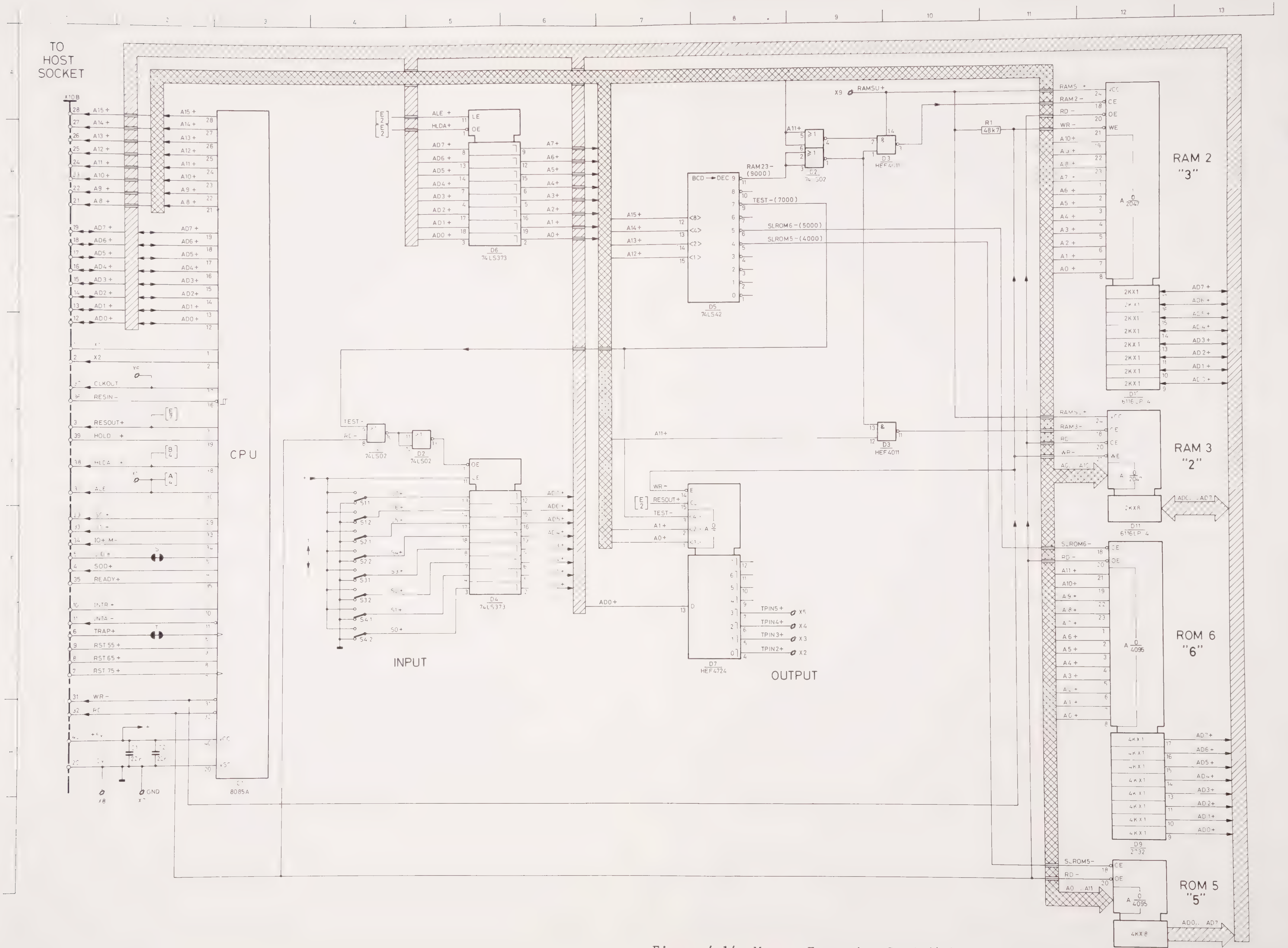

TO HOST SOCKET
CPU
8085A
D6
74LS373
D5
74LS42
BCD → DEC
RAM23− (9000)
TEST−(7000)
SLROM6−(5000)
SLROM5−(4000)
D2
74LS02
D3
HEF4011
R1
48k7
RAM 2
"3"
D10
6116LP 4
RAM 3
"2"
D11
6116LP 4
ROM 6
"6"
D9
2732
ROM 5
"5"
D8
2732
INPUT
D4
74LS373
OUTPUT
D7
HEF4724
TPIN5+
TPIN4+
TPIN3+
TPIN2+
GND
RD5480
850423

Figure 4.14 Memory Extension Card (4K), Schematic

4.3 DUAL SERIAL INTERFACE CARD

4.3.1 INTRODUCTION

The Dual Serial Interface Card acts as two independant interfaces between the PW1710 and two terminals. Each interface has independent channels, one for input and one for output. However, the software treats the second interface as an output only channel.

These input/output channels can be connected to terminals, VDUs, or a computer as long as they are EIA-RS232C/V24 or current loop compatible.

The following functions are provided on the card:

* Two completely independent serial interfaces
* Full duplex operation, transmitter and receiver can work simultaneously
* Setting of all communication parameters via software
* Baud rates from 50 to 19200 bits per second
* 7 or 8 bits per character
* 1 or 2 stop bits
* Parity: none, odd or even
* Error detection
* RS232C/V24 or Current Loop
* V24 for full modem control or data-only
* Current loop 20mA, electrically isolated, with/without current source
* Module address comparator, jumper selectable to address 0 to F (Hex)

To provide the above mentioned functions the card utilizes the following hardware groups:

* Address Comparator
* Card Control
* Data Bus Driver
* Mode Selection
* USART 1
* USART 2
* Mode Selection
* Interrupt
* Driver 1
* Driver 2

The schematic diagram for this card is shown in figure 4.17, and the layout is given in figure 4.16.

4.3.2 ADDRESS COMPARATOR

D34 [A,B-2] decodes the 4 module address lines into a card select signal (jumper selected to 1 hex).

4.3.3 CARD CONTROL

The card select signal enables D27 [D-4] to decode the 4 byte address lines into dedicated byte select lines. Together with IORED- and IOWRT- the various read-byte and write-byte signals are composed (D30 and D29).

Table 4.3 below gives an overview of the bytes and their functions:

Table 4.3 Byte Allocation

BYTE ADDRESS (hex)	DIRECTION	FUNCTION
0	WRITE	data, to be transmitted by USART 1
0	READ	data, received by USART 1
1	WRITE	Mode/command for USART 1
1	READ	Status from USART 1
2	READ	Mode setting switches for USART 1
4	WRITE	Baud rate settings for USART 1
4	READ	Baud rate switches for USART 1
8	WRITE	data, to be transmitted by USART 2
8	READ	data, received by USART 2
9	WRITE	Mode/command for USART 2
9	READ	Status from USART 2
A	READ	Mode setting switches for USART 2
C	WRITE	Baud rate settings for USART 2
C	READ	Baud rate switches for USART 2

4.3.4 DATA BUS DRIVER

Since the card uses +5V logic and the XRA-bus uses +12V logic, level converters are necessary in both directions. Parts of D26 and D32 [G,H,J-3] convert data from the XRA-bus from +12V into +5V and D21 drives the card´s data bus except during a card-read cycle.

During a card-read cycle, data from the card is converted into +12V by D19 and D20. Normally the outputs of D19 and D20 are floating, but when IORED- goes LOW (=TRUE) and the card is selected the outputs become active.

4.3.5 USARTs 1 and 2

The heart of the card is formed by two 8251A type USARTs (Universal Synchronous or Asynchronous Receiver and Transmitter). The USART is a complex and versatile LSI which requires initial configuration. The USART has two serial-to-parallel converters (a transmitter and a receiver), and five registers, three for control purposes and two for data. The registers are:

MODE REGISTER - Control
COMMAND REGISTER - Control
STATUS REGISTER - Control
INPUT DATA REGISTER (BUFFER) - Data
OUTPUT DATA REGISTER (BUFFER) - Data

4.3.5.1 The Receiver

The receiver accepts data via pin RxD (received data) from the outside world in a character-serial/bit-serial format with a predetermined sample rate (called the baud rate).

Upon completion of a character, this character is converted into parallel data and put into the INPUT DATA REGISTER.

4.3.5.2 The Transmitter

The transmitter accepts data in a parallel format from the XRA-bus controller and puts it in the OUTPUT DATA REGISTER.

Upon receiving data, the transmitter starts transmission of the stored data via pin TxD (transmit data) in a bit-serial way, with a predetermined speed (the baud rate), provided the transmitter is enabled and pin CTS (clear to send) is LOW (=TRUE).

As long as the OUTPUT DATA REGISTER holds a character, pin TRDY (transmitter ready) is LOW, when it is empty TRDY goes HIGH. This will generate the common DUAL SERIAL INTERFACE interrupt RST6.5, provided that the appropriate jumper "T" is closed and the transmitter is enabled.

TRDY can be driven LOW by storing another character in the OUTPUT DATA REGISTER or by disabling the transmitter.

Apart from the signal CTS, the USART provides another three signals for modem control (modem =modulator/demodulator) these are:

DTR (Data Terminal Ready),
DSR (Data Set Ready),
RTS (Request To Send)

The presence or absence of these three signals does not affect the functions of the USART.

The structure of the READ and WRITE bytes for the two USARTs is the same for all four bytes and is as follows:

WRITE byte 0= USART 1 output data
READ byte 0= USART 1 input data
WRITE byte 8= USART 1 output data
READ byte 8= USART 1 input data

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

NOTE: When 7 bits/char is selected, the 8th bit (BIT7) is always a "0"

Explanation of the format of Serial Output Data.

Refer to figure 4.15, it can be seen from the figure that data is output from the USART in serial form as follows:

1. It always starts with a START bit.
2. The START bit is then followed by the data bits, which, depending on the selected parameter can be 7 or 8 bits in length (least significant bit first). Although the USART also supports 5 and 6 bits per character, they are not used on this card.
3. If PARITY has been requested the USART will add a parity bit onto the end of the data bits.
4. The sequence is ended by a STOP bit, or if requested by TWO STOP bits.

The selection of parameters such as parity, number of stop bits and so on, is dependant on the peripheral device (terminal) which is to work with the interface.

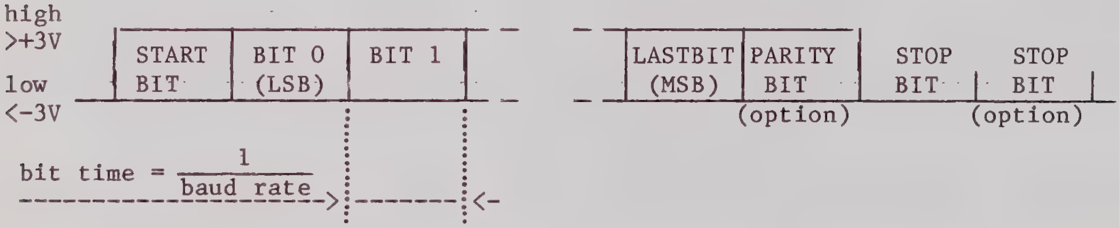


Figure 4.15 Data Output

4.3.5.3 Mode Register - Control

The mode buffer stores information on the format of the character in serial mode such as:

> SYNCHRONOUS or ASYNCHRONOUS transmission, how many STOP BITS in asynchronous mode, parity CHECK yes/no; and if yes, ODD or EVEN check the number of bits in a character, baud rate factor (ratio between baud rate clock and baud rate).

The first write instruction to this address after a RESET is a mode instruction:

WRITE byte 1= USART 1 mode } first WRITE after RESET
WRITE byte 9= USART 2 mode

STOP BITS	PARITY	PARITY	CHAR. LENGTH	BD. RATE FACTOR
00= NO STOP BITS	0=ODD	0=DIS.	00= 5 BITS/CHAR	00= SYNC
01= 1 STOP BIT	1=EVEN	1=ENAB.	01= 6 BITS/CHAR	01= FACTOR 1
10= 1/2 STOP BITS			10= 7 BITS/CHAR	10= FACTOR 16
11= 2 STOP BITS			11= 8 BITS/CHAR	11= FACTOR 64

4.3.5.4 Command Register - Control

All data written to this address other than in a mode instruction is stored in the command buffer. This buffer controls the operation of the USART such as:

enable/disable the transmitter,
enable/disable the receiver,
drive the modem control pins (DTR, RTS),
reset the error flags.

WRITE byte 1= USART 1 command
WRITE byte 9= USART 2 command

ENABLE HUNT MODE=1	RETURN TO MODE=1	RTS 1 = ON	ERROR FLAGS 1=RESET	BREAKS 1=SEND	RCV 1 = ON	DTR 1 = ON	TMIT 1 = ON

4.3.5.5 Status Register - Control

On request the USART can send status information to the XRA-bus controller. The status register contains information about:

readiness for use of transmitter and receiver,
monitor the modem status (DSR),
communication error (error flags),

READ byte 1= USART 1 status
READ byte 9= USART 2 status

DSR 1 = ON	DETECT 1=BREAK	FRAMING 1=ERROR	OVERRUN 1=ERROR	PARITY 1=ERROR	TMIT 1=EMPTY	RCV * 1=READY	TMIT * 1=READY

* = An interrupt request "RST6.5" is generated as long as at least one of the indicated bits is true and the appropriate receiver or transmitter is enabled and the appropriate jumper (R or T) is closed.

BREAK:	An all "1" character has been detected (level).
ERRORS:	Framing error: A character has been received with an improper frame, for example, the required number of data bits is incorrect. Overrun error: The character in the INPUT DATA REGISTER has overwritten the previous character which was not read in time by the XRA-bus controller. Parity error: The expected parity bit has not been detected.
REGISTER STATUS:	Transmitter empty: No character is currently being put into serial form. Receiver ready: A character is available in parallel mode in the INPUT DATA REGISTER. Transmitter ready: The OUTPUT DATA REGISTER can accept a character.

4.3.5.6 Input Data Register (Buffer) - Data

The INPUT DATA REGISTER receives characters in parallel form from the Receiver. The XRA-bus controller is signalled that the character is ready by pin RRDY (receiver ready) going HIGH. This will generate a common DUAL SERIAL INTERFACE interrupt RST6.5, provided the appropriate jumper "R" is closed and the receiver is enabled.

RRDY will go LOW when the INPUT DATA BUFFER has been read.

4.3.5.7 Output Data Register (Buffer) - Data

The OUTPUT DATA REGISTER is used by the Transmitter to store a character before transmission.

4.3.5.8 Baud Rate

The speed per USART for input bit sampling and output bit shifting is derived from the baud rate generators, which consist of a crystal oscillator and a programmable divider. On this card the two baudrate generators D13 [A-12] and D12 [G-12] share the same crystal oscillator (2.4576 MHz; in D13), but perform independently.

The crystal frequency is first divided by 8, resulting in a frequency of 307.2 kHz. This frequency is used by the USARTs as their internal clock (CLK), and is available for further division.

The divider (a 4-bit value) is stored by the XRA-bus controller in the D-type flip-flops D10 and D11. The required frequency x 16 at output Z of the baud rate generators is routed to the USART transmitter and receiver clock inputs TxC and RxC.

Because it is a common clock, both the transmitter and the receiver have a common baud rate.

The baud rates are set by WRITE bytes 4 and C, and their structure is as follows:

WRITE byte 4 = USART 1 baud rate } for baud rates, refer to the
WRITE byte C = USART 2 baud rate } settings overview in Chapter 2.

				BAUD RATE SELECTION			
X	X	X	X	S3	S2	S1	S0

The baud rate settings can be checked together with other communication parameter settings, not supported by the USARTs.

DCD (Data Carrier Detected)
ECHO (Re-transmit the received character as a check)

These parameters are read by READ bytes 4 and C which are structured as follows:

READ byte 4 = USART 1 miscellaneous settings
READ byte C = USART 2 miscellaneous settings

DCD	ECHO	SWITCH	CTS	BAUD RATE SELECTION			
1=OFF	0 = NO 1 = YES	S8.1 #1 S8.2 #2	1=OFF	S3	S2	S1	S0

NOTE: Switches S8.1 and S7.1 are not used at present.

4.3.6 MODE SELECTION

Initialisation for the USARTs is made by the XRA-bus controller. The operator can select the appropriate parameters to be used by the software by means of slide switches on the printed circuit board, the slide switch settings are read by the XRA-bus controller during initialization.

Mode parameters can be copied from the MODE SELECTION switches via D24 and D25 and stored in the USART´s mode register. Some of the bits are fixed already:
Only 1 or 2 STOP BITS are possible,
Only 7 or 8 BITS/CHARACTER are possible,
The baud rate factor is fixed to 16.

READ byte 2= USART #1 mode settings
READ byte A= USART #2 mode settings

STOP BITS	PARITY	PARITY	CHAR. LENGTH	BD. RATE FACTOR
01= 1 STOP BIT 11= 2 STOP BITS	0=ODD 1=EVEN	0=DIS. 1=ENAB.	10= 7 BITS/CHAR 11= 8 BITS/CHAR	10= FACTOR 16

4.3.7 INTERRUPT

Each receiver and transmitter has a dedicated "ready" pin. Via jumpers W9 to W12 [L-13], OR-gate D35 collects these signals and D31 converts it into the 12V common interrupt RST6.5.

A particular interrupt source can be reset by performing the appropriate function (for example, read a character, store a character, and so on).

4.3.8 DRIVERS 1 and 2

Connection to the outside world is possible in two ways:

1. RS232C / V24 compatible (voltage swing)
2. Current loop (20mA), quiescent current principle.

* EIA-RS232C / V24 ; This communication system uses data lines and control (handshake) lines. The data lines are as follows:

Pin	Mnemonic	Name	Explanation
2	TxD	transmitted data	data from USART to outside world
3	RxD	received data	data from outside to the USART
4	RTS	request to send	USART wants to transmit data
5	CTS	clear to send	enable the USART´s transmitter
6	DSR	data set ready	outside world (modem) is ready
8	DCD	data carrier detected	carrier wave detected
20	DTR	data terminal ready	ready from USART
1	FGND	frame ground	
7	SGND	signal ground	

EIA levels are:

voltage	level	frame	control	data
> +3V	SPACING	START	ON	"0"
< -3V	MARKING	STOP	OFF	"1"

Converters are necessary to interface the USART to the EIA levels.

Data output TxD is inverted and converted from TTL to EIA-level by D16 or D14. In rest the level at XB is LOW(=MARKING).

Data input RxD is inverted and converted from EIA-level to TTL by D6. In rest the level at XB is LOW. Provided switch S6.2 or S5.2 is in the position "V24", this data is routed to the USART.

The same applies for the input and output control (handshake) lines RTS, CTS, DTR, DSR and DCD. These signals all have pull up/pull down resistor networks (R9 and R10, switch selected) to serve both full modem control and data-only interfacing.

Full modem control (handshake lines are used to affirm and control communication). When switch S6.1 or S5.1 is in position "HS" (hardware handshake), these resistors pull the input levels down, so that lines that are not connected or not driven properly will inhibit communication.

Data-only interface (only data lines are used). When switch S6.1 or S5.1 is in position "DO" (data only), these resistors pull the input levels up, and non-connected inputs do not inhibit communication (which of course must use a protocol in software to control data flow).

For each interface, +12V d.c. and -12V d.c. are available at connector XB to power future adaptors.

- Current Loop; this interface consists of a data output stage, a data input stage and a current source.

  Data output TxD- from the USART is buffered by D1, and via optocoupler D2 or D3, transistor V1 or V3 is turned ON if TxD- is HIGH (marking state) so a current can flow. If switch S2 or S1 is in the position "NC" (no current source), the collector and emitter of V1 or V3 are immediately connected to the communications connector XB and the connected terminal must provide the 20 mA current source. A START bit (TxD- is LOW) results in transistor V1 or V3 being turned OFF.

  If switch S2 or S1 is in the position "C" (with current source), a current can flow from CL+ via R13 or R12, S2.2 or S1.2, V1 or V3, TOUT, the terminal´s receiver, TIN and S2.1 or S1.1 to CL-. When the power supply CL+ CL- is isolated from other power supplies, the current loop circuitry is a completely isolated 20 mA interface.

  Data input RxD- is handled similarly to data output. If switch S3 or S4 is in the position "NC" (no current source), current from the terminal´s transmitter can flow through the LED in optocoupler D5 or D4, causing the corresponding transistor to conduct. Provided S6.2 or S5.2 is in position "CL", RxD- is HIGH, thus indicating the marking state. A START bit (absence of current) interrupts the current through the optocoupler, pulling RxD- LOW.

  If S3 or S4 is in the position "C" (with current source), a current can flow from CL+ via S3.2 or S4.2, R8 or R7, D5 or D4, ROUT, the terminal´s transmitter, RIN and S3.1 or S4.1 to CL-.

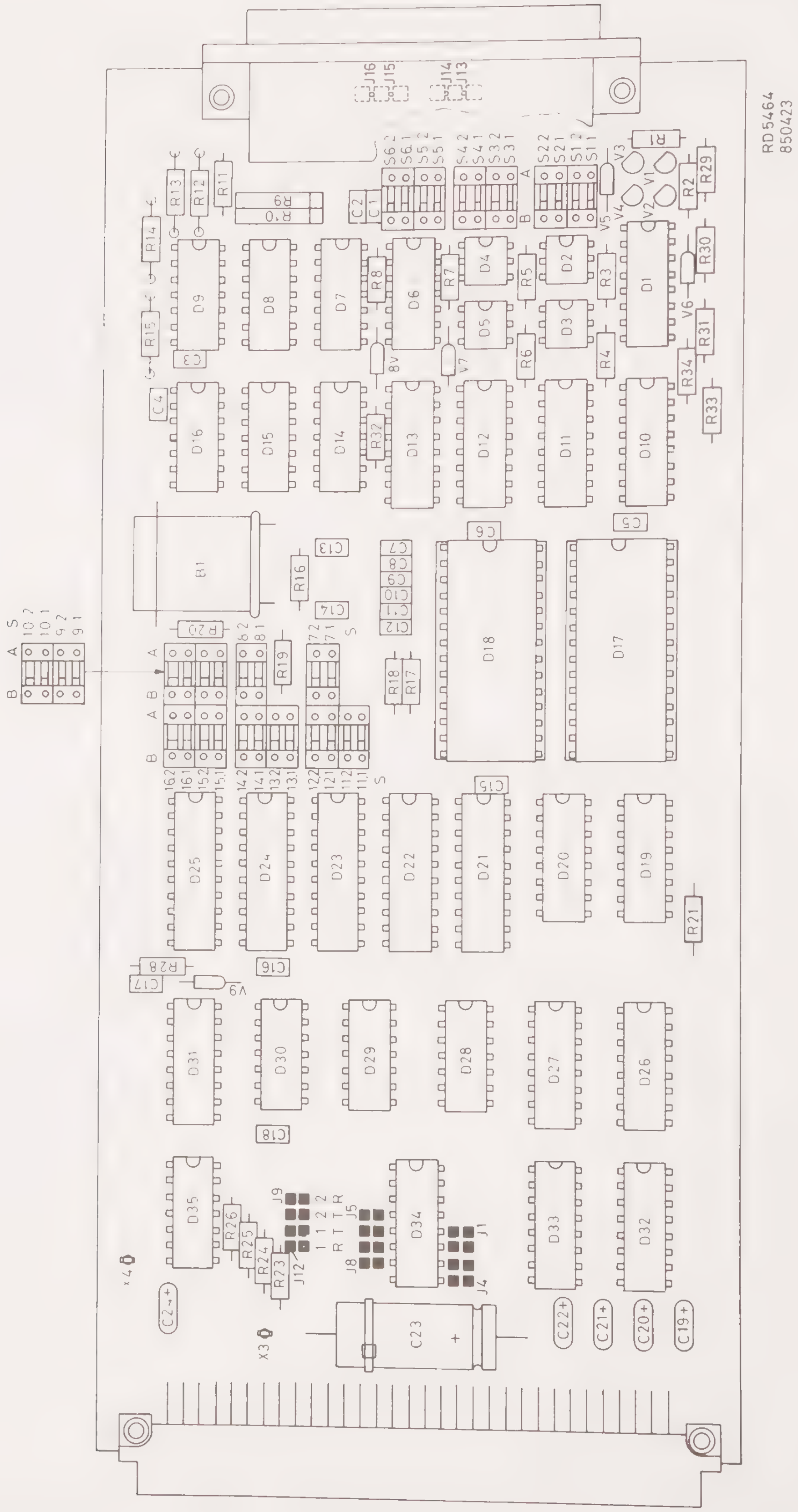

RD5464
850423
J16
J15
J14
J13
R1
R2
R29
V1
V2
V3
V4
V5
V6
V7
V8
V9
S11
S12
S21
S22
S31
S32
S41
S42
S51
S52
S61
S62
A
B
C1
C2
R9
R10
R11
R12
R13
R14
R15
D1
D2
D3
D4
D5
D6
D7
D8
D9
R3
R4
R5
R6
R7
R8
R30
R31
R33
R34
C3
C4
D10
D11
D12
D13
D14
D15
D16
R32
C5
C6
B1
C7
C8
C9
C10
C11
C12
C13
C14
R16
R17
R18
R19
R20
D17
D18
C15
D19
D20
D21
D22
D23
D24
D25
R21
R28
C16
C17
D26
D27
D28
D29
D30
D31
C18
D32
D33
D34
D35
J1
J4
J5
J8
J9
J12
R23
R24
R25
R26
C19+
C20+
C21+
C22+
C23
C24+
X3
X4

Figure 4.16 Dual Serial Interface Card, Layout

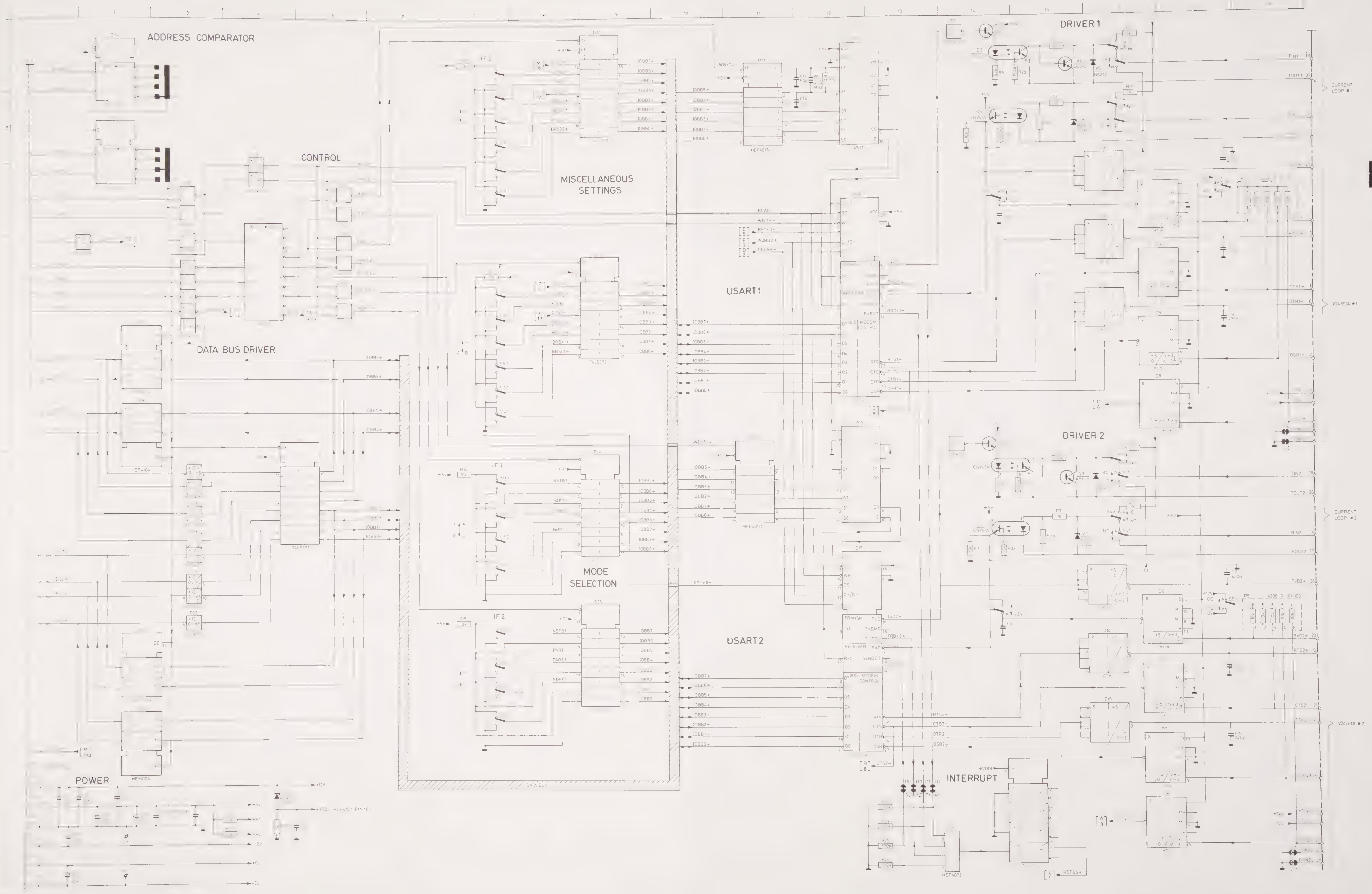

ADDRESS COMPARATOR
CONTROL
MISCELLANEOUS SETTINGS
DATA BUS DRIVER
USART1
MODE SELECTION
USART2
DRIVER 1
DRIVER 2
INTERRUPT
POWER
DATA BUS
CURRENT LOOP #1
V24/EIA #1
CURRENT LOOP #2
V24/EIA #2
HEF4104
74LS373
HEF40174
HEF4072

Figure 4.17 Dual Serial Interface Card, Schematic

RD5481
850423

4.4 DISPLAY KEYBOARD CONTROL CARD

4.4.1 INTRODUCTION

This card is the service hatch between the XRA-BUS and the Display Keyboard (DKB) and the Secondary Control Panel (SCP). In order to do this, there are four functions on the card:

1. Buffering and decoding of module and byte address lines
2. Buffering of input and output data lines
3. Supply of cathode and filament voltages
4. Buffering of Tube-attenuator and Attenuator signals

The schematic diagram for this card is shown in figure 4.19, and the layout is given in figure 4.18.

4.4.2 BUFFERING AND DECODING OF MODULE AND BYTE ADDRESS

The module and byte address lines are applied to latch D9 [B-11] where they are enabled by module address lines ADRM2 and 3 and the IORED signal from D 14-13 [B-4], or by ADRM2 and 3 and the IOWRT signal from D11-6 [B-4] via Nand gate D12 1.2 [B-4].

Via inverting level converters D8 and D4, the module and byte adress lines are connected to NAND gates D11, D12, D13 and D14 and, AND gate D10 [BCDEF-4]; where they are decoded into the following signals:

WRDIS+ = write display
RDDIS- = read display
RDSW1- = read switch 1 (keyboard)
RDSW2- = read switch 2 (hardware selection switches SCP)
WRLED+ = write LED (LED´s BUSY ASSEMBLY REMOTE)

WRDIS and RDDIS are signals which enable the display to be read from or written to. As the XRA-BUS starts on address D800 and the signals WRDIS and RDDIS are decoded from module address lines ADRM 2 and 3, WRDIS and RDDIS start at D8CO and are enabled respectively by the IORED and IOWRT signals from the microprocessor:

RDSW1 is a signal which enables the input latch of the keyboard and has the address D8F2 and is enabled by IORED.

RDSW2 is a signal which enables the input latch of the hardware selection switches on the SCP and is enabled by IORED.

WRLED is a signal to enable the output flip-flop to the LEDs: BUSY, REMOTE and ASSEMBLY on the DKB.

4.4.3 BUFFERING OF IO LINES

In one direction (output data to DKB), the IOBU0-7 lines are connected to output latch D5 [D-9] via inverting level convertors D3 and D4 [D-7]. To enable the output of this latch, the signal coming from D11-6 [B-4] must be true, this means that address D8C0 to D8FF (inclusive) must be on the address lines and the IOWRT signal must be true.

In the other direction (input data from DKB), the IOBU0-7 lines are connected to the inverting input flip-flop, D6 and D7 [E,G-9] where they are converted from 12V to 5V level. To enable these flip-flops, the signal coming from D10-6 [B4] must be true. This means that address D8C0 to D8FF (inclusive) must be on the address lines and the IORED signal must be true.

4.4.4 FILAMENT AND CATHODE SUPPLY VOLTAGE

The 40V coming from the MOPS is rectified and level controlled by V5 [J7] and the filament voltage 9V is superimposed on this rectified voltage, and output as Vf.

The +5v is the supply for the control voltage at the base of V5 which is held at a constant level (-35V) by zener diode and potentiometer R7. If for any reason the +5V is not present, control of V5 is impossible, and the cathode supply is stopped.
Via zener diodes V6 and V7, the 9V is superimposed on the -35V where V6 and V7 act as limiters to obtain the correct RMS value for the filament voltage.

The zener diode V3 serves as a limiter for the collector of V5.

4.4.5 BUFFERING OF ATTENUATOR SIGNALS

The outputs of the tube-attenuator and attenuator are supplied to the X1 amplifiers D1 and D2 [JK-9] and buffered in this way.

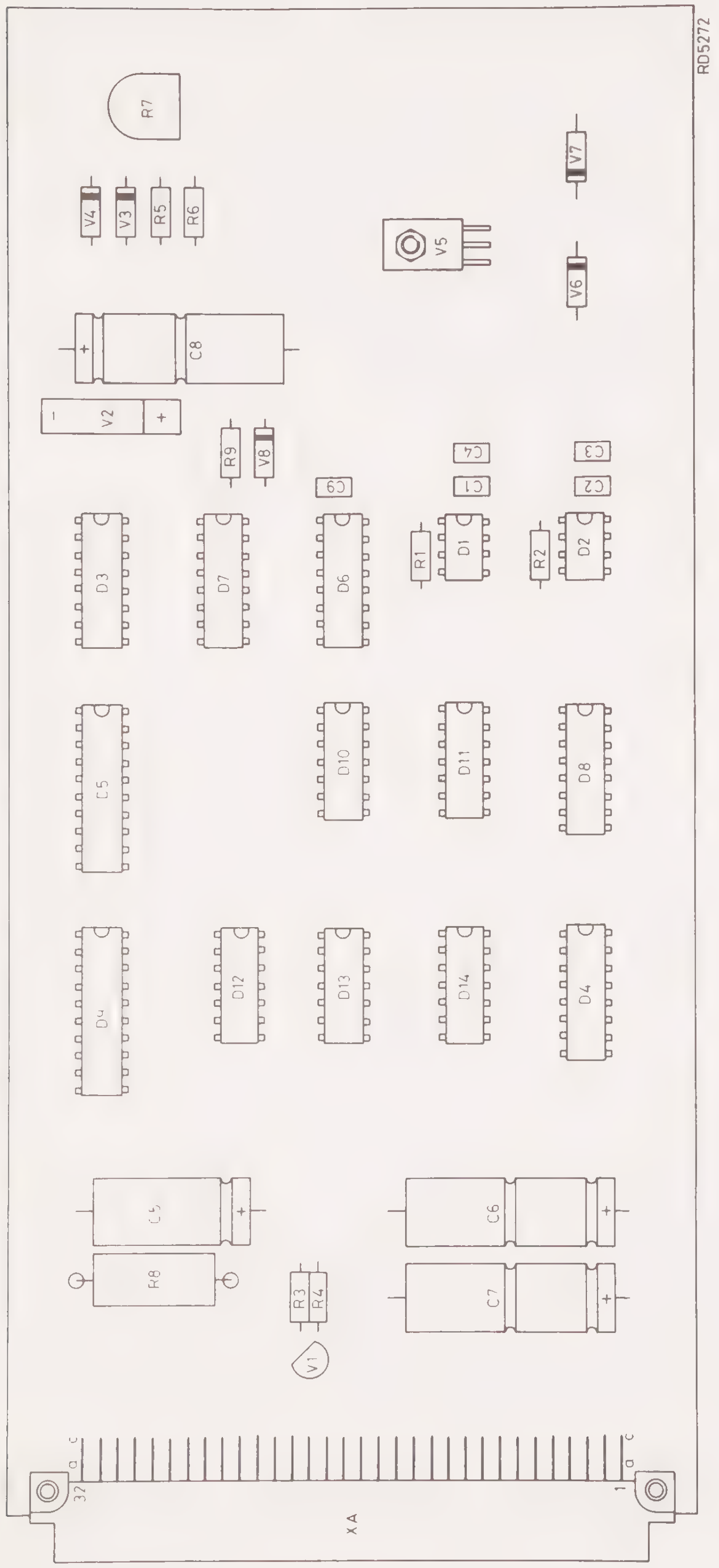

RD5272
R7
V4
V3
R5
R6
V5
V7
V6
C8
V2
R9
V8
C9
C4
C1
C3
C2
R1
D1
R2
D2
D3
D7
D6
D5
D10
D11
D8
D9
D12
D13
D14
D4
C5
C6
R8
R3
R4
C7
V1
32
1
a
c
XA

Figure 4.18 Display Keyboard Control Card, Layout

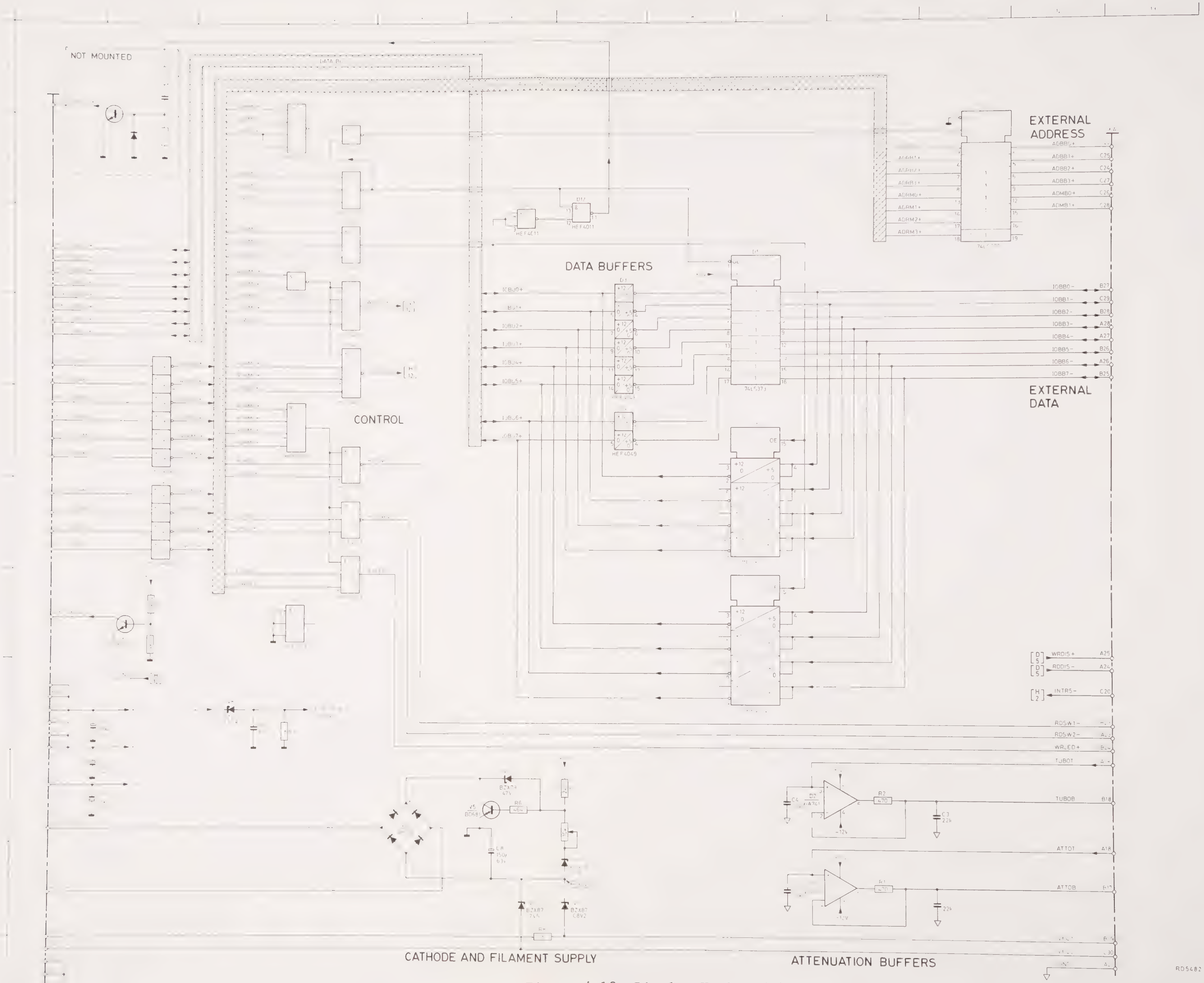

NOT MOUNTED
DATA BUFFERS
CONTROL
EXTERNAL ADDRESS
EXTERNAL DATA
HEF4011
HEF4049
74LS373
ADBB0+
ADBB1+
ADBB2+
ADBB3+
ADMB0+
ADMB1+
IOBB0-
IOBB1-
IOBB2-
IOBB3-
IOBB4-
IOBB5-
IOBB6-
IOBB7-
WRDIS+
RDDIS-
INTRS-
RDSW1-
RDSW2-
WRLED+
TUB01
TUB0B
ATT01
ATT0B
BD681
BZX79
BZX87
CATHODE AND FILAMENT SUPPLY
ATTENUATION BUFFERS
RD5482

Figure 4.19 Display Keyboard Control Card, Schematic

4.5 DISPLAY KEYBOARD

4.5.1 INTRODUCTION

On this board there are three functions:

- Keyboard
- Display
- Function indication

The display function consists of the following:

- Scan oscillator
- 5 bit counter
- Display memory
- 1 out of 20 decoder
- Digit and segment driver
- Twenty 16 segment displays

The schematic diagram for this card is shown in figures 4.22 and 4.24. The layout of the Display Keyboard is given in figure 4.21, and the layout of the Secondary control panel is given in figure 4.23. Figures 4.25 and 4.26 show the layout and schematic diagram of the Secondary Control Panel for the Options Rack PW1748.

4.5.2 KEYBOARD

The keyboard consists of 35 switches connected in a matrix. Commands or display functions can be entered using the keyboard. The switches are as follows:

- 20 Characters (A to X, with J, K, Q, V, Y, Z missing from the alphabet)
- 10 numbers (0 to 9)
- Decimal Point (DP). The decimal point also serves as a space when pressed twice.
- Dash (-)
- STOP switch
- CLEAR switch
- ENTER switch

The keyboard functions as follows:

As an example, when switch S36 [H-5] is pressed, input 10 of D14 [H-4] and input 13 of D15 [H-9] are both switched to +5V. As D14 and D15 are decimal-to-binary encoders with non-inverting outputs, at the output of D14 the binary representation of 0 appears, and at the output of D15 the binary representation of 3 appears. These are respectively 000 and 011. These codes represent 0 and 3, and, as D14 is the Column encoder, and D15 is the Row encoder, from the following table we can decode the switch which was pressed on the keyboard. In this case the switch was in Column 0 and Row 3, which is the S on the keyboard.

Table 4.4 Column and Row numbers

	Column Number									
	0	1	2	3	4	5	6	7		7
Row 0	A	B	C	D	E	7	8	9	Row 4	STOP
Row 1	F	G	H	I	L	4	5	6	Row 5	CLEAR
Row 2	M	N	O	P	R	1	2	3	Row 6	
Row 3	S	T	U	W	X	0	.	-	Row 7	ENTER

If one of the inputs of D14 and D15 is high, the output GS (gate select) also goes high. These outputs are connected to AND gate D18 [J-10], the output of D18 charges capacitor C10 via 10k resistor R8. This causes a delay in activating the second AND gate D18 [J-11], the output of this AND gate clocks the information from D14 and D15 into flip-flop D13 [H-13] and then the information is ready to be read in by the microprosessor when the control signal RDSWI is present. Via C11 and invertor D3 [J-13] interrupt signal INTR5 is generated. The above mentioned delay is required to debounce the switches from the keyboard, and in this way to be sure that stable information is at the input of D13 before it is clocked in.

4.5.3 DISPLAY

4.5.3.1 Scan Oscillator

The scan oscillator [C-4] is made up of two invertors and an RC network. When the output D3-6 is 0V the output D3-4 is high, capacitor C4 is then discharged via resistor R1 until the input of D3-7 is low, giving a high on output D3-6 and a low on output D3-4, capacitor C4 is charged until input D3-7 is high and output D3-6 is low. This will repeat itself continously, and in this way provide a clock signal.

This clock signal is connected via an invertor to the counter input of the 16 CNT, D17 [C-5], the carry output of D17 is connected to the counter input of D16. The outputs of this 5 bit counter (D16/D17) are used as address lines for the RAM chips D9 to D12, and will write the information on the 10 lines into the RAM chips, or read from the RAM chips. Buffered address line ADDB0+ selects between D9 and 11, or D10 and 12; where D9 and 11 is the even part (ADBB0 = 1), and D10 and 12 is the odd part (ADBB0 = 0), in this way it is possible to address 40 addresses with a 5 bit counter. Control signals WRDIS and RDDIS are connected to the PL input (parallel load) of D17 and D16, in this way accessing the Ram chips directly with the address lines ADBB0 to ADDB3 and ADBM1.
Each output from the display memory represents a segment on the 16 segment display as follows:

D9 and D11 represent the segments A, B, C, D, E, F, G and H.

D10 and D12 represent the segments I, J, K, L, M, N, DP and COMMA.

The organisation of the segments is shown in figure 4.20.

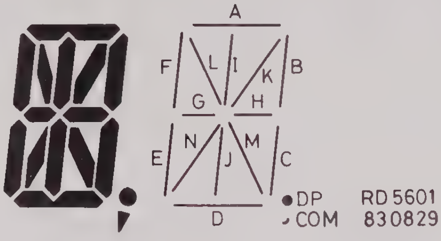


Figure 4.20 Organisation of the Segments in one DIGIT

Because the data bus is only 8 bits wide, and up to 16 segments are needed for one digit, each digit is spread over two bytes using two addresses, an even address and an odd address as follows:

Write D8C0 up to and including D8E7

H	G	F	E	D	C	B	A

COMMA	DP	N	M	L	K	J	I

For example, to write the letter R onto the display the segments A, B, E, F, G, H and M must be lit. For the even byte: A, B, E, F, G, H; and M for the odd byte. To write this to the most right-hand digit, give the command in TEST:

WD8C0 F3 (Hexadecimal) - (even)
WD8C1 10 (Hexadecimal) - (odd)

The following addresses are involved with the display:

DIGIT	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01
Even byte	E6	E4	E2	E0	DE	DC	DA	D8	D6	D4	D2	D0	CE	CC	CA	C8	C6	C4	C2	C0
Odd byte	E7	E5	E3	E1	DF	DD	DB	D9	D7	D5	D3	D1	CF	CD	CB	C9	C7	C5	C3	C1

The segment lines from the RAMs are connected to the segment drivers V26 to V34 [B-5 to 14 on Figure 4.24].

The outputs of the 5 bit counter D16/17 are supplied to the one of 20 decoder D19-D20, the outputs of the decoder are connected to the digit drivers V16 to V25.

The supply for segment and digit drivers comes from V5 [B-5] which is controlled by the clock (CLK). In this way the display is scanned so that the correct segment information is sent to the appropriate digit.

4.5.4 FUNCTION INDICATION

The function indication comprises three LED´s (ASSEMBLY, REMOTE and BUSY) which are controled by the signal WRLED and the datalines IOBU0 to IOBU5 via the HEX flip-flop D1 [Figure 4.24, G-5].

4.5.5 SECONDARY CONTROL PANEL

4.5.5.1 Introduction

The secondary control panel holds three functions:

1. Hardware selection switches
2. Tube selection and attenuation factor
3. High voltage adjustment for scintillation and gas filled detectors

4.5.5.2 Hardware Selection Switches (HWS)

These switches are used to provide information to the microprocessor and are read by the signal RDSW2 on the DKB. Table 4.5 below shows the information that is coming from the switches:

Table 4.5 Hardware Switches

HWS	POSITION 0	POSITION 1	OPTION
0	PW1775	PW1170/10	Sample changer
1	2K	4K	RAM capacity
2	MEMORY TEST	SKIP MEMORY TEST	
3	NO	YES	Second Counting Channel
4	-	-	Spare
5	PM8210/31	PM8203A	Recorder
6	NO	YES	Theta Drive
7	NO	YES	Two-theta Drive

4.5.6 ATTENUATORS

The tube attenuators (selection) can be set to Cr Fe Co Cu or Mo. This attenuator can be set according to the tube annode used in the diffraction setup, without adjusting the high voltage of the detector to match the different pulse height from the detector.

The attenuator can be set between 1 and 8 in six steps to match the pulse height. The attenuators are used on the amplifier annalyser to attenuate the reference voltage of the automatic pulse height correction circuit. See also the Amplifier Analyser Card circuitry.

4.5.7 HV ADJUSTMENT

The HV reference voltage is supplied to a voltage divider which can be set to GAS or SCINT. From this voltage divider a portion of the reference voltage is suplied to the HV2000 card where it is compared with the actual value. See also the HV2000 Card circuit.

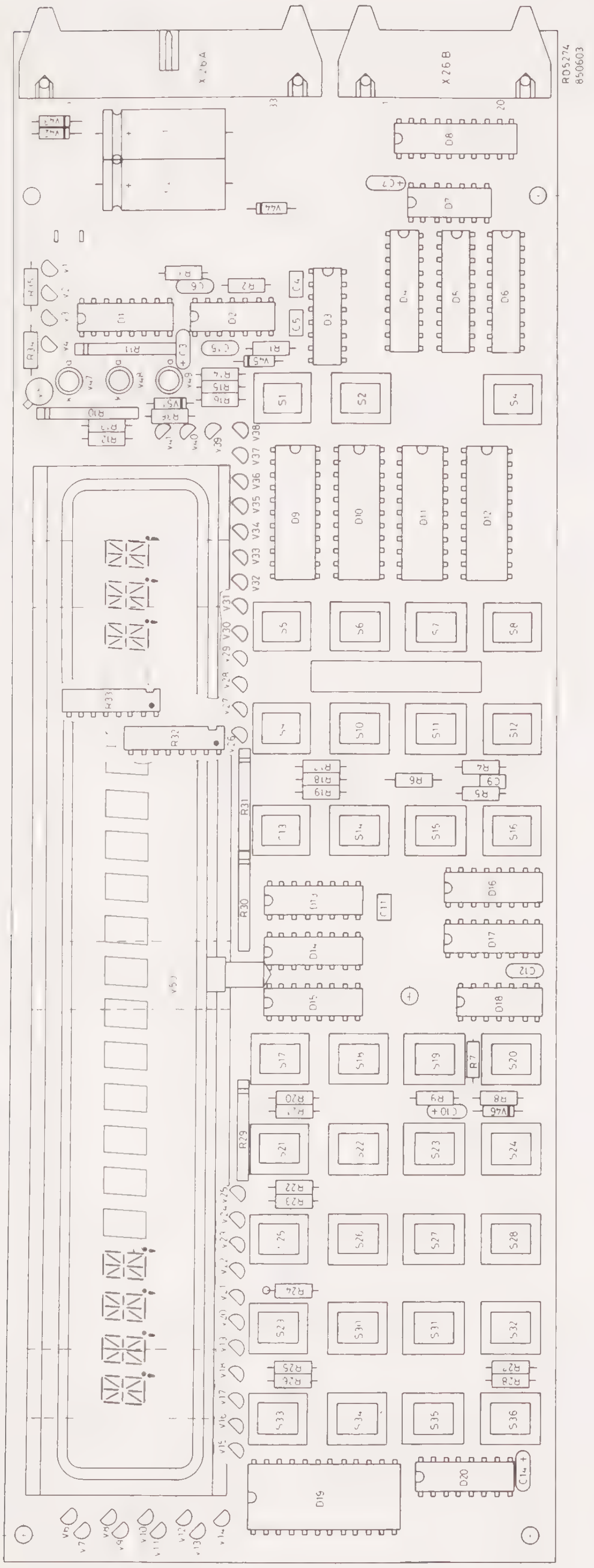

X 26 A
X 26 B
RD5274
850603
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
S1
S2
S4
S5
S6
S7
S8
S10
S11
S12
S14
S15
S16
S17
S19
S20
S21
S22
S23
S24
S25
S26
S27
S28
S31
S32
S33
S35
S36
R31
R30
R29
R32
R33
V38
V37
V36
V35
V34
V33
V32

Figure 4.21 Display Keyboard, Layout

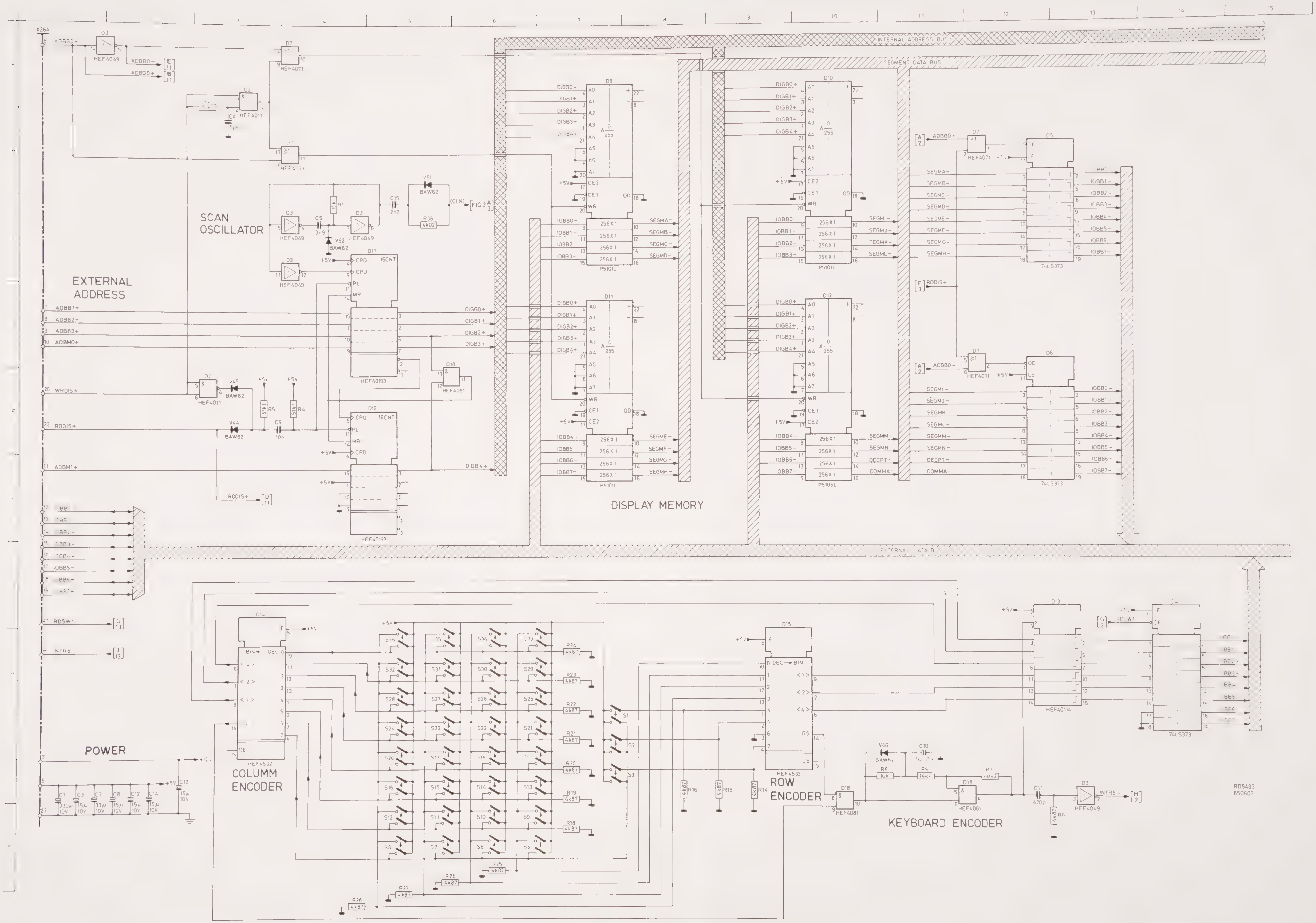
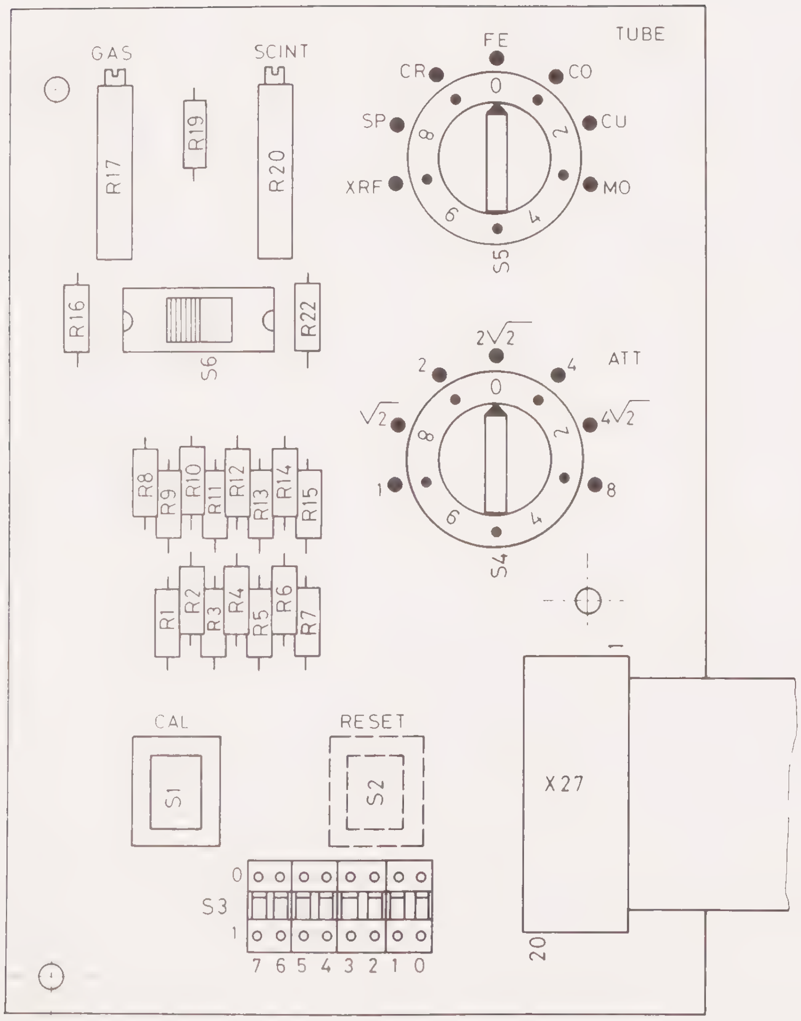

INTERNAL ADDRESS BUS
SEGMENT DATA BUS
EXTERNAL ADDRESS
SCAN OSCILLATOR
DISPLAY MEMORY
EXTERNAL DATA BUS
POWER
COLUMM ENCODER
ROW ENCODER
KEYBOARD ENCODER
X26A
HEF4049
HEF4011
HEF4071
HEF40193
HEF4081
P5101L
74LS373
HEF4532
HEF40174
BAW62
RD5483
850603

Figure 4.22 Display Keyboard Card, Schematic Figure 1


GAS
SCINT
TUBE
FE
CR
CO
SP
CU
XRF
MO
R17
R19
R20
S5
R16
S6
R22
$2\sqrt{2}$
2
4
ATT
$\sqrt{2}$
$4\sqrt{2}$
1
8
S4
R8 R9 R10 R11 R12 R13 R14 R15
R1 R2 R3 R4 R5 R6 R7
CAL
S1
RESET
S2
X27
S3
0
1
7 6 5 4 3 2 1 0
20

RD5467
850423

Figure 4.23 Secondary Control Panel, Layout

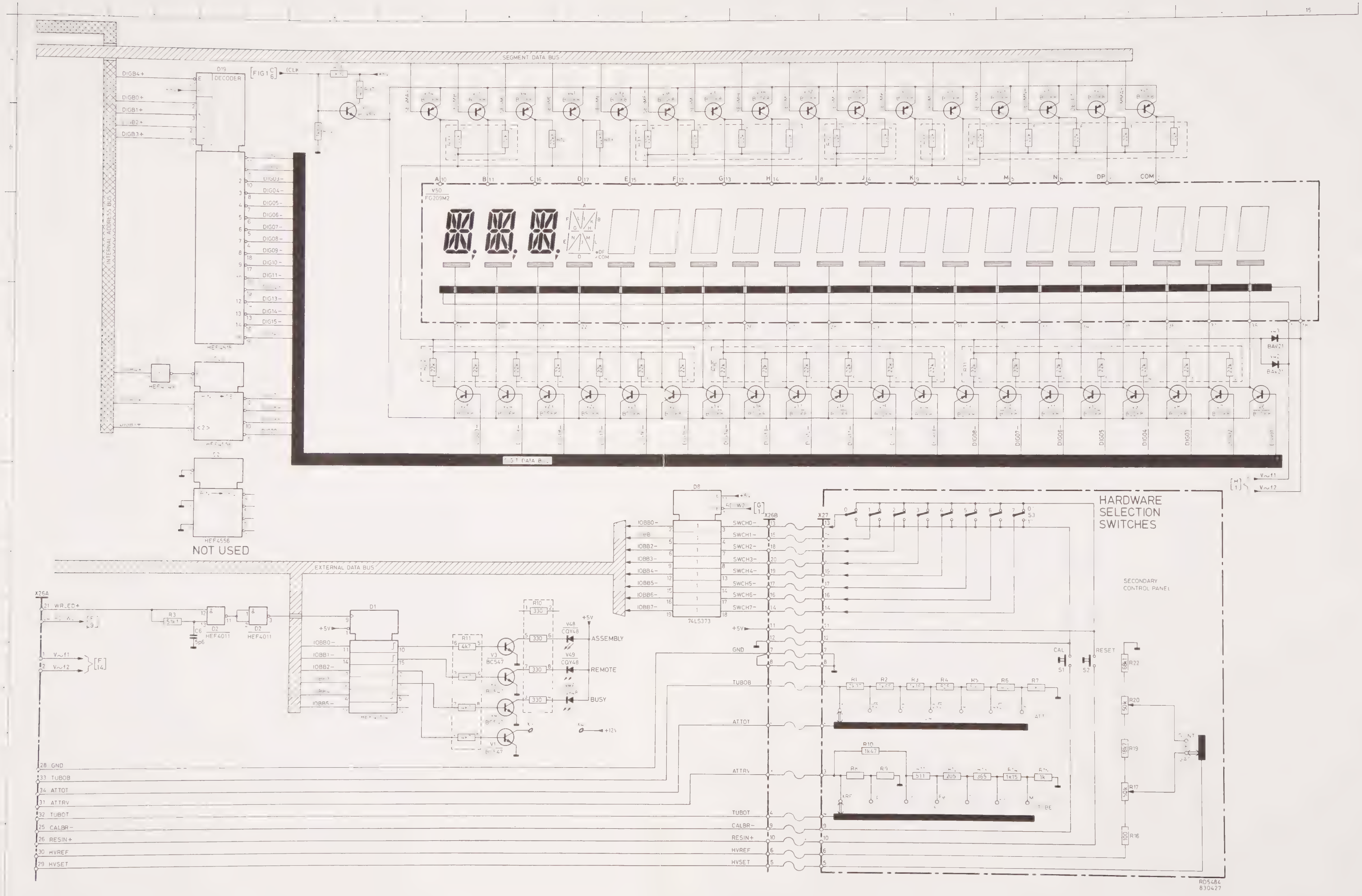
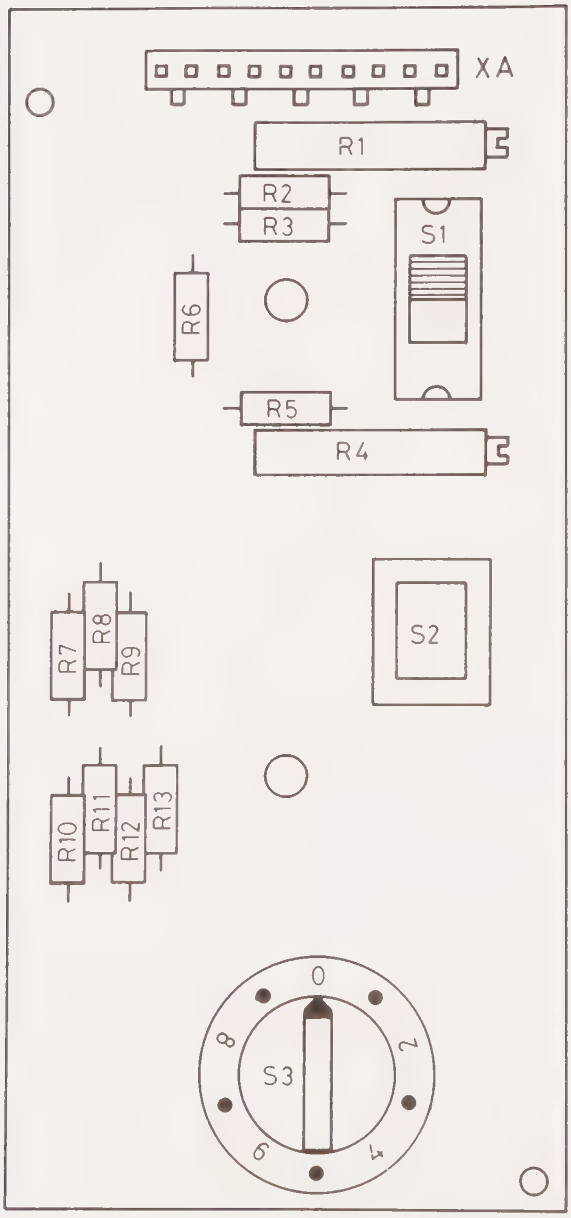

SEGMENT DATA BUS
INTERNAL ADDRESS BUS
DIGB4+
DIGB0+
DIGB1+
DIGB2+
DIGB3+
D19
DECODER
FIG1 C 6
CLK
DIG03–
DIG04–
DIG05–
DIG06–
DIG07–
DIG08–
DIG09–
DIG10–
DIG11–
DIG13–
DIG14–
DIG15–
HEF4515
HEF4556
NOT USED
V50
FG209M2
A
B
C
D
E
F
G
H
I
J
K
L
M
N
DP
COM
BAV21
DIG08–
DIG07–
DIG06
DIG05
DIG04
DIG03
V~f1
V~f2
D8
X26B
X27
HARDWARE SELECTION SWITCHES
S3
IOBB0–
IOBB2–
IOBB3–
IOBB4–
IOBB5–
IOBB6–
IOBB7–
SWCH0–
SWCH1–
SWCH2–
SWCH3–
SWCH4–
SWCH5–
SWCH6–
SWCH7–
74LS373
EXTERNAL DATA BUS
X26A
21 WR.LED+
R3
51k1
C6
5p6
D2
HEF4011
D1
+5V
IOBB0–
IOBB1–
IOBB2–
IOBB5–
R10
330
R11
4k7
V3
BC547
V1
BC547
V48
CQY48
V49
CQY48
ASSEMBLY
REMOTE
BUSY
+12V
SECONDARY CONTROL PANEL
CAL
S1
RESET
S2
R22
R20
R19
R17
R16
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
1k47
511
205
365
1k15
1k
+5V
GND
TUBOB
ATTOT
ATTRV
TUBOT
CALBR–
RESIN+
HVREF
HVSET
28 GND
33 TUBOB
34 ATTOT
31 ATTRV
32 TUBOT
25 CALBR–
26 RESIN+
30 HVREF
29 HVSET
RD5484
830427

Figure 4.24 Display Keyboard Card, Schematic Figure 2


XA
R1
R2
R3
S1
R6
R5
R4
R7
R8
R9
S2
R10
R11
R12
R13
0
2
4
6
8
S3

RD5468

Figure 4.25 Secondary Control Panel (for PW1748), Layout

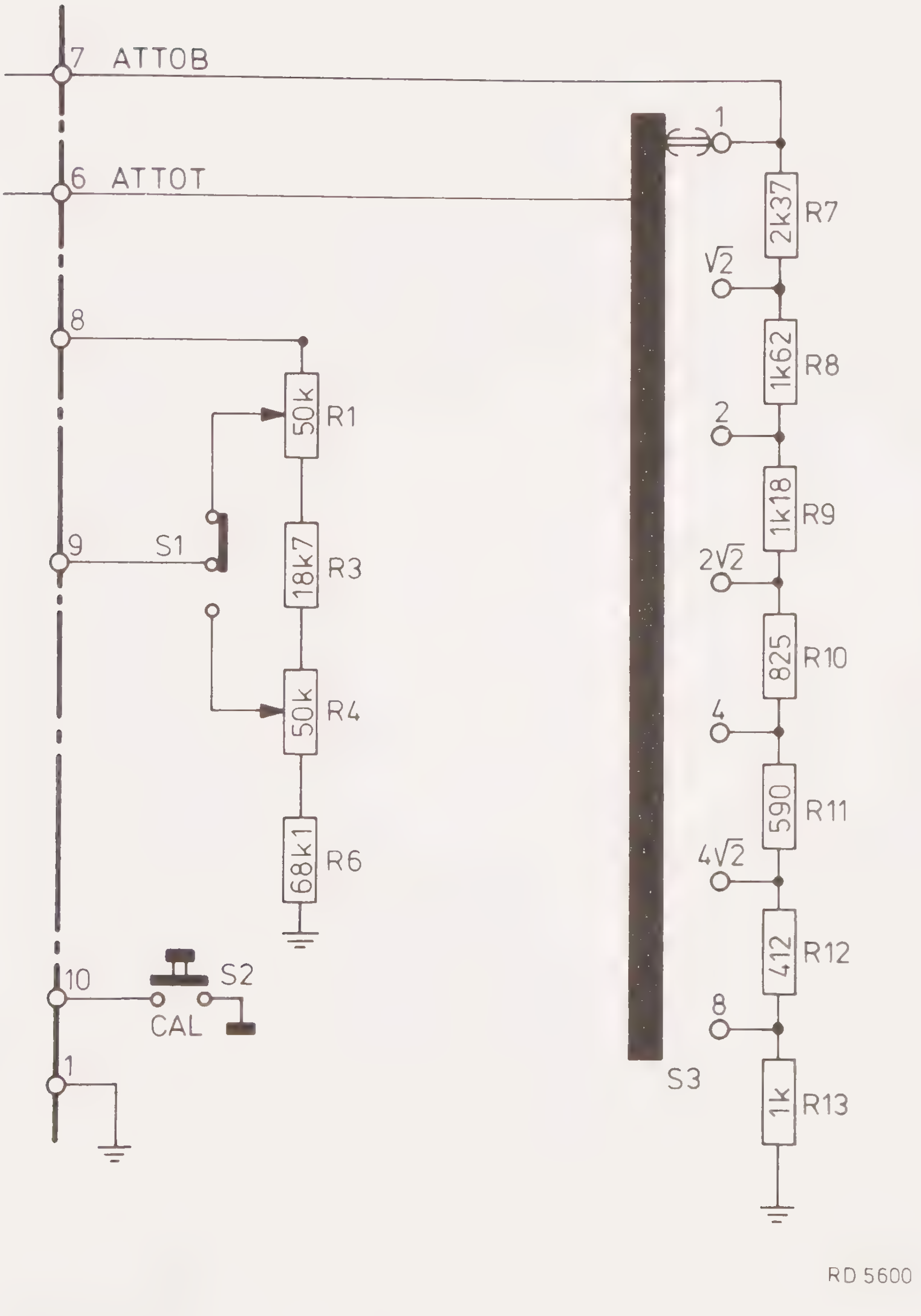

7 ATTOB
6 ATTOT
8
9
10
1
S1
S2
CAL
50k R1
18k7 R3
50k R4
68k1 R6
S3
1
√2
2
2√2
4
4√2
8
2k37 R7
1k62 R8
1k18 R9
825 R10
590 R11
412 R12
1k R13
RD 5600

Figure 4.26 Secondary Control Panel (for PW1748), Schematic

4.6 GONIOMETER CONTROL CARD

4.6.1 INTRODUCTION

This card - together with the Stepping Motor Supply Driver card - acts as an interface between the XRA-bus and a goniometer: stepping motor (with or without shaft encoder) and limit switches. The presence of a shaft encoder permits closed loop control (and in addition much higher setting speed).

Specification of the functions of this microcomputer-based card is largely determined by the software in the on-board ROM.

On this card the software in the on-board RAM "locks-out" most of the usual service possibilities of reading from various addresses. It is however possible to check the microswitch positions and the jumper settings by reading their addresses. The description of the card in this section is therefore supplied more to help in understanding of its working than as an aid to fault-finding.

A number of input and output bits have been provided for future expansion (for instance: a multiplexed angle display output in BCD; which is not yet used).

Brief specifications of this card (combination of hardware and software):

* FAST ANGLE SETTING. Set the goniometer to a predetermined angle as quickly as possible. Setting speed is about 5 to 7.5 degrees/sec (See note 1). An anti-backlash loop is provided when coming from higher angles.

* NORMAL ANGLE SETTING. Set the goniometer to a predetermined angle. Setting speed is about 1 degrees/sec (see note 1). No anti-backlash loop is provided. Stopping without overshoot is guaranteed.

NOTE 1: Without shaft encoder the motor frequency is fixed to 300Hz.

* CONTINUOUS SCAN. Scan to a predetermined angle with a fixed speed, starting from the actual (current) position. Two ranges of scan speeds are available:

0.001 to 0.127 degrees/sec in steps of 0.001
0.01 to 1.27 degrees/sec in steps of 0.01

* (RE)CALIBRATE. Correct the value in the angle register. This correction will always be used by the software when setting an angle for the goniometer until another CALIBRATE updates it.

In order to perform the above mentioned functions, the following items are provided:

- An address decoder (address is jumper selected)
- A CPU
- A chip select decoder
- One socket for 2K (2716) or 4K (2732) of ROM
- 256 bytes of static RAM
- A programmable timer
- Parallel inputs
- 4 x 8 input multiplexer
- Parallel outputs
- Display output (not yet supported)
- Software

The schematic diagrams for this card are shown in figures 4.28 and 4.29, and the layout is given in figure 4.27.

4.6.2 ADDRESS DECODER

IORED and IOWRT are converted from 12V to 5V by D13 to provide the correct logic levels for the micro-processor input, OR-ed by D8 and converted back to the necessary 12V by D26, to enable decoder D25. When enabled, D25 decodes the module address lines. The address is jumper selectable. In the PW1710 the address is set to 7 (in hexadecimal code, jumpers 14 and 3 closed). For the second stepping motor option PW1747 the address is set to 3 in hexadecimal code, jumpers 14 and 4 closed).

D10 converts this card select signal into 5V, the LOW-to-HIGH transition loads a "1" into D9 [E-4] (=set). The output of D9 is connected to the level converter D26, the output of D26 (READY+) turns transistor V1 ON, switching the READY+ line (pin C12) OFF (LOW). At the same time, an interrupt RST6.5 is sent to the CPU D1. The CPU reacts by reading the byte address, the IORED and the IOWRT signals from the data bus. Then the CPU decodes the required function and, if data is to be read from this card, makes that data available to the data bus, or if data is to be written to the card, it reads that data from the data bus. After that the CPU turns the READY+ line ON again by pulling the SOD line HIGH, this triggers D5. D9 will be reset and V1 will be turned OFF, releasing the XRA-bus controller. Maximum allowable OFF-time for READY is 300 microseconds.

4.6.3 CPU

The CPU (D1) is a 8085A with partially time-multiplexed data/address bus, running at 3MHz (= full speed). The frequency of a 6MHz crystal Z1 is divided by two inside the CPU and is used as the master clock. Four vectored interrupts - TRAP (timer interrupt), RST5.5 (shaft encoder index), RST6.5 (bus interrupt) and RST7.5 (shaft encoder step interrupt) - enable fast response to asynchronous events.

For more information about this LSI, refer to the SYSTEM CONTROL CARD or to the 8085A user´s handbook from INTEL or AMD.

4.6.4 CHIP SELECT DECODER

On this card all the data transfers between the card´s CPU and other chips on the card are memory mapped IO. This means that IO+/M- (IO/M) must always be low to enable data transfer.

Address lines A13 and A12 together with the IO/M signal (I/O=HIGH; memory=LOW) are decoded in the Binary-to-Decimal decoder D6 [D,E-6] into dedicated chip select lines. Table 4.6 shows how these signals are decoded, the mnemonic of the decoded signal, the range, the function and the type of device selected.

Table 4.6 Address Line Decoding

IO/M	A13	A12	A8	MNEMONIC	RANGE (HEX)	FUNCTION	IC TYPE
HIGH	x	x	x	x	x	None	
LOW	0	0	x	SLROM	0000 - 07FF	Select ROM	2716
LOW	0	0	x	SLROM	0000 - 0FFF	select ROM	2732
LOW	0	1	x	x	x	none	
LOW	1	0	0	SLRAM	2000 - 20FF	select RAM	8155
LOW	1	0	1	SLRAM	2100 - 2106	select I/O+TIMER	8155
LOW	1	1	x	SLPPI	3000 - 3003	select I/O	8255A

4.6.5 ROM

One socket is provided for ROM (D4), either 2Kbytes (2716) or 4Kbytes (2732). Jumper J7 must be set to the ROM type.

The lower 8 address bits of the CPU are latched into D7 at the falling edge of ALE. When the address is stable and both OE (=RD) and CE (=SLROM) are true (=LOW), the ROM outputs [G,H-10], which are normally floating, become active and place the contents of the addressed byte onto the data bus.

4.6.6 RAM

The 8155 chip (D2) is a combined RAM, parallel I/O and programmable timer chip. When the LSI is addressed by SLRAM being LOW, the falling edge of ALE clockes the lower 8 address bits (contained in AD7 to AD0) into the chip´s internal address buffer. If in addition A8 (=IO/M) is LOW, RAM can be accessed (see table 4.7 below).

256 bytes of static RAM (no refresh required) are provided in D2.

WR- going LOW writes data at pins AD7 to AD0 into the indicated RAM location. RD- going LOW activates the LSI´s output data buffers and RAM contents can be read at AD7 to AD0.

I/O-bits can be addressed similarly to RAM access, except that A8 must be HIGH and AD2 to AD0 contain a code from 000 to 011 when ALE goes LOW. There are 22 IO pins available, they are arranged in three parallel ports of 8, 8, and 6 bits (Port A = PA0 to 7, Port B = PB0 to 7, Port C PC0 to 5). Each port can be configured as input or output port. For the memory map of this IC see table 4.7.

Table 4.7 RAM Port Memory Map

IO/M	AD2	AD1	AD0	FUNCTION
LOW	x	x	x	RAM
HIGH	0	0	0	Port configuration code
HIGH	0	0	1	Port A
HIGH	0	1	0	Port B
HIGH	0	1	1	Port C
HIGH	1	0	0	Timer, low byte
HIGH	1	0	1	Timer, high byte + mode

4.6.7 PROGRAMMABLE TIMER

The timer (also D2) is a 14-bit (high byte and low byte) up counter which can be configured as a preset counter or a frequency divider. To serve as a timer interrupt, the CPU must load the time interval (expressed in a number of clock units) and the timer mode (in this case automatic reload mode). This results in a pulse, at the end of each time interval, with a pulse length equal to the cycle time of the clock input. This pulse is routed to the TRAP input of the CPU, causing a non-maskable interrupt.

The clock input is a 3MHz signal derived from the CPU (=internal clock) or from the XRA-bus (=external clock). An external clock can be switched off temporarily by the XRA-bus controller to allow time for asynchronous events during scans (for example, the printing of Peak Labels).

The timer is addressed when CE is LOW, A8 (=IO/M) = HIGH and AD2 to AD0 contain 100 or 101 when ALE goes LOW. The memory map is given in table 4.7.

4.6.8 PARALLEL INPUT

D3 [Figure 4.28 A,J-11] is a 8255A programmable parallel interface, featuring three 8-bit ports which can be configured as either input or output ports during initialization, it is addressed when SLPPI- = LOW.

Port B of D3 (PB0 to 7) is configured as an input port. It reads data from the goniometer microswitches and XRA-bus signals IORED and IOWRT.

Port C of D3 (PC0 to 7) is configured as an input port. The lower four bits are connected to the 4 x 8 input multiplexer D21 to D24. The upper four bits are connected to stepping motor signals. Since the shaft encoder has open-collector outputs, shaft encoder signals SECHA, SECHB and SECHC are pulled-up by R12 to R14. Parts of D13 and D12 convert 12V into 5V and the CPU can read these levels via PC7 to PC5.

The circuitry around D6 composes several interrupt requests out of the shaft encoder signals SECHA, SECHB and SECHC. The interrupt requests are as follows:

* RST7.5 is an interrupt sent to the CPU at each transition (HIGH-to-LOW or LOW-to-HIGH) of SECHB, provided SECHA is LOW.

  In rest, output 0 or output 3 of D6 is LOW (which of them is LOW is dependant on the state of SECHB, which is reflecting the position in which the stepping motor stopped). During a level transition, the bit codes 01 or 10 are temporarely present at A1 and A2, the inputs of D6 (the signal on A1 is delayed for 5 us by R19 + C9). The codes 01 or 10 result in a negative pulse at output 1 or 2 of D6 for 5 µs, this causes the output of D8 to go LOW for this period and then go HIGH again, the transition LOW-to-HIGH is the RST7.5 interrupt

  In the interrupt service routine, the CPU must know in which direction the motor shaft moved. Therefore the direction of rotation, represented by the level of SECHB after its transition, is clocked into flip-flop D9 (DIRFF).

* RST5.5 is an interrupt sent to the CPU each time the one-time-per-revolution signal SECHC (INDEX) = LOW. For more accuracy this signal is gated (narrowed) by SECHA being LOW.

4.6.9 4 X 8 INPUT MULTIPLEXER

32 Input bits can be read via four multiplexer ICs D21, D22, D23 and D24. Each multiplexer has three selection bits S2, S1 and S0 to select which of the eight input bits is to be read. Parts of D11 and D12 convert the multiplexer´s 12V logic into 5V for D3´s port C.

The selection bits SELB2 to SELB0 are driven by D2. Bits PC2 to PC0 of port C are converted by D16, D20 and D17 and connected to the four multiplexers. The various data sources for the multiplexer input are listed in Table 4.8 below:

Table 4.8 Multiplexer Data Sources

	READ BY D3 (PPI 8255A) PORT C				
S2 S1 S0	PC3	PC2	PC1	PC0	FUNCTION
0 0 0	IOBU7	IOBU6	IOBU5	IOBU4	XRA-bus data, upper nibble
0 0 1	IOBU3	IOBU2	IOBU1	IOBU0	XRA-bus data, lower nibble
0 1 0	MCOLA	MCOLB	MCOLC	MCOLD	Motor coils (check)
0 1 1	MOTHV	DEGRM	STEP2	INTR2	Miscellaneous signals (check)
1 0 0	BLANK	DSEL4	DSEL2	DSEL1	Display: digit number (check)
1 0 1	DISB8	DISB4	DISB2	DISB1	Display: digit data (check)
1 1 0	ADRB3	ADRB2	ADRB1	ADRB0	XRA-bus byte address
1 1 1	J8	J9	J10	J11	Jumpers

4.6.10 PARALLEL OUTPUT

Parts of ports B and C of D2 are used for driving output bits (therefore these ports must be configured as output ports during initialization). Before the ports have been initialized, their outputs float and resistors are necessary to guarantee proper logic levels.

The output bits are connected to level converters D16, D20 and D17 to drive the 12V XRA-data bus.

Bits PB7 to PB4 control the stepping motor coils (MCOLA to MCOLD). The high voltage is supplied to the stepping motor under the control of the 20 ms one-shot D5 (MOTHV). When the motor is running, the output from PB7 tries to trigger (and retrigger) the 20 ms one-shot D5. This is only possible when PB3 is high; in this case the output of D5 is continuously HIGH (provided the frequency of PB7 is over 50 Hz). This one-shot is used as a safety device for the stepping motor. When the motor is blocked, the high voltage supply is switched off via MOTHV because the one-shot will not be triggered anymore.

PB2 drives transistor V3, which controls an event marker in the strip chart recorder (DEGRM).

PB1 (STEP2) can be used to synchronize external events to the stepping motor. At every 0.01 degree step, a pulse is generated.

Via PB0 the CPU generates an interrupt (INTR2) to the XRA-bus when the required function has come to an end (READY becomes "1" in the card´s status register; refer to "Software").

PC4 switches LED V6 ON via transistor V4 as long as power is present.

4.6.11 DISPLAY

Port A of D3 is configured as output port, but is not yet supported by software. When used as a display driver the upper four bits PA7 to PA4 could contain the digit address and the leading zero blanking information. The lower four bits PA3 to PA0 could contain digit data in BCD. Level converters D18 and D19 convert 5V into 12V provided DISPA (display angle) = HIGH (otherwise the outputs remain floating). Outputs can be checked via multiplexers D21 to D24.

4.6.12 SOFTWARE

The link between the card´s input and output bits and the XRA-bus is via software. This software determines to a high degree the transparency of the hardware to the XRA-bus. Software and hardware together define the instruction set of this card.

Some of the terms used in the following software/byte assignment description may not be familiar to you, they are:

SETPOINT REGISTER:	The setpoint is stored in this register. The setpoint is the angle to which the goniometer must slew or scan after a slew or scan command.
ANGLE REGISTER:	The actual goniometer position is stored in this register. The register is three bytes long.
SCAN SPEED REGISTER:	The scan speed in, binary, in units of 0.01 or 0.001 parts of a degree is stored in this register.
CALIBRATION ANGLE:	The calibration angle is stored in this register. The calibration angle is the angle that the goniometer is set to at power up, or after a RESET, or after a fault. It is the offset between $0^{o}2\theta$ and channel C of the shaft encoder.

WRITE byte 8: command "STOP"

0	0	0	0	0	0	0	0

An all-zero command stops all actions in process.

WRITE byte 8: command "RESTART MICROPROCESSOR PROGRAM"

0	1	1	1	1	1	1	1

This command acts like a hardware RESET to this card.

WRITE byte 8: command "SLEW TO SETPOINT"

1	0	0=FAST 1=SLOW	0	0	X	X	X

Two speeds are available to direct the stepping motor to the required angular position:

FAST means about 5 to 7.5 degrees/s with anti-backlash loop.

SLOW means about 1 degree/s without anti-backlash loop. The direction in which to run is determined by the software.

Angle approach coming from another angle:

1. Fast UP until about 1.2° below setpoint.
2. Then slow UP until setpoint.

Angle approach coming from higher angles:

1. Fast DOWN until about 0.7° above setpoint.
2. Slow DOWN until about 0.5° below setpoint.
3. slow UP until setpoint.

WRITE byte 8: command "SCAN TO SETPOINT"

1	1	X	0	1	X	X	X

The stepping motor must run with a pre-selected and constant speed to the required position. The speed is contained in the SCAN SPEED REGISTER (refer to "scan speed").

WRITE byte 8: command "COPY SETPOINT TO ANGLE REGISTER"

1	1	X	0	0	X	X	X

Copy the three bytes previously stored by WRITE bytes 9, A and B, into Angle register and calculate new offset.

Three bytes contain the setpoint (final angle of a SCAN, SLEW or CALIBRATION ANGLE (in binary, in units of 0.005°):

WRITE byte 9: low byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

WRITE byte A: mid byte

BIT15	BIT16	BIT13	BIT12	BIT11	BIT10	BIT 9	BIT 8

WRITE byte B: high byte

BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16

WRITE byte C: scanspeed

UNIT 0=.001° 1= .01°	SCANSPEED in UNITS PER SECOND (in binary)						
	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

WRITE byte D: scanspeed mode

All bits "0" = NORMAL SCANSPEED
Any non-zero value = HALF SCANSPEED (for second motor drive)

READ byte 0: status (0 = false, 1 = true)

READY *)	LIMIT	EQUAL	0	CALIBR	SCAN	0=DOWN 1=UP	INDEX

*) An interrupt request to the XRA-bus is generated when "READY" becomes true.

The names of the signals mean the following:

READY means that the requested action is completed.
LIMIT means that the limit switch has been activated (READ byte E).
EQUAL means that the goniometer is at the setpoint.
CALIBR means that calibration is in progress.
SCAN means that a scan is in progress.
DOWN/UP indicates the direction of travel of the goniometer.
INDEX means that SECHC (Shaft Encoder CHannel C) is present.

An example of this could be: To scan with a speed of 0.5°/sec. to 40° 2θ, the following actions are required:

1. Convert the 40° into hexadecimal in units of 0.005 degrees. = 1F40.
2. Convert the scan speed into hexadecimal code in units of 0.01°/sec. = 32.
3. Store the hexadecimal code of the setpoint (40°) into bytes 9, A and B.
4. Store the hexadecimal code of the scan speed into byte C.
5. Store 00 hexadecimal into byte D for normal scanspeed mode.
6. Store scan command into byte 8. = C8.

In TEST mode that means the following commands:

```
TST
WD879 40
WD87A 1F
WD87B 00
WD87C 32
WD87D 00
WD878 C8
```

After C8 is enterred the goniometer will scan to 40°.

READ byte 7: software version number (in binary)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

Three bytes contain the actual angular position (in binary; two's complement; in units of 0.005°):

READ byte 9: low byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

READ byte A: mid byte

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT 9	BIT 8

READ byte B: high byte

BIT23	BIT22	BIT21	BIT20	BIT19	BIT18	BIT17	BIT16

READ byte C: error counter (in binary)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

This indicates the accumulated number of errors. An error is the detection of a mismatch of SECHC and the position counter. If this occurs, the motor will be re-calibrated and the error counter will be incremented by 1.

The counter will be reset to zero at power-up, or after a hardware reset, or a "RESTART MICRO-PROCESSOR PROGRAM" command.

READ byte D: zero offset = distance from lower limit to first index pulse in steps of 1/200 of a motor revolution (in binary)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

READ byte E: microswitches ("1" = activated)

0	0	LWLIM	UPLIM	ARDOC	X	0	0

READ byte F: jumpers (see table; "1" = closed)

0	0	0	J5	J8	J9	J10	J11

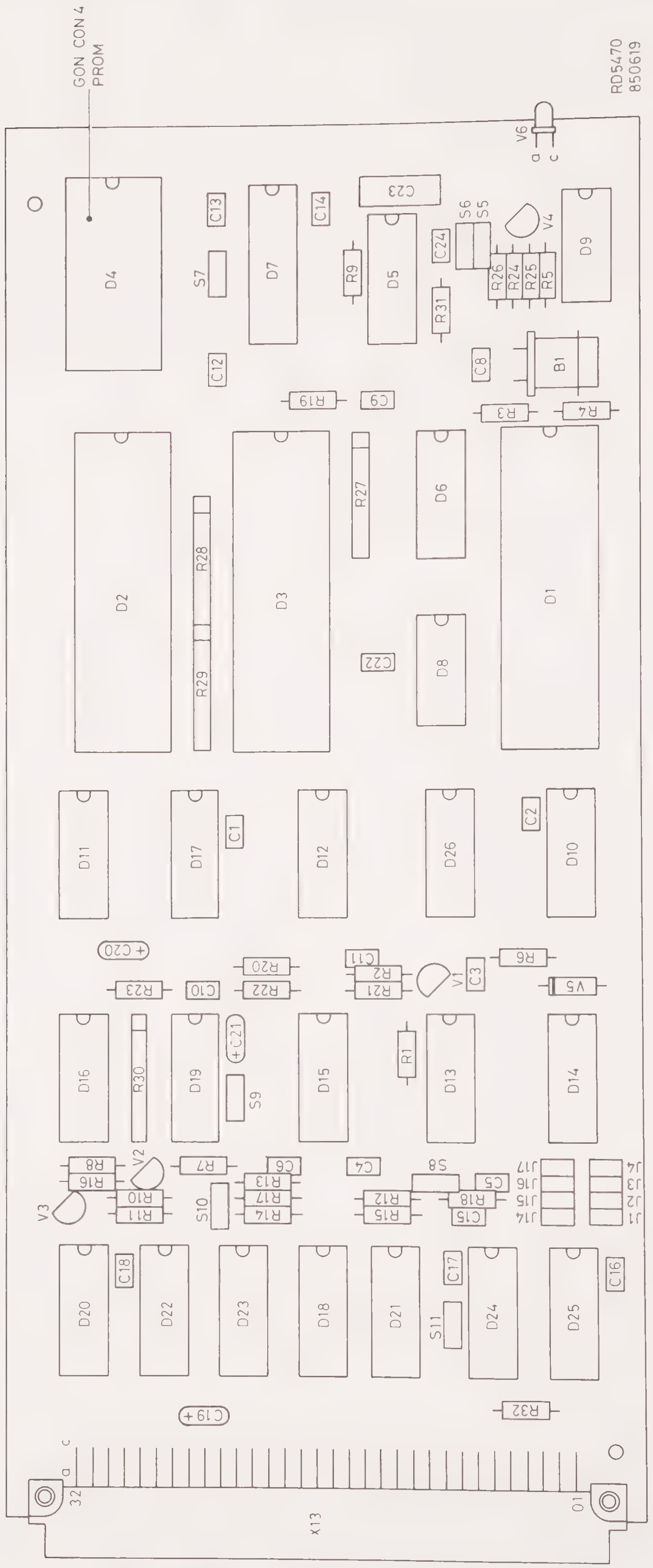

GON CON 4
PROM
RD5470
850619
V6
a
c
D4
C13
S7
D7
C14
C23
R9
D5
C24
S6
S5
V4
R26
R24
R25
R5
D9
R31
C12
C8
B1
R19
C9
R3
R4
D2
R28
R29
D3
R27
D6
D8
C22
D1
D11
D17
C1
D12
D26
C2
D10
C20
R23
C10
R20
R22
C11
R2
R21
V1
C3
R6
V5
D16
R30
D19
C21
S9
D15
R1
D13
D14
R8
R16
V2
R7
C6
R13
R17
R14
C4
S8
C5
J17
J16
J15
J14
J4
J3
J2
J1
V3
R10
R11
S10
R12
R15
R18
C15
D20
C18
D22
D23
D18
D21
C17
S11
D24
D25
C16
C19
R32
c
a
32
X13
01

Figure 4.27 Goniometer Control Card, Layout

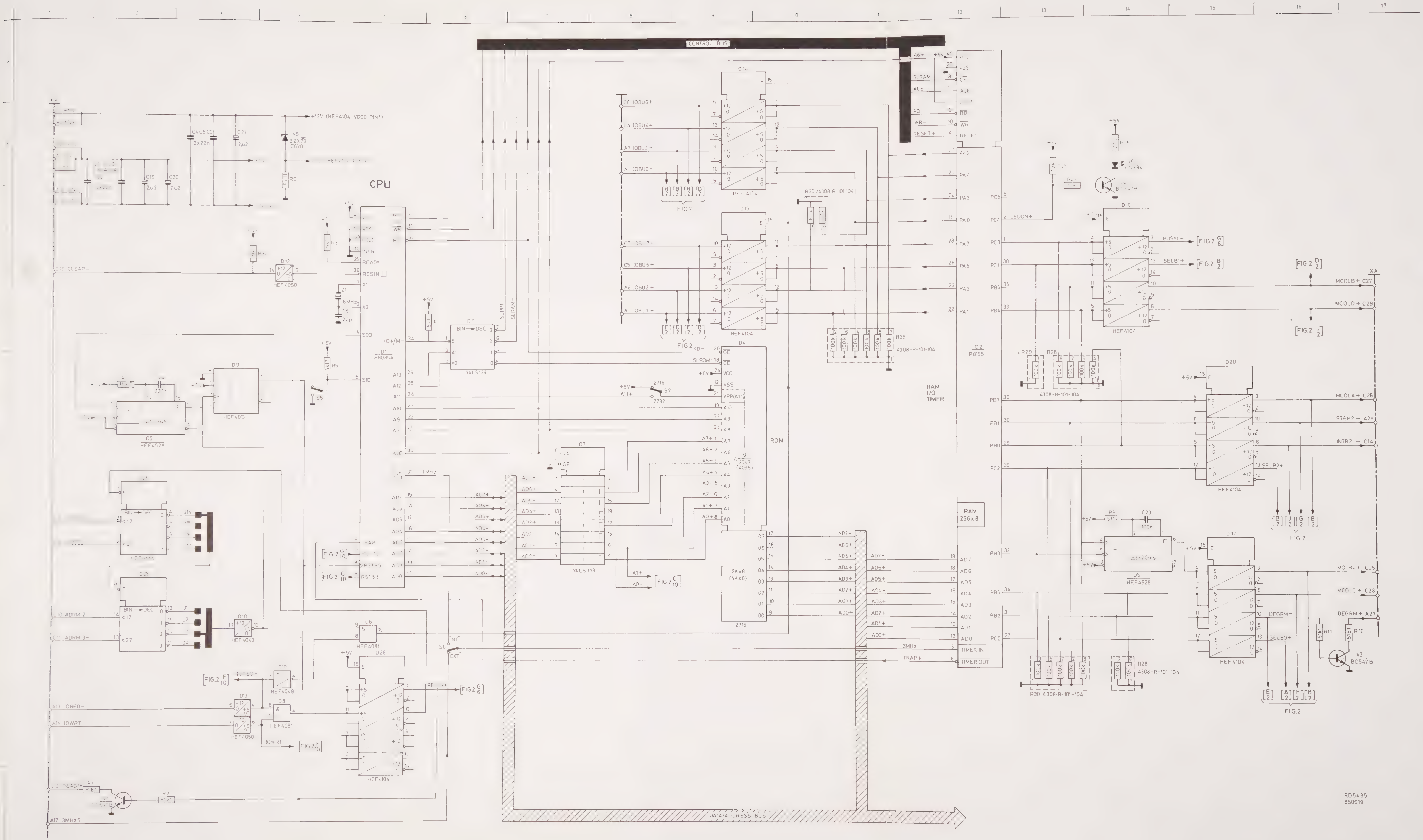

CONTROL BUS
CPU
D1
P8085A
+12V (HEF4104 VDDO PIN1)
C4C5C6
3x22n
C21
2μ2
C19
2μ2
C20
2μ2
BZX79
C6V8
C13 CLEAR–
D13
HEF4050
RESIN
READY
X1
X2
6MHz
SOD
SID
IO/M–
TRAP
RST7.5
RST6.5
RST5.5
A13
A12
A11
A10
A9
A8
ALE
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
3MHz
D9
HEF4013
D5
HEF4528
HEF4556
C10 ADRM 2–
C11 ADRM 3–
D10
HEF4049
D6
HEF4081
D25
HEF4104
A13 IORED–
A14 IOWRT–
D8
HEF4081
IORED–
IOWRT–
FIG 2
S5
S6
INT
EXT
S7
2716
2732
R1
R2
BC547B
C12 READY+
A17 3MHzS
D8
BIN→DEC
74LS139
SLPPI–
SLRAM–
D7
74LS373
D4
SLROM–
RD–
VPP(A11)
2047
(4095)
ROM
2Kx8
(4Kx8)
D14
HEF4104
C6 IOBU6+
C4 IOBU4+
A7 IOBU3+
A4 IOBU0+
D15
HEF4104
C7 IOBU7+
C5 IOBU5+
A6 IOBU2+
A5 IOBU1+
R30 4308-R-101-104
R29
4308-R-101-104
DATA/ADDRESS BUS
D2
P8155
RAM
I/O
TIMER
RAM
256x8
SLRAM
ALE
RD–
WR–
RESET+
TIMER IN
TIMER OUT
TRAP+
PA6
PA4
PA3
PA0
PA7
PA5
PA2
PA1
PC5
PC4
PC3
PC1
PB6
PB4
PB7
PB1
PB0
PC2
PB3
PB5
PB2
PC0
LEDON+
D16
HEF4104
BUSYL+
SELB1+
R28
4308-R-101-104
D20
HEF4104
XA
MCOLB+ C27
MCOLD+ C29
MCOLA+ C26
STEP2– A28
INTR2– C14
SELB2+
R9
511k
C23
100n
D5
HEF4528
Δt≈20ms
D17
HEF4104
MOTHS+ C25
MCOLC+ C28
DEGRM–
DEGRM+ A27
SELB0+
R11
R10
V3
BC547B
FIG.2
RD5485
850619

Figure 4.28 Goniometer Control Card, Schematic Figure 1

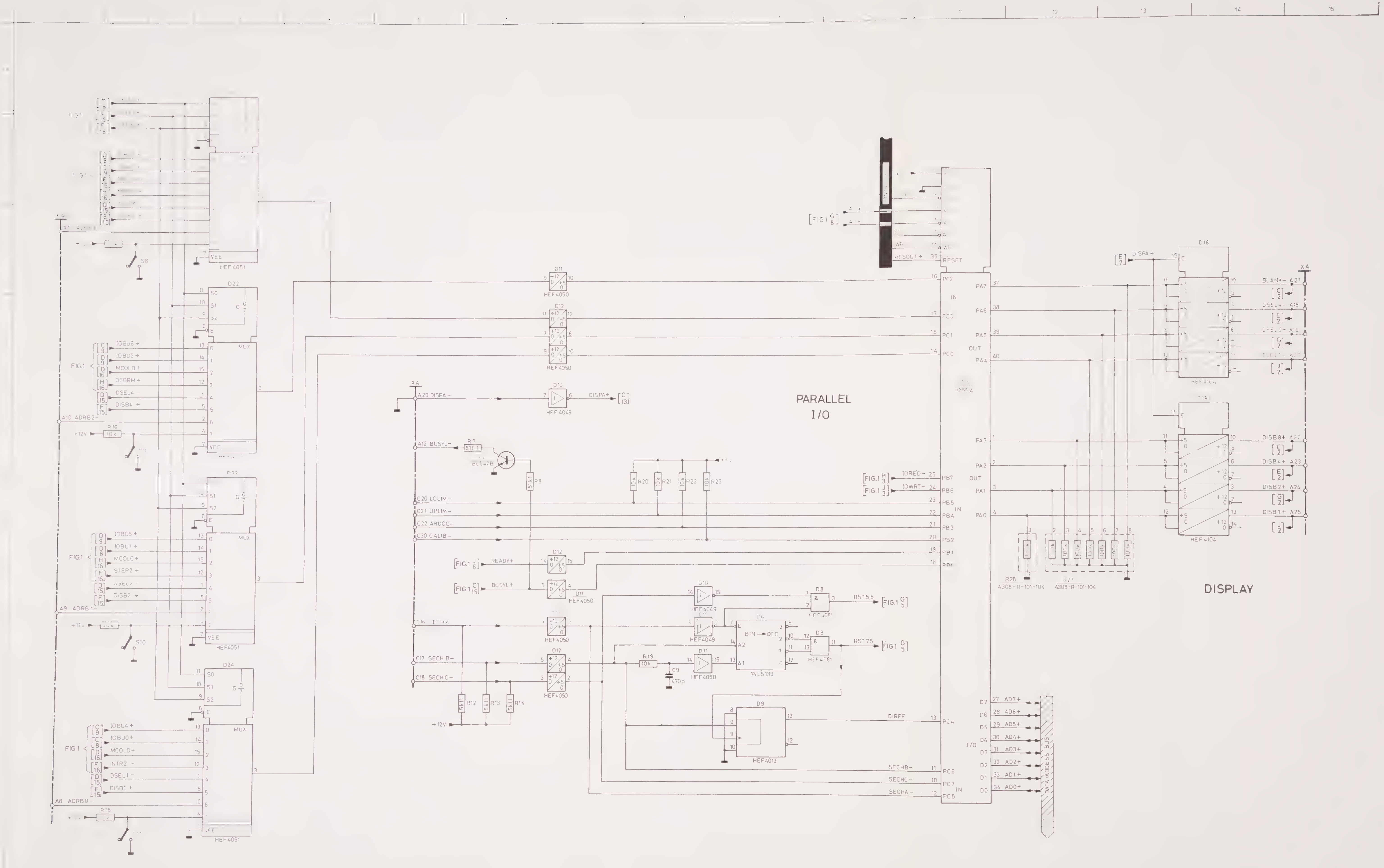

PARALLEL
I/O
DISPLAY
HEF4051
HEF4050
HEF4049
HEF4081
HEF4013
HEF4104
74LS139
D9
D10
D11
D12
D18
D22
D23
D24
MUX
BIN → DEC
IN
OUT
I/O
RESET
PA7
PA6
PA5
PA4
PA3
PA2
PA1
PA0
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
D7
D6
D5
D4
D3
D2
D1
D0
AD7+
AD6+
AD5+
AD4+
AD3+
AD2+
AD1+
AD0+
DATA/ADDESS BUS
BLANK− A21
DSEL4− A18
DSEL2− A19
DSEL1− A20
DISB8+ A22
DISB4+ A23
DISB2+ A24
DISB1+ A25
DISPA+
XA
A29 DISPA−
A12 BUSYL−
BC547B
C20 LOLIM−
C21 UPLIM−
C22 ARDOC−
C30 CALIB−
READY+
BUSYL+
C16 SECH A
C17 SECH B−
C18 SECH C−
SECHB−
SECHC−
SECHA−
DIRFF
IORED−
IOWRT−
RST5.5
RST7.5
R8
R12
R13
R14
R16
R18
R19
R20
R21
R22
R23
R28
4308-R-101-104
C9
470p
10k
+12V
S8
S10
A10 ADRB2−
A9 ADRB1−
A8 ADRB0−
IOBU6+
IOBU2+
MCOLB+
DEGRM+
DSEL4−
DISB4+
IOBU5+
IOBU1+
MCOLC+
STEP2+
DSEL2−
DISB2+
IOBU4+
IOBU0+
MCOLD+
INTR2−
DSEL1−
DISB1+
FIG.1
VEE
RD5486
850619

Figure 4.29 Goniometer Control Card, Schematic Figure 2

4.7 STEPPING MOTOR SUPPLY DRIVER

4.7.1 INTRODUCTION

This card provides power for the stepping motor under the control of the GONIOMETER CONTROL CARD. To do this, the following functions are provided on the card:

1. Supply
2. Coil control
3. Voltage control
4. Spike suppression

The schematic diagram for this card is shown in figure 4.31, and the layout is given in figure 4.30.

4.7.2 SUPPLY

Two AC voltages - one for the stepping motor at rest or low-speed, and another one for high speeds - are full-wave rectified by V17 and V18 for -5V, and V19 and V20 for -20V.

The motor supply voltage is available between MOTOR+ and MOTOR- (the collector of transistor V11). When MOTHV+ = LOW, this transistor is turned off, cutting off the -20V supply, therefore only the -5V is available at MOTOR- via diode V16.

4.7.3 COIL CONTROL

Transistors V6 to V9 switch the motor coils ON and OFF. All the coils have one common connection MOTOR-.

When MCOLA+ (logic level) = LOW, transistors V1 and V6 are turned OFF. Therefore coil A will not be energised. When MCOLA+ = HIGH, transistors V1 and V6 are turned ON. Therefore the nominal current will flow through coil A.

The same principle applies for motor coils B, C and D.

4.7.4 VOLTAGE CONTROL

When MOTHV+ = HIGH, transistors V5, V10 and V11 are turned ON, and the -20V is connected to MOTOR-. The -5V is blocked by diode V16 which is reverse biased.

This -20V is only allowed for a fast moving motor (only then the current per coil will not reach its final value, which would destroy the windings).

4.7.5 SPIKE SUPPRESSION

Diodes V12 to V15 protect transistors V6 to V9 from being destroyed by over-voltage. When any motor coil is switched OFF, a negative peak voltage is generated by that coil. Capacitor C5 reduces this peak (the capacitor is charged). During the time between the peaks, the capacitor discharges through resistors R19 and R20.

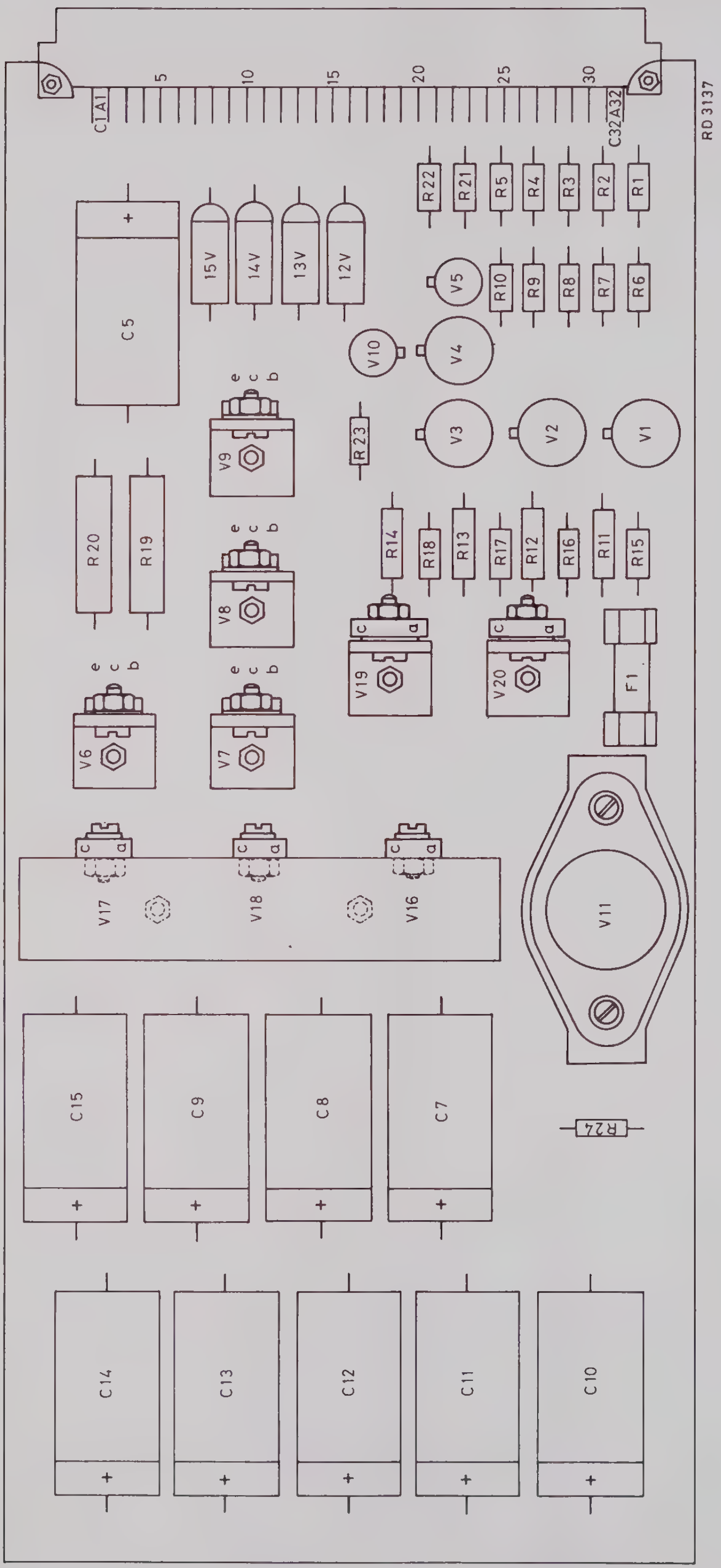

C1A1
5
10
15
20
25
30
C32A32
RD3137
R22
R21
R5
R4
R3
R2
R1
C5
15V
14V
13V
12V
V5
R10
R9
R8
R7
R6
V10
V4
e c b
V9
R23
V3
V2
V1
R20
R19
R14
R18
R13
R17
R12
R16
R11
R15
V8
c b
V19
V20
F1
V6
V7
V17
V18
V16
V11
C15
C9
C8
C7
R24
C14
C13
C12
C11
C10

Figure 4.30 Stepping Motor Supply Driver Card, Layout

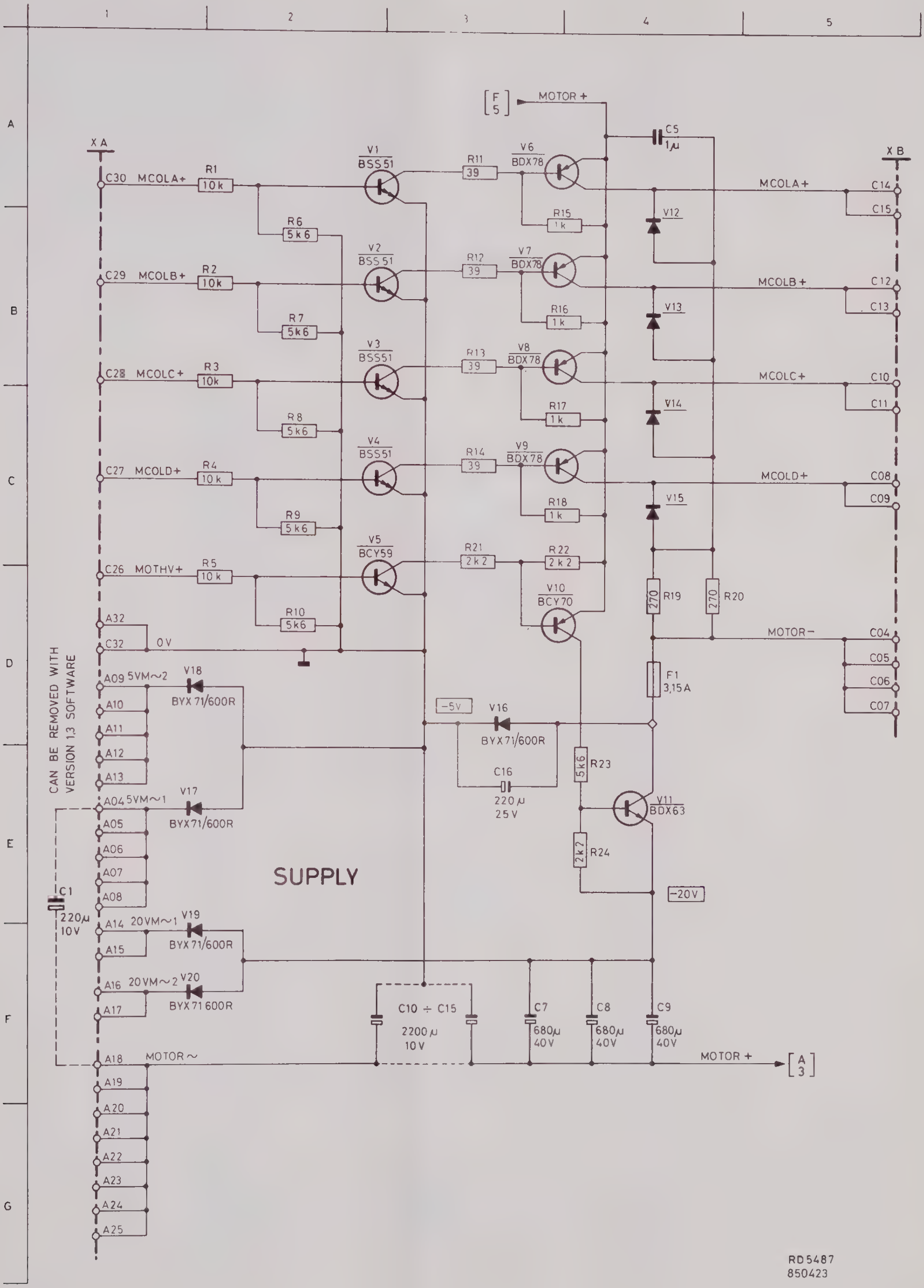

1
2
3
4
5
A
B
C
D
E
F
G
XA
XB
F 5
MOTOR +
C5 1µ
C30 MCOLA+
C29 MCOLB+
C28 MCOLC+
C27 MCOLD+
C26 MOTHV+
R1 10k
R2 10k
R3 10k
R4 10k
R5 10k
R6 5k6
R7 5k6
R8 5k6
R9 5k6
R10 5k6
V1 BSS51
V2 BSS51
V3 BSS51
V4 BSS51
V5 BCY59
R11 39
R12 39
R13 39
R14 39
R21 2k2
R22 2k2
V6 BDX78
V7 BDX78
V8 BDX78
V9 BDX78
V10 BCY70
R15 1k
R16 1k
R17 1k
R18 1k
V12
V13
V14
V15
R19 270
R20 270
MCOLA+
MCOLB+
MCOLC+
MCOLD+
MOTOR−
C14
C15
C12
C13
C10
C11
C08
C09
C04
C05
C06
C07
F1 3,15A
A32
C32 0V
A09 5VM~2
A10
A11
A12
A13
V18 BYX 71/600R
A04 5VM~1
V17 BYX71/600R
A05
A06
A07
A08
CAN BE REMOVED WITH VERSION 1.3 SOFTWARE
C1 220µ 10V
A14 20VM~1
V19 BYX 71/600R
A15
A16 20VM~2
V20 BYX71 600R
A17
A18 MOTOR ~
A19
A20
A21
A22
A23
A24
A25
SUPPLY
−5V
V16 BYX71/600R
C16 220µ 25V
R23 5k6
R24 2k7
V11 BDX63
−20V
C10 ÷ C15 2200µ 10V
C7 680µ 40V
C8 680µ 40V
C9 680µ 40V
MOTOR +
A 3
RD5487
850423

Figure 4.31 Stepping Motor Supply Driver Card, Schematic

4.9 WINDOW CONTROL CARD

4.9.1 INTRODUCTION

The WINDOW CONTROL CARD is the interface between the XRA-bus and the AMPLIFIER ANALYZER CARD. It is part of the counting channel card set. Its main function is to generate the two analogue levels for the pulse height discriminator. In addition, it generates a number of digital signals to control the operation of the AMPLIFIER ANALYZER CARD. To do that the following functions are provided on the card:

- Address decoder
- Lower level Digital-to-Analogue Converter (DAC)
- Window digital-to analogue converter
- Analogue adder
- Control circuitry

Some circuits are not used by the the PW1710 (divide-by 90/8, display output and some control signals). The schematic diagram for this card is shown in figure 4.36, and the layout is given in figure 4.35.

4.9.2 ADDRESS DECODER [A-2]

Data can only be written to this card, no data can be read from it.

Decoder D19 [A-1] is only enabled if IOWRT- is LOW. Only then can the four module address lines be decoded into a "card selected" signal for D33-1 [B-4]. The wiring is such that at module address 4 (in hexadecimal code), D33-1 is LOW. Two of the bytes address lines are then decoded into dedicated "write byte" lines. Table 4.9 shows the memory map of this card.

Table 4.9 Window Control Card Memory Map

BYTE ADDRESS	FUNCTION
1	Window DAC
2	Lower level DAC (tens and units)
3	Lower level DAC (tenths) and control

4.9.3 LOWER LEVEL DAC [M-10]

Data for the lower level DAC consists of 12 bits in BCD. The tens and units are contained in one byte, and are clocked into data registers D22 [E-6] and D21 [G-6]. There are two ways of changing the register contents:

> The first is by writing data in from the data bus, the data is contained in WRITE BYTEs 2 and 3.
>
> The second is to count the pulses coming from the divide-by-90/8 circuit.

The registers for the tenths, the units and the tens are cascaded. The pulses coming from the divide-by-90/8 circuit are counted in D20, D21 and D22. D20 generates a carry for D21, and D21 generates a carry for D22. This mechanism is not used in the PW1710, but the sequence of storing the bits for the lower level is important.

When the tenths register contents of the lower level DAC is "9" and the value is replaced by any value not equal to 9, this register will generate a carry to the units register, which will be incremented by one. Therefore, writing to the lower level register should have the following sequence: first write the tenths, after that write the units and tens.

The information is carried in the WRITE BYTEs in the following manner:

WRITE BYTE 2: lower level setting (tens and units) (in % F.S.)

Tens of lower level (in BCD)				Units of lower level (in BCD)			
L28	L24	L22	L21	L18	L14	L12	L11
BIT 8	BIT 4	BIT 2	BIT 1	BIT 8	BIT 4	BIT 2	BIT 1

A LOW on the CLEAR- line of the XRA-bus resets this register to zero.

The lower four bits (the tenths) and the control signals are contained in one byte, and are clocked into registers D20 [J-6] and D27 [L-6].

WRITE BYTE 3: lower level (tenths) (in % F.S.) + control

PHDIV	RECON *)	WWINF	PHDVR *)	Tenths of lower level (in BCD)			
				L08	L04	L02	L01
0 = ON	1 = ON	1 = ON	1 = ON	BIT 8	BIT 4	BIT 2	BIT 1

A LOW on the CLEAR- line of the XRA-bus resets this register to zero. The twelve output bits of the lower level register are connected to a hybrid digital-to-analogue converter. Analogue switching arrays in D12 to D15 [M-10 to H-10] switch resistor networks such that D4 (tens), D3 (units) and D2 (tenths) [H-12 to L-12] attenuate a reference voltage UREF [D-4] (4V d.c.) proportional to the register contents.

The principle of operation for one decade of this DAC is shown in figure 4.33.

When bit 1 is ON, Vout = 1/20 x Vref }
When bit 2 is ON, Vout = 2/20 x Vref }
When bit 4 is ON, Vout = 4/20 x Vref }
When bit 8 is ON, Vout = 8/20 x Vref }

When more than one bit is ON at a time, the results will be summed.

Therefore any bit pattern on the input of the switch array results in an analogue voltage proportional to the bit pattern.

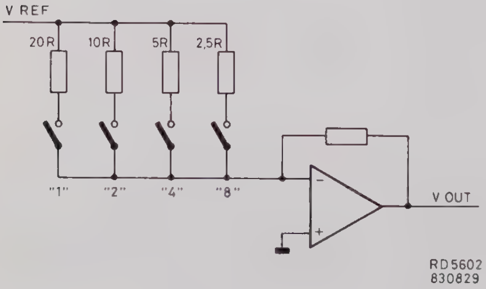


Figure 4.33 Single Decade

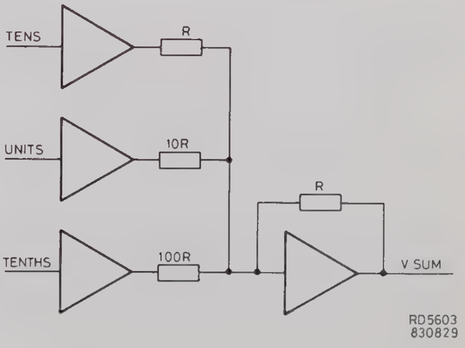


Figure 4.34 Attenuators

The three decades are summed by D5 [G-13], and at the same time, the "units" voltage is attenuated by 10 and the "tenths" voltage is attenuated by 100 (refer to figure 4.34). D11 and V3 [G-14] provides this voltage LWLEV on output pin C22 with sufficient output power. The output voltage can be adjusted by R1 of the reference voltage generator.

A 100 mV d.c. full scale output is available on pin C19. This voltage can be adjusted by R47 (and has to be readjusted each time the lower level has been adjusted).

4.9.4 WINDOW DAC [A-12]

The window DAC operates identically to the lower level DAC. Register D25 [B-6] and D24 [D-6] will hold the 8 bit BCD window value, once it has been stored. The window information is contained in WRITE BYTE 1 as follows:

WRITE BYTE 1: Window setting (in % of full scale)

Tens of window (in BCD)				Units of window (in BCD)			
W28 BIT 8	W24 BIT 4	W22 BIT 2	W21 BIT 1	W18 BIT 8	W14 BIT 4	W12 BIT 2	W11 BIT 1

A LOW on the CLEAR- line of the XRA-bus resets this register to zero.D7 [C-12] and D6 [E-12] generate the voltage for the tens and the units respectively. D8 [C-13] sums the two decades.

4.9.5 ADDER [C-14]

To develop an upper level voltage, the window voltage and the lower level voltage have to be added together. This two-stage generation of the upper level has been chosen to meet accuracy requirements.

D9 [D-14] adds the two voltages and both D10 and V2 provide the necessary output power. The output voltage can be adjusted using R33 (it must be readjusted each time the lower level has been adjusted).

4.9.6 CONTROL [M-15]

Four control bits are available, and two of them are not used in the PW1710.

WRITE BYTE 3: lower level (tenths) (in % F.S.) + control

PHDIV	RECON *)	WWINF	PHDVR *)	Tenths of lower level (in BCD)			
0 = ON	1 = ON	1 = ON	1 = ON	BIT 8	BIT 4	BIT 2	BIT 1

*) not used in the PW1710.

PHDIV Pulse height division. When this bit is TRUE, the automatic pulse shift correction on the AMPLIFIER ANALYZER CARD will maintain the correction level it had at the moment at which this bit became TRUE.

WWINF Window infinite. When this bit is TRUE, the AMPLIFIER ANALYZER CARD will ignore the upper level, and all pulses with a height, equal to or greater than the lower level, will be accepted.

D31, D35 [J-14], V6 and V7 [L-16] provide the necessary output power.

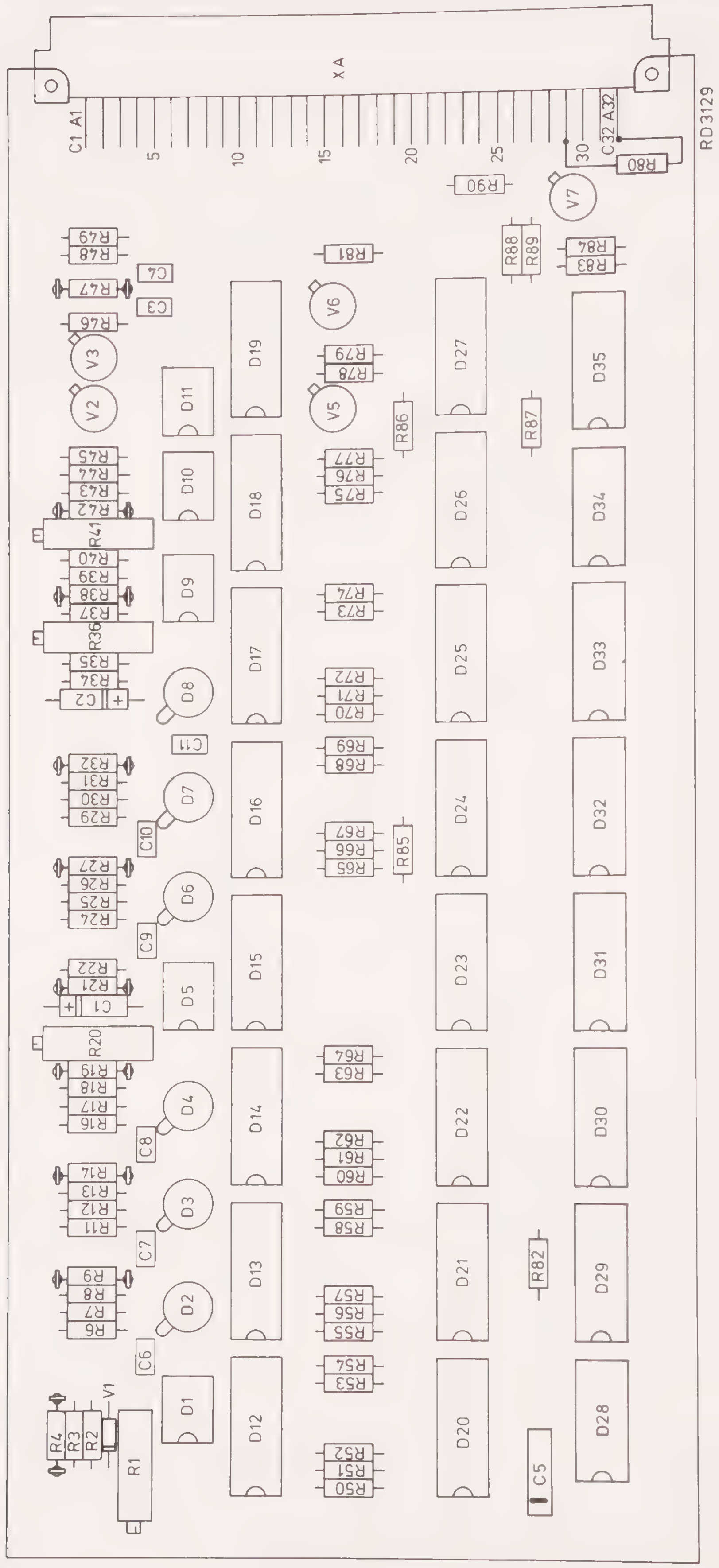

XA
C1 A1
5
10
15
20
25
30
C32 A32
RD3129
R80
R90
V7
R88
R89
R84
R83
R81
R49
R48
C4
R47
C3
R46
V6
D19
D27
D35
V3
R79
R78
V2
D11
V5
R86
R87
R45
R44
R43
R42
R41
D10
D18
R77
R76
R75
D26
D34
R40
R39
R38
R37
D9
R74
R73
R36
D17
D25
D33
R35
R34
R72
R71
R70
C2
D8
C11
R69
R68
R32
R31
R30
R29
D7
C10
D16
R67
R66
R65
R85
D24
D32
R27
R26
R25
R24
D6
C9
D15
D23
D31
R22
R21
C1
D5
R20
R64
R63
R19
R18
R17
R16
D4
C8
D14
D22
D30
R62
R61
R60
R14
R13
R12
R11
D3
R59
R58
C7
D13
D21
R82
D29
R9
R8
R7
R6
D2
R57
R56
R55
C6
R54
R53
V1
R4
R3
R2
D1
D12
D20
D28
R1
R52
R51
R50
C5

Figure 4.35 Window Control Card, Layout

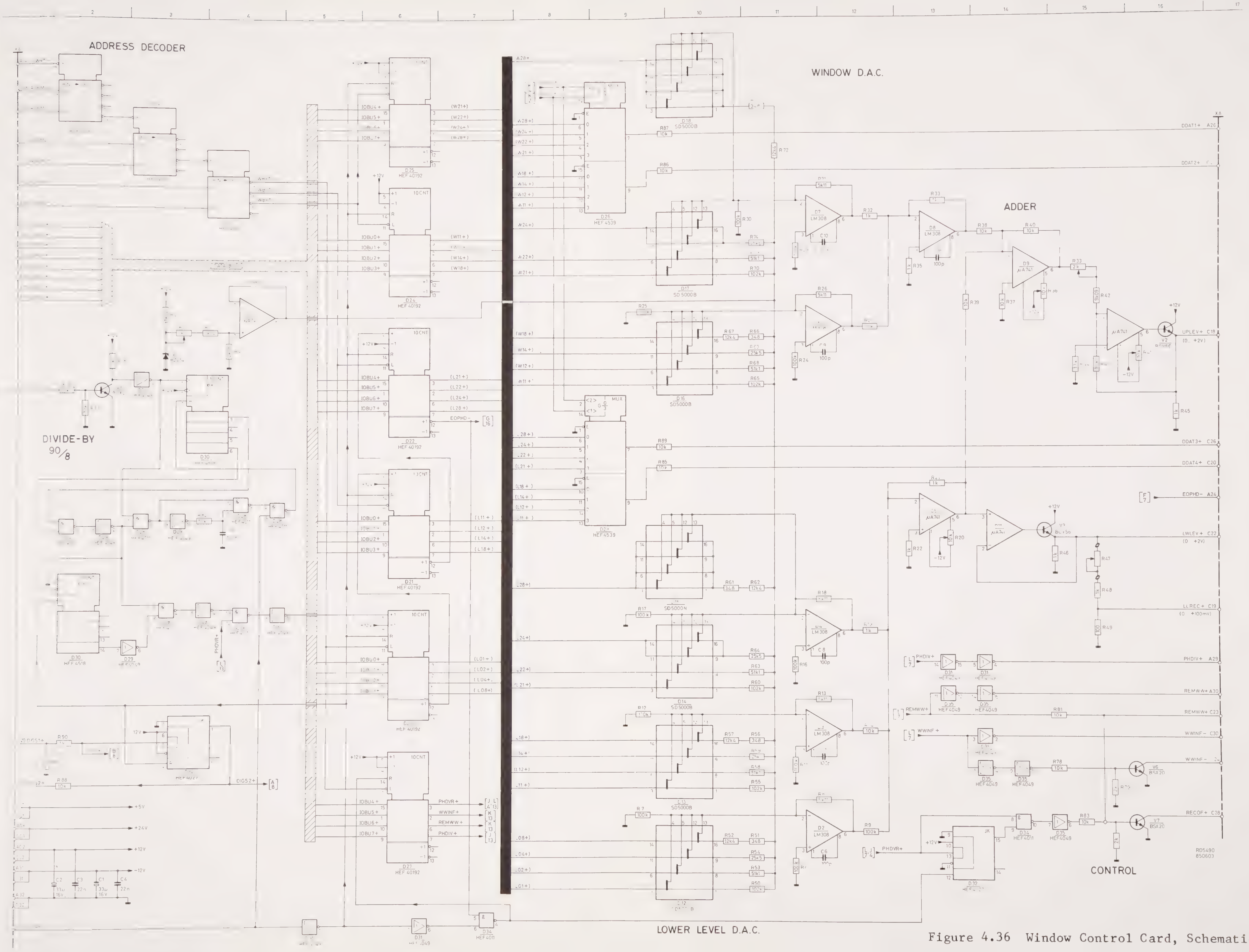

ADDRESS DECODER
WINDOW D.A.C.
ADDER
DIVIDE-BY 90/8
LOWER LEVEL D.A.C.
CONTROL
D25 HEF40192
D24 HEF40192
D22 HEF40192
D21 HEF40192
D27 HEF40192
D26 HEF4539
D23 HEF4539
MUX
D18 SD5000B
D17 SD5000B
D16 SD5000B
D14 SD5000B
D13 SD5000B
D7 LM308
D8 LM308
D9 μA741
D30 HEF4518
D29 HEF4049
D31 HEF4049
D34 HEF4011
D35 HEF4049
D32
DDAT1+ A26
DDAT2+
DDAT3+ C26
DDAT4+ C20
EOPHD- A24
UPLEV+ C18
(0 ... +2V)
LWLEV+ C22
(0 +2V)
LLREC+ C19
(0 +100mV)
PHDIV+ A29
REMWW+ A30
REMWW+ C23
WWINF- C30
RECOF+ C28
V6 BSX20
V7 BSX20
PHOVR+
WWINF+
REMWW+
PHDIV+
EOPHD-
DIG52+
+5V
+24V
+12V
-12V
RD5490
850603

Figure 4.36 Window Control Card, Schematic

4.9

4.10 AMPLIFIER ANALYSER CARD

4.10.1 INTRODUCTION

The amplifier/analyser card performs several functions. These functions are:

1. It corrects for pulse shift which occurs at high count rates. (Over approximately 5 000 c/s).
2. It amplifies the pulses by a predetermined amount (x 100).
3. It provides a pulse height analyser in the form of variable upper and lower level settings (thresholds).
4. It converts incoming pulses from an analogue to a digital form.
5. It introduces a correction for dead-time losses.

The schematic diagram for this card is shown in figure 4.41, and the layout is given in figure 4.40.

4.10.2 CORRECTION AMPLIFIER

Analogue pulses (DETS1) from the detector pre-amplifier are fed to a correction amplifier where they are multiplied by two correction factors, "A" and "B".

Correction factor "A" [C-4] is a value which depends on the position of the ATT. and TUBE switches S4 and S5 on the Secondary Control Panel [G-19]. The reference voltage for this circuit is situated on V8, D23 [B-13].

Correction factor "B" [D-5] is a factor which compensates for the shift in pulse amplitude which occurs at high count rates, and effectively results in the mean pulse height being adjusted to the ideal level.

During calibration, the detector high voltage and the amplifier attenuation mustbe adjusted so that the whole span of the pulse shift correction is available for use. This is arranged by switching the pulse shift correction circuit out and substituting a fixed value of -4V via V36, R90, R91 and D16 [D-29]. The correction range available is -10% to + 100% of this fixed value (that means -3,5V to -8.5V).

In a similar way, the correction factor "B" is fixed at -4V for low count rates via D16-7 [C-27]. At low countrates the outputs of D25 and D26 [C,D-26] are so low that when they are added D17 will switch FET D36 on, which allows the -4V from D16 to be connected to the correction amplifier.

During automatic pulse height distribution scans, the pulse shift correction circuit is also switched off, but in this case factor "B" is a voltage level derived from the previous measurement and stored in capacitors C4 and C5 [E-3].

4.10.3 100X AMPLIFIER AND ZERO LINE RESTORER

The pulses from the correction amplifier [B-7] (pulses multiplied by "A" and "B") are fed to the two-stage 100x amplifier. The amplification factor is given by R17/R10 and R24/R20 [B-7,8 and D-9,10].

This amplifier is also provided with a zero line restorer D16 and D21 and so on [E-8, E-11]. If, at the output of the amplifier the pulses are superimposed on a d.c. level (that means that they are not referred to the correct zero level), it is important that this is corrected.

One side of capacitor C12 is maintained at earth potential by the "ideal diode" formed by V5 and D21. The pulses only pass C12 while a d.c. level appears accross C12. This d.c. level is fed back to the input of the amplifier via the integrator D16, the filter R34, C16, and the jumper B, where it is subtracted from the input pulse. Thus the pulse is effectively referred to the original zero value.

4.10.4 PULSE SHIFT CORRECTION

Pulses leaving the amplifier are fed to the pulse shift correction circuit. This circuit consists of two "windows", one above the other with one common level. The common level is arranged to be at 50% of the range of the analyser, so that when the mean pulse height is also at 50% of the range, exactly half of the pulses leaving the amplifier will pass through each of the "windows". The pulses passing each window are fed to a ratemeter, and the outputs of the ratemeters D25 and D26 [C/E-25] are compared. If the two outputs are not equal at the input to the difference amplifier D16 then the current sources V33 or V34 are activated, changing the charge on capacitors C4 and C5 [E-3] via V35. This results in a change in factor "B".

If the CALIBRATE push-button is pressed this results in signal CALBR- = 0, fixing factor "B" at -4V via V36 [D-14]. At low countrates factor "B" is also fixed at -4V via the difference amplifier D16-7.

When an automatic pulse height distribution is being made, signal PHDIV+ = 1 causes the whole pulse shift correction circuit to be switched out via V37 and V35 [H-30]. The correction voltage which applied to the previous measurement is used for correction, since this voltage is "remembered" by capacitors C4 and C5 [E-3].

4.10.5 PULSE HEIGHT ANALYSER

Pulses leaving the amplifiers are passed to the detector switches D19-1 and D19-9. These FET switches are controlled by signals SLDET1+ and SLDET2+.

There is a two position switch S1 on this card [L-2] which enables a 30kHz test signal (CLOCK) from the System Contract Card to be applied to the discriminator in place of the detector pulses.

The discriminator consists of two pairs of difference amplifiers, supplied with variable reference voltages from the Window Control Card. The reference voltages cause the difference amplifiers to act as thresholds, one representing the upper level and the other the lower level. A block diagram of one discriminator circuit is shown in figure 4.37 below.

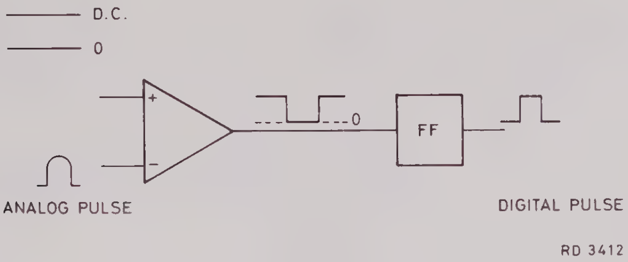


Figure 4.37 Discriminator Block Diagram

The pulse height analyser can operate in several different modes:

1. Usually only pulses of a particular energy level (wavelength) are required to be counted, for example, Cu k alpha. In this case, both discriminators are used, the pulses passing the upper level being subtracted from the pulses passing the lower level. The resultant pulses fed to the counter circuit are therefore only those which have a pulse height between the lower and upper levels (the so called "window").

2. If, for example, a scan is to be made, it is then normally required to count all pulses which pass the lower level (a "window").

3. A very narrow "window" (for example, 2% of the total window range) can be used to scan the whole pulse height range, the pulses passing the window being used to record the "pulse height distribution".

   Pulses passing the upper level, set the flip-flop D12-8 and D13-8, and after being delayed in D15-3 and D15-6 are presented to one input of D7-6. Pulses passing the lower level, set the flip-flop D12-11 and D13-12, trigger the deadtime one-shot D14, and are presented to the other input of D7-6. Owing to the built-in delays and the one-shot, these components act as an anticoincidence circuit, the only pulses passing D7-6 being those which are above the lower level and below the upper level, (therefore in the "window"). This delay is necessary because the lower level flip-flop is triggered earlier than that for the upper level. Refer to figure 4.39 Discriminator Pulse Diagram.

4.10.6 DEAD-TIME CORRECTION

For a short period after a pulse has been produced in a detector, the detector is effectively saturated and can not accept a further pulse. This is the so called "dead-time" of the detector, and varies slightly between detectors. For this reason a fixed dead-time, longer than that of the detector is built-in to the circuit. This dead-time is provided by a one-shot D14 [K-7] and is fixed at 300ns, this means: after a pulse has been accepted, no further pulse will be accepted for 300ns.

Since the production of X-ray quanta, and therefore detecting pulses, is a random process, provided sufficient pulses are counted, the number of pulses which occur during the dead-time can be calculated statistically. This number of pulses is produced in the dead-time correction circuit and added to the detector pulses to obtain the true countrate.

If it is assumed that all the pulses with pulse heights below the lower level are caused by noise (and can therefore be neglected), and if N_W = true countrate in the "window"

N_W1 = actual countrate in the "window"

N_{ll} = pulses with pulse heights above the lower level

τ = dead-time

then: The fraction of time for which the system is dead is:

$$N_{ll}\,\tau$$

(eg at 100 000 c/s, with τ = 300 ns, the system will be dead for 3% of the time),

and the fraction for which it will be open is

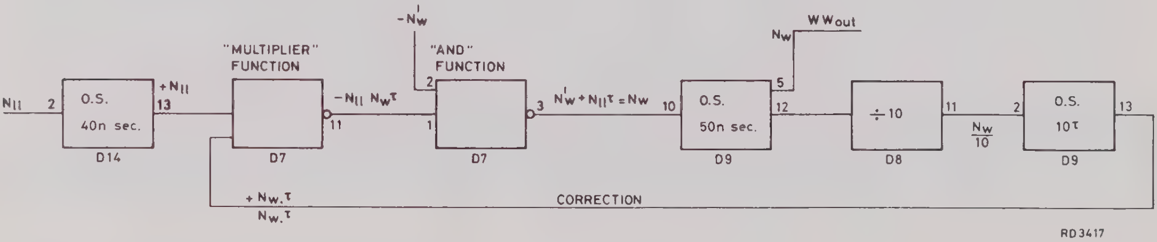
$$1-N_{ll}\tau$$

$$\text{So } N_W = \left(\frac{1}{1-N_{ll}\tau}\right) N_{W'}$$

$$= \frac{N_{W'}}{1-N_{ll}\tau}$$

$$= N_{W'} + N_{ll}\,N_W\,\tau$$

The corrected pulses (WWOUT) are fed to the ratemeter and counter circuits, figure 4.38 shows this.



$-N_W'$
"MULTIPLIER" FUNCTION
"AND" FUNCTION
N_W
WWout
N_{ll}
2
O.S.
40n sec.
13
$+N_{ll}$
D14
D7
$-N_{ll}\,N_W\tau$
11
2
1
D7
3
$N_W' + N_{ll}\tau = N_W$
10
O.S.
50n sec.
5
12
D9
÷10
D8
11
$\frac{N_W}{10}$
2
O.S.
10τ
13
D9
$+N_W.\tau$
$N_W.\tau$
CORRECTION
RD3417

Figure 4.38 Deadtime Correction Block Diagram

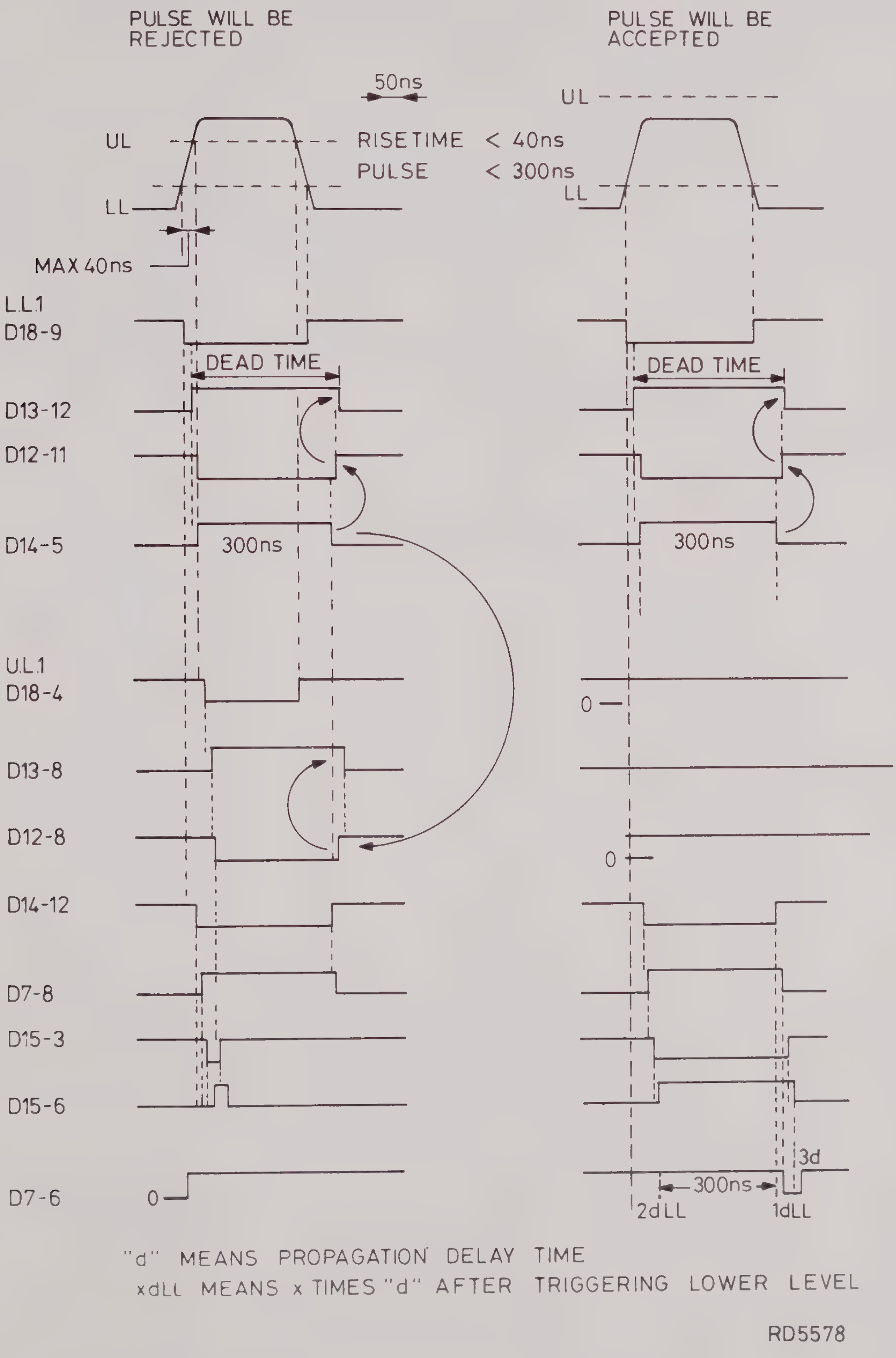

PULSE WILL BE REJECTED
PULSE WILL BE ACCEPTED
50ns
UL
LL
RISETIME < 40ns
PULSE < 300ns
MAX 40ns
L.L.1 D18-9
DEAD TIME
D13-12
D12-11
D14-5
300ns
U.L.1 D18-4
D13-8
D12-8
D14-12
D7-8
D15-3
D15-6
D7-6
0
3d
300ns
2dLL
1dLL
"d" MEANS PROPAGATION DELAY TIME
xdLL MEANS x TIMES "d" AFTER TRIGGERING LOWER LEVEL
RD5578

Figure 4.39 Discriminator Circuit Pulse Diagram

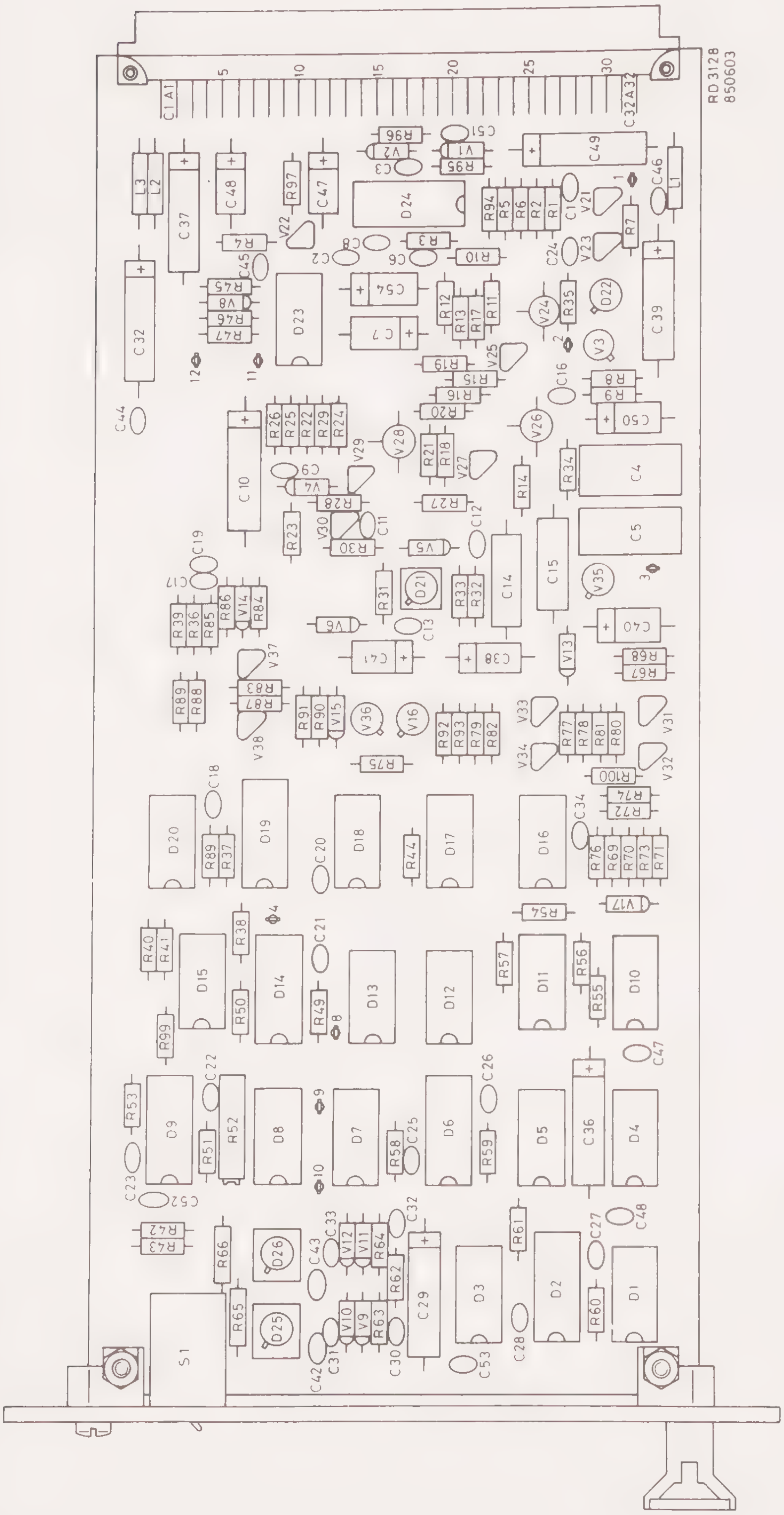
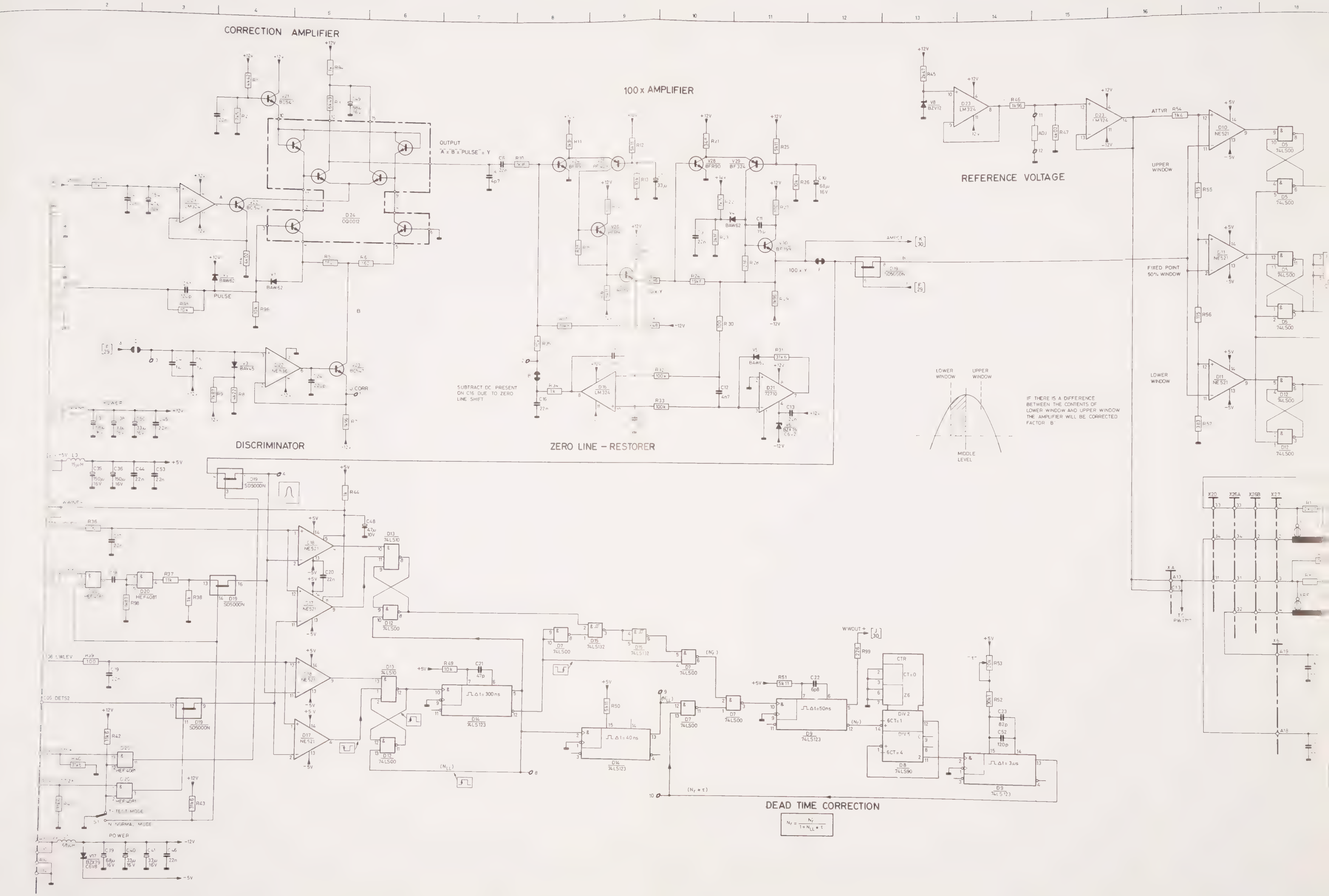

RD 3128
850603
C1 A1
5
10
15
20
25
30
C32 A32
S1
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
D19
D20
D21
D22
D23
D24
D25
D26
C37
C32
C10
C39
C49
C4
C5
C14
C15
C29
C36
L1
L2
L3

Figure 4.40 Amplifier Analyzer, Layout


2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
CORRECTION AMPLIFIER
D24
OQ0012
OUTPUT
"A" x "B" x "PULSE" = Y
BC547
BAW62
PULSE
R96
B
LM324
100 x AMPLIFIER
BFR90
BF324
BF199
BAW62
AMPLT
100 x Y
SD5000N
REFERENCE VOLTAGE
D23
LM324
BZV12
R45
R46
1k96
R47
ADJ
ATTVR
R54
1k4
UPPER WINDOW
FIXED POINT 50% WINDOW
LOWER WINDOW
D10
NE521
D11
NE521
D5
74LS00
D4
74LS00
D12
74LS00
R55
R56
R57
LOWER WINDOW
UPPER WINDOW
MIDDLE LEVEL
IF THERE IS A DIFFERENCE
BETWEEN THE CONTENTS OF
LOWER WINDOW AND UPPER WINDOW
THE AMPLIFIER WILL BE CORRECTED
FACTOR B
DISCRIMINATOR
D22
NE536
BAV45
U CORR
SUBTRACT DC PRESENT
ON C16 DUE TO ZERO
LINE SHIFT
C16
22n
ZERO LINE – RESTORER
D16
LM324
D21
72710
R33
100k
R30
R31
BZX79
C6V2
POWER
+12V
+5V
-12V
-5V
L3
15μH
C35
150μ 16V
C36
150μ 16V
C44
22n
C53
22n
D19
SD5000N
R44
C48
47μ 10V
D13
74LS10
D18
NE521
D17
NE521
C20
22n
D20
HEF4081
R37
11k
R38
R98
R36
R39
100
C19
R42
R43
D12
74LS00
HEF4081
T- TEST MODE
S1
N- NORMAL MODE
68μH
V17
BZX79
C6V8
C39
68μ 16V
C40
33μ 16V
C41
33μ 16V
22n
D7
74LS00
D15
74LS132
R49
10k
C21
47p
D14
74LS123
Δt = 300ns
R50
Δt = 40ns
(Nf)
(NLL)
(Nf = τ)
WWOUT+
R99
R51
5k11
C22
6p8
D9
74LS123
Δt = 50ns
CTR
CT=0
Z6
DIV 2
CT=1
DIV 5
CT=4
D8
74LS90
R53
R52
C23
82p
C52
120p
Δt = 3μs
DEAD TIME CORRECTION
$N_f = \frac{N_f}{1 + N_{LL} \cdot \tau}$
X20
X26A
X26B
X27
X4
A13
C13
TO PW17
X6
A19
A18

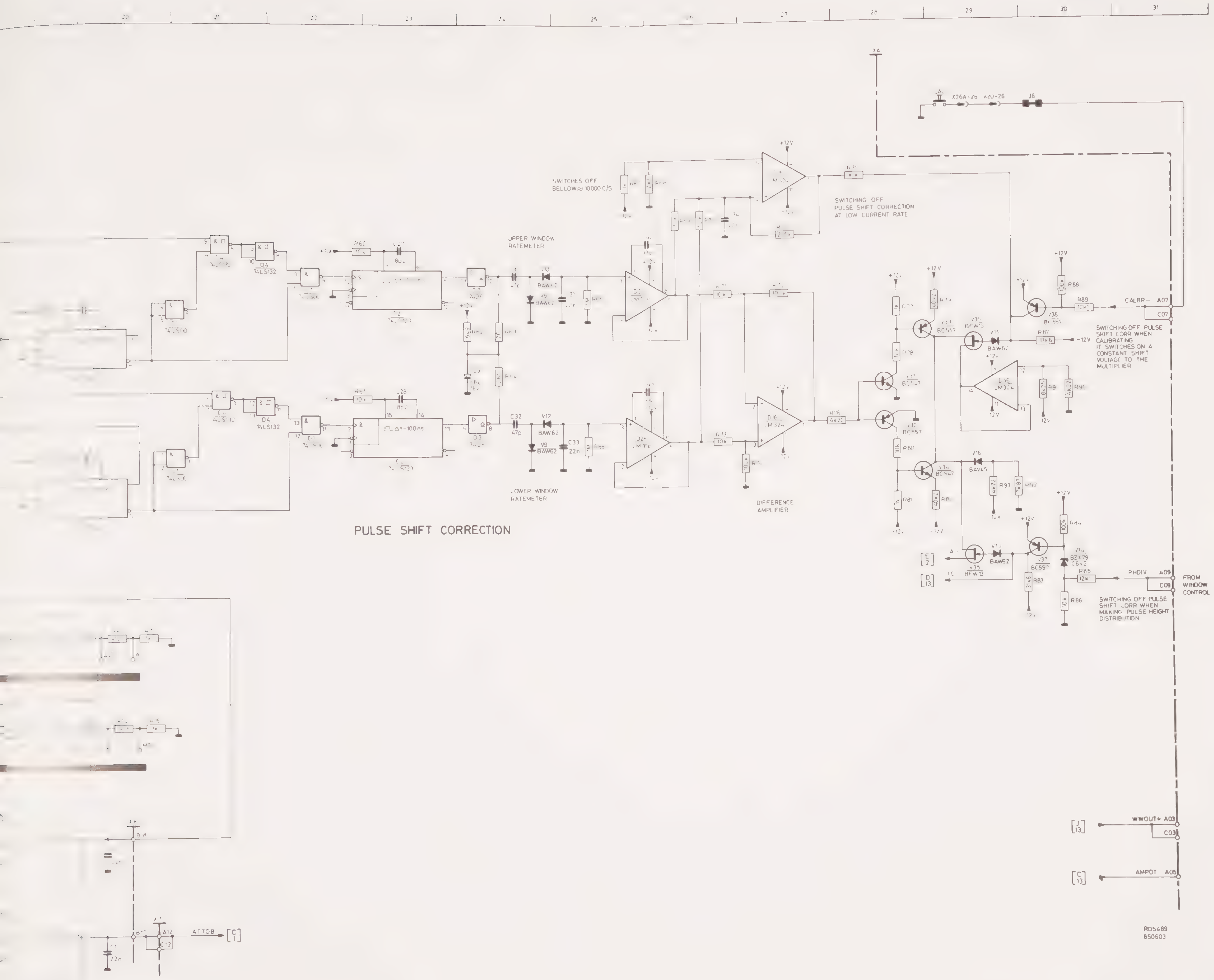

20
21
22
23
24
25
26
27
28
29
30
31
XA
X26A-26
X20-26
J8
+12V
SWITCHES OFF
BELLOW ≈ 10000 C/S
SWITCHING OFF
PULSE SHIFT CORRECTION
AT LOW CURRENT RATE
UPPER WINDOW
RATEMETER
R60
8p2
+5V
D4
74LS132
BAW62
V9
BAW62
+12V
R62
6k9
1M
D16
LM324
R76
4k22
R73
10k
10k
DIFFERENCE
AMPLIFIER
R28
8p2
15
14
13
12
Δt–100ns
D3
C32
47p
V12
BAW62
C33
22n
LOWER WINDOW
RATEMETER
PULSE SHIFT CORRECTION
R77
1k
R79
40k2
V33
BC557
V36
BFW13
V15
BAW62
R78
V31
BC547
V32
BC557
R80
10k
V34
BC547
R81
1k
R82
40k2
-12V
V16
BAV45
R93
4k22
R92
7k87
12V
V38
BC557
R88
100k
R89
12k1
CALBR–
A07
C07
R87
31k6
-12V
SWITCHING OFF PULSE
SHIFT CORR WHEN
CALIBRATING
IT SWITCHES ON A
CONSTANT SHIFT
VOLTAGE TO THE
MULTIPLIER
R91
8k25
R90
4k22
E
2
D
13
V35
BFW13
V13
BAW62
V37
BC557
R83
31k6
R84
100k
V14
BZX79
C6V2
R85
12k1
PHDIV
A09
C09
FROM
WINDOW
CONTROL
R86
10k
SWITCHING OFF PULSE
SHIFT CORR WHEN
MAKING PULSE HEIGHT
DISTRIBUTION
J
13
WWOUT+
A03
C03
C
13
AMPOT
A05
ATTOB
C
1
22n
A12
C12
RD5489
850603

Figure 4.41 Amplifier Analyzer, Schematic

4.11 FOUR DIGIT BINARY COUNTER

4.11.1 INTRODUCTION

This card stores pulses from the pulse height discriminator and presents the accumulated number to the XRA-bus controller. It is a pre-scaler for incoming pulses (WWOUT). Maximum input count rate is determined by WWOUT=LOW and WWOUT=HIGH > 10 ns. Maximum capacity is 65535 counts. To do this, the following functions are provided on the card:

- Address decoder (jumper selected)
- 16-bit binary counter
- Write control (START, STOP, RESET and CLEAR) circuits
- Read control (START and OVERFLOW indication) circuits

The schematic diagram for this card is shown in figure 4.43, and the layout is given in figure 4.42.

4.11.2 ADDRESS DECODER

The binary-to-decimal decoder D5 decodes the four bit module address into a card select signal, appearing at input D3-2 and D4-5. The address is jumper selectable. In the PW1710 the address is set to 6 (in hexadecimal code, that means: jumpers 2 and 7 closed). For the second counting channel option PW1748 the address is set to 1 hex (jumpers 3 and 8 closed).

4.11.3 16-BIT BINARY COUNTER

The 16-bit counter consists of a flip-flop (divider) and two 8-bit counting chips. This means a count of 17 in total. The output of the flip-flop is connected as the Least Significant output bit, and the output pin 14 from D7 (the 17th bit) is used as an overflow bit.

Input signal WWOUT has TTL-compatible levels. JK flip-flop D13 acts as the first stage of the 16-bit binary counter. For reasons of speed, this flip-flop uses Low-Power Schottky technology. To enable this stage both the J and K input must be HIGH. As the rest of the card uses 12V-logic, D9 converts D13´s TTL output into 12V logic level. This output from D13 is the count-up input for the cascaded counter ICs.

4.11.4 WRITE CONTROL

Four commands are available on this card. No particular byte address is assigned to the command word. When the card is addressed and IOWRT- goes LOW, the lower four bits contain the command code.

WRITE BYTE x (any byte number): command

X	X	X	X	RESOV	STPCT	SRTCT	RESCT

RESOV	A "1" means: Reset the overflow indicator to zero. This signal passes through D3 [E-3] and resets D6 [E-4].
STPCT	A "1" means: Disable the counting of WWOUT pulses. STPCT triggers D6, so the contents of the D-input (LOW) are copied to the output (SRTFF+ goes LOW).

SRTCT	A "1" means: Enable the counting of WWOUT pulses. STRCT uses the direct-set input of D6 [D-4] to set this flip-flop, and SRTFF+ goes HIGH. Via level converter D14, the J and K inputs of D13 go HIGH and the counter starts counting.
RESCT	A "1" means: Reset the counter (make its contents all zeros). This signal (RESCT+) is connected to the master reset input of each counter IC (D8 and D7), and via D14 to the direct-reset input of D13.

4.11.5 READ CONTROL

When "card select" is LOW (=TRUE) and IORED goes LOW (=TRUE), the decoder D1 is enabled and ADRB1- and ADRB0- are decoded into dedicated "read byte" signals (ADRB3- and ADRB2- are don´t cares).

4.11.5.1 Status

When ADRB1 = HIGH, and ADRB0 = LOW, RSTAT goes LOW and the status of the card can be read. Outputs of part of D10 [F-6] become active and drive the XRA-data bus.

READ BYTE 1: status

X	X	X	X	X	X	SRTFF	OVFFF

SRTFF	A "1" means: Start flip-flop. When set to "1", it is an indication that the counter is enabled to count pulses.
OVFFF	A "1" means: Overflow bit flip-flop. When bit 8 of the most significant nibble of counter D7 [E-5] goes HIGH, this is an indication that the counter´s capacity has been exceeded and the actual number of counted pulses is uncertain (there is no check on how many times this bit went HIGH and LOW).

4.11.5.2 Counter High Byte

When ADRB1 = LOW, and ADRB0 = HIGH, RCTHI- goes LOW and the contents of the upper eight bits of the counter can be read. Outputs of data buffers D11 [D-6] and D10 [F-6] become active and drive the XRA-data bus.

READ BYTE 2: counter contents, high byte

BIT15	BIT14	BIT13	BIT12	BIT11	BIT10	BIT 9	BIT 8

4.11.5.3 Counter Low Byte

When ADRB1 = LOW, and ADRB0 = LOW, RCTLO- goes LOW and the contents of the lower eight bits of the counter can be read. Outputs of data buffers D12 [B-6] and D11 [C-6] become active and drive the XRA-data bus.

READ BYTE 3: counter contents, low byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

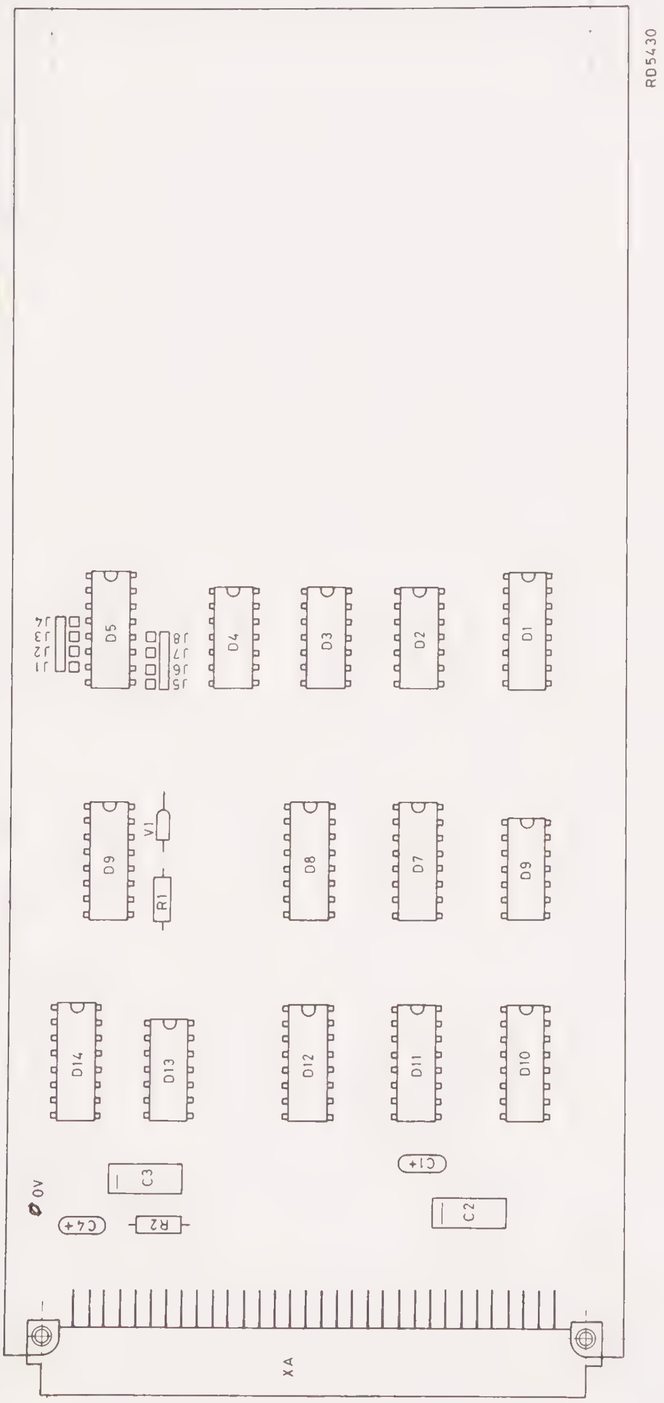

RD5430
J1
J2
J3
J4
D5
J5
J6
J7
J8
D4
D3
D2
D1
D9
V1
R1
D8
D7
D9
D14
D13
D12
D11
D10
C1+
C3
0V
C4+
R2
C2
XA

Figure 4.42 Four Digit Binary Counter Card, Layout

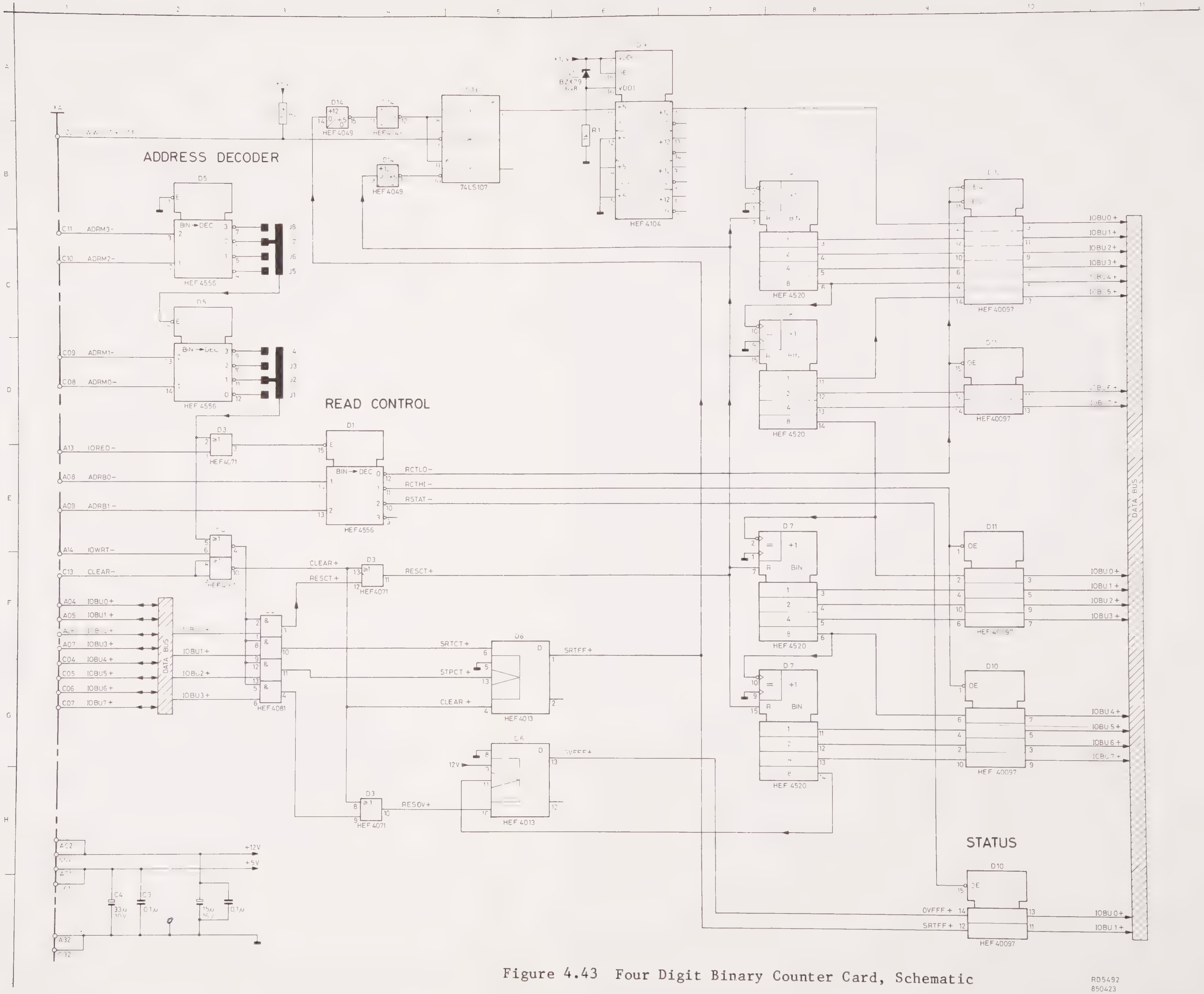

ADDRESS DECODER
READ CONTROL
STATUS
DATA BUS
D5
HEF 4556
BIN→DEC
C11 ADRM3-
C10 ADRM2-
C09 ADRM1-
C08 ADRM0-
J8
J6
J5
J3
J2
J1
D14
HEF4049
74LS107
HEF 4104
R1
D1
D3
HEF4071
A13 IORED-
A08 ADRB0-
A09 ADRB1-
A14 IOWRT-
C13 CLEAR-
RCTLO-
RCTHI-
RSTAT-
CLEAR+
RESCT+
A04 IOBU0+
A05 IOBU1+
A07 IOBU3+
C04 IOBU4+
C05 IOBU5+
C06 IOBU6+
C07 IOBU7+
HEF4081
D6
HEF4013
SRTCT+
STPCT+
SRTFF+
RESOV+
12V
D7
HEF 4520
D11
D10
OE
HEF 40097
IOBU0+
IOBU1+
IOBU2+
IOBU3+
IOBU4+
IOBU5+
IOBU6+
IOBU7+
OVFFF+
+12V
+5V
C4
C3
A32

Figure 4.43 Four Digit Binary Counter Card, Schematic

RD5492
850423

4.12 RATEMETER

4.12.1 INTRODUCTION

The ratemeter integrates the pulses from the amplifier/analyser for a period determined by the TIME CONSTANT. The resultant output can be displayed on an external Chart Recorder (100mV FSD, Ri > 100 k for 1% accuracy).

The range of the ratemeter is determined by information on the data bus (as a result of the RFS command). Although circuitry is provided for manual and automatic range setting, these facilities are not used in the PW1710/00.

The time constant of the ratemeter, which affects the chart recorder output, is set with the command RTC. The best setting for this depends on the countrate, the recorder chart speed, and the goniometer scanning speed.

Figure 4.44 shows a block diagram of the Ratemeter Card.

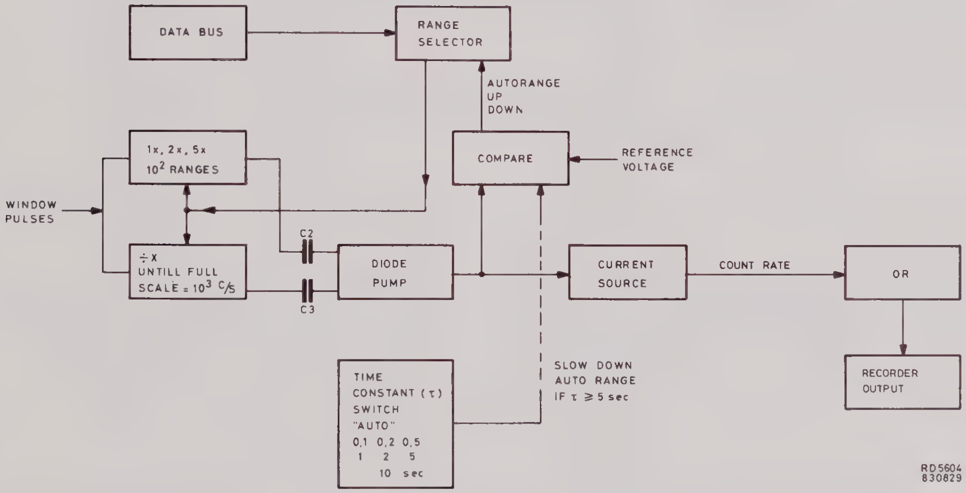

DATA BUS
RANGE SELECTOR
AUTORANGE UP DOWN
1x, 2x, 5x
10² RANGES
COMPARE
REFERENCE VOLTAGE
WINDOW PULSES
C2
÷X
UNTILL FULL SCALE = 10³ C/S
C3
DIODE PUMP
CURRENT SOURCE
COUNT RATE
OR
TIME CONSTANT (τ) SWITCH "AUTO"
0,1 0,2 0,5
1 2 5
10 sec
SLOW DOWN AUTO RANGE IF τ ≥ 5 sec
RECORDER OUTPUT
RD5604
830829

Figure 4.44 Ratemeter Block Diagram

The schematic diagram for this card is shown in figure 4.46, and the layout is given in figure 4.45.

4.12.2 MODULE ADDRESS DECODING

D5 [E-3] decodes the four module address lines into a card select signal when the address D85x is present and is enabled by the IOWRT signal. The IOWRT signal is also used to enable the REMOTE latch D6.

This card has no readable data from the selected ranges. The byte assignment of the card are as follows:

WRITE D85x Full Scale Settings (refer to table 4.10)

BIT 7	BIT 6	BIT 5	BIT 4	FULL SCALE SETTINGS			
				BIT 3	BIT 2	BIT 2	BIT 0

Table 4.10 Full Scale Settings

IOBU bit				HEX Value	RANGE	COMMENT
3	2	1	0			
0	0	0	0	0	Manual	Not used in PW1710/00
0	0	0	1	1	1.10^2	
0	0	1	0	2	2.10^2	
0	0	1	1	3	5.10^2	
0	1	0	0	4	Automatic	ranging not used in PW1710/00
0	1	0	1	5	1.10^3	
0	1	1	0	6	2.10^3	
0	1	1	1	7	5.10^3	
1	0	0	0	8	OFF	
1	0	0	1	9	1.10^4	
1	0	1	0	A	2.10^4	
1	0	1	1	B	5.10^4	
1	1	0	0	C	OFF	
1	1	0	1	D	1.10^5	
1	1	1	0	E	2.10^5	
1	1	1	1	F	5.10^5	

4.12.3 RANGE SELECTION

The data bits IOBU0 to IOBU3 are multiplexed by D3 and D4 [F-4] and the output lines A+ to D+ are connected to the range selector D9 [G-9]. The range selector signals called 1x (times 1), 2x, 5x and 10^2, 10^3, 10^4 and 10^5 determine how the input pulses must be divided to achieve a maximum of 10^3 counts per second at the input to the diode pump circuit V41, C5 [B-15] unless 10^2 was selected.

If 10^2 is selected, V5 [B-14] conducts and will switch on the FET V2. In this case the capacitance is increased by a factor of 10, which causes the range to be decreased from 10^3 to 10^2.

4.12.4 TIME CONSTANT SELECTION

The time constant can be manually selected between 0.1 seconds to 5 seconds in six steps weighted 1, 2, 5, or it can be automatic. The command for automatic mode is RTC S or F, and the command for manual is RTC x.

The time constant is set via the Recorder Control Card by the lines RTC10 to RTC.2 and RTCAU. If either of the commands RTC S or F have been given, the signal RTCAU is "low", and the time constant is set according to the "counting range" selected by the range selection circuits.

If RTCAU is not low, the time constant is set according to the lines RTC10 to RTC.2, if none of these lines are active, the time constant is set to .1 second and is determined by R13, R14 and R15 together with C5 [C-15]. To increase the time constant, the lines from the Recorder Control switch capacitors in parallel to C5 via the drive transistors V18 to V23, which control FET switches V35 to V40.

The output of the ratemeter (VU) at the junction of V41 and C5 [B-15] is connected to D19 which converts it to a current ouput of 0 - 100 uA which is then connected to the Recorder Control.

4.12.5 CALIBRATION

To display the output on the Chart Recorder you must give the command MAN.
In order to display several different ranges on the recorder, the pulse train is divided in such a way that the meter recorder displays full scale deflection for each range. The actual range in use is indicated in the parameter list (PAR). There is a slight difference in the way that the ranges $<10^3$ and $>10^3$ are calibrated, therefore the calibration must be done in two stages:

(a) Ranges $> 10^3$ c/s:

Select the value of R7 [B-16] to give full scale deflection.

(b) Ranges 1,2,5, 10^2 c/s:

Connect a suitable capacitor in parallel with C3 to give full scale deflection:

10pF/mV output on recorder (100 mV = full scale deflection). PM8203A.

10pF/10mV output on recorder (1000 mV = full scale defln). PM8210/31/32.

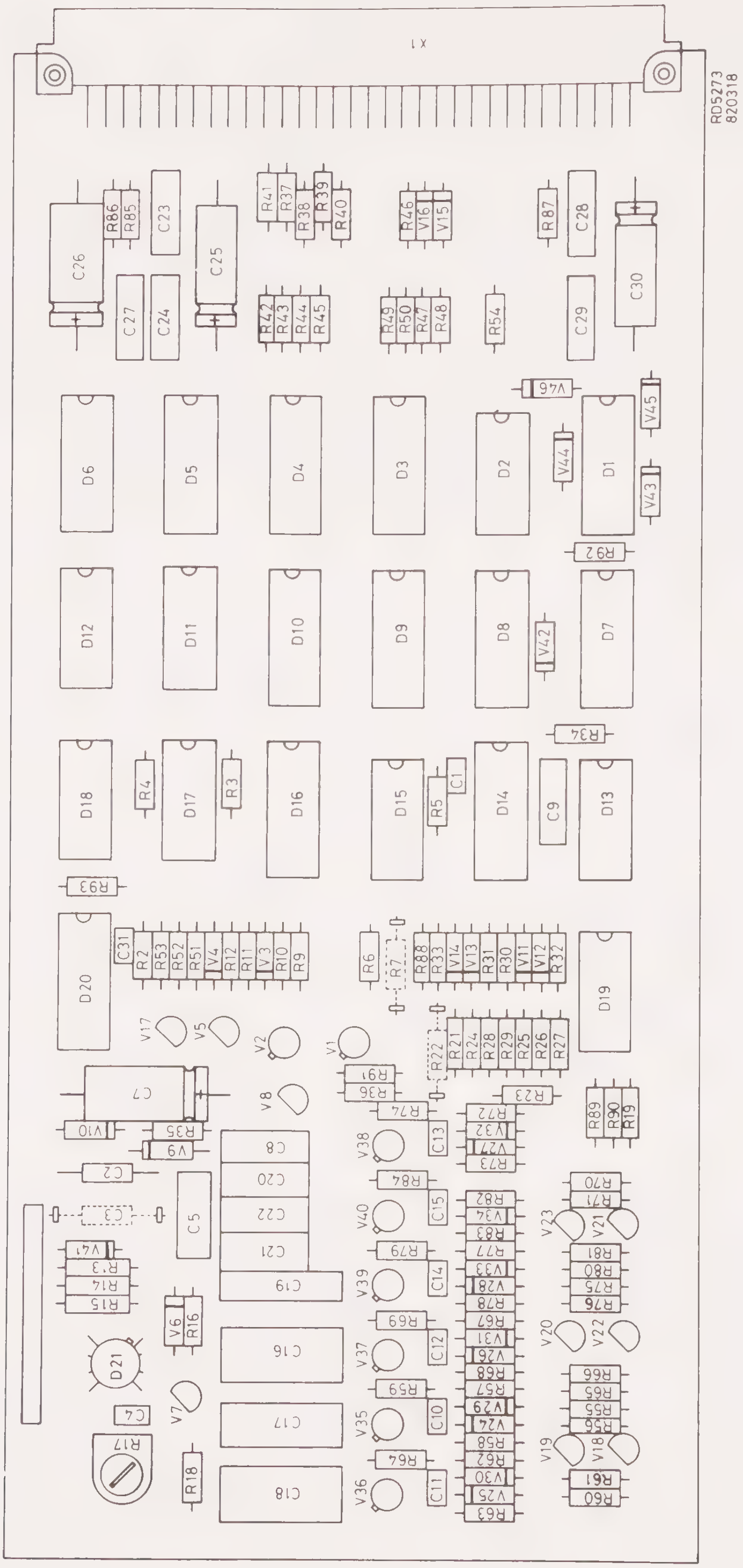
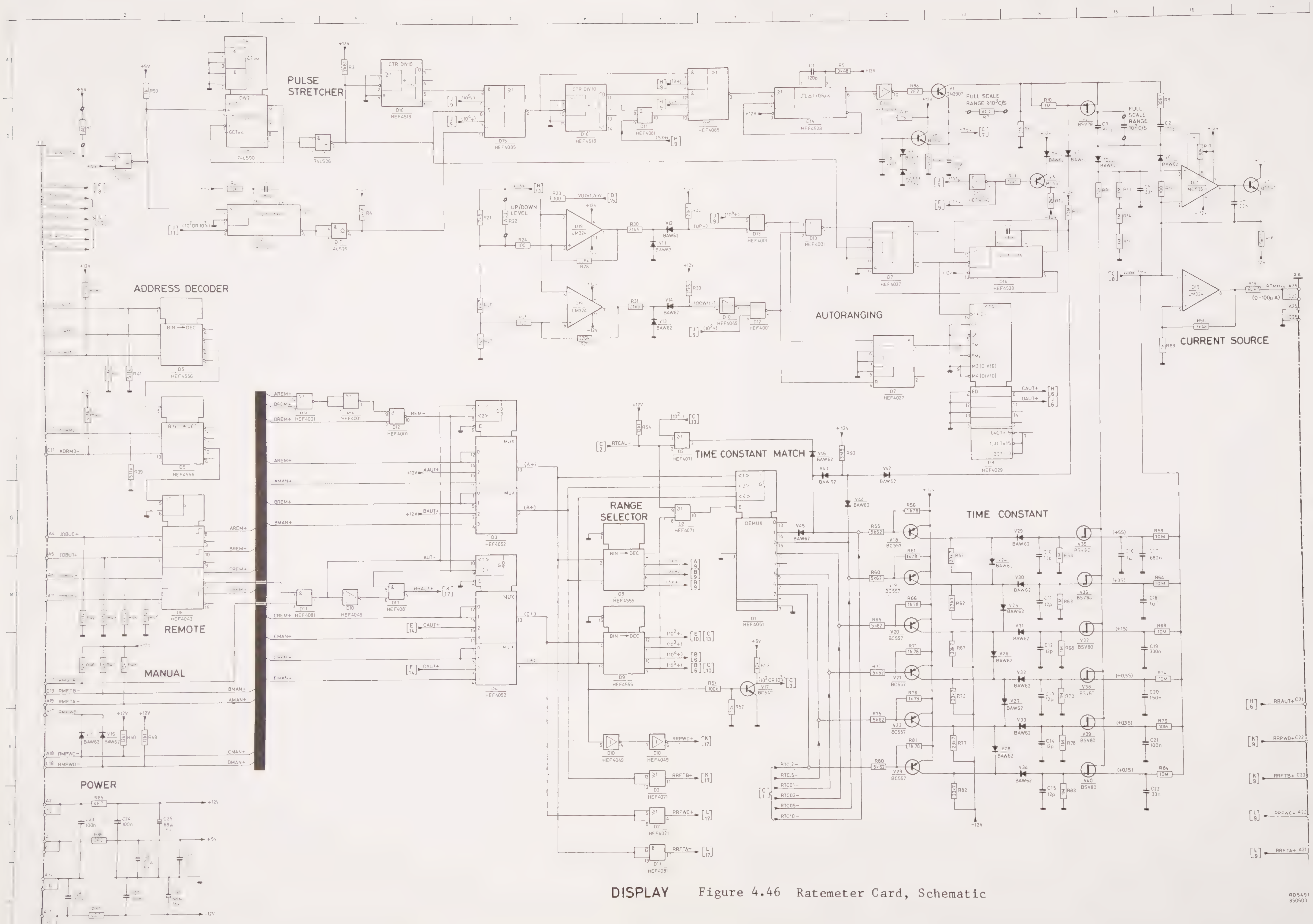

X1
RD5273
820318
C26
R86
R85
C23
C25
R41
R37
R38
R39
R40
R46
V16
V15
R87
C28
C30
C27
C24
R42
R43
R44
R45
R49
R50
R47
R48
R54
C29
V46
V45
D6
D5
D4
D3
D2
V44
D1
V43
R92
D12
D11
D10
D9
D8
V42
D7
R34
D18
R4
D17
R3
D16
D15
R5
C1
D14
C9
D13
R93
D20
C31
R2
R53
R52
R51
V4
R12
R11
V3
R10
R9
R6
R7
R88
R33
V14
V13
R31
R30
V11
V12
R32
D19
V17
V5
V2
V1
R22
R21
R24
R28
R29
R25
R26
R27
R91
R36
C7
V8
R23
R74
R72
V32
V27
R73
R89
R90
R19
V10
R35
V9
C8
V38
C13
R70
R71
C2
C20
R84
R82
V34
V23
V21
C3
C5
C22
V40
C15
R83
V41
R13
C21
R79
R77
R81
R80
R14
C19
V39
C14
V33
V28
R75
R15
R76
V6
R16
R78
R69
R67
D21
C16
V37
C12
V31
V26
V20
V22
R68
R66
R59
R57
R65
C4
V7
C17
V35
C10
V29
V24
R55
R56
R17
R58
V19
V18
R64
R62
R18
C18
V36
C11
V30
V25
R63
R61
R60

Figure 4.45 Ratemeter Card, Layout


PULSE STRETCHER
CTR DIV10
D16
HEF4518
D15
HEF4085
D16
HEF4518
D11
HEF4081
D15
HEF4085
D14
HEF4528
74LS90
74LS26
2N2907
FULL SCALE RANGE ≥10³C/S
FULL SCALE RANGE 10²C/S
BSV78
UP/DOWN LEVEL
D19
LM324
BAW62
D13
HEF4001
D10
HEF4049
D12
HEF4001
D7
HEF4027
D14
HEF4528
AUTORANGING
D8
HEF4029
CAUT+
DAUT+
CURRENT SOURCE
(0-100μA)
ADDRESS DECODER
BIN → DEC
D5
HEF4556
REMOTE
D6
HEF4042
MANUAL
POWER
+12V
+5V
-12V
AREM+
BREM+
CREM+
DREM+
AMAN+
BMAN+
CMAN+
DMAN+
AAUT+
BAUT+
MUX
D3
HEF4052
D4
HEF4052
TIME CONSTANT MATCH
RANGE SELECTOR
D9
HEF4555
DEMUX
D1
HEF4051
D2
HEF4071
TIME CONSTANT
BC557
BSV80
RRAUT+
RRPWD+
RRFTB+
RRPWC+
RRFTA+
RTC.2-
RTC.5-
RTC01-
RTC02-
RTC05-
RTC10-
RD5491
850603

DISPLAY Figure 4.46 Ratemeter Card, Schematic

4.13 CABLE CARD "DETECTOR"

4.13.1 INTRODUCTION

This cable card is used as a connection between the motherboard and the rear panel.

Figure 4.47 shows the wiring for this cable card.

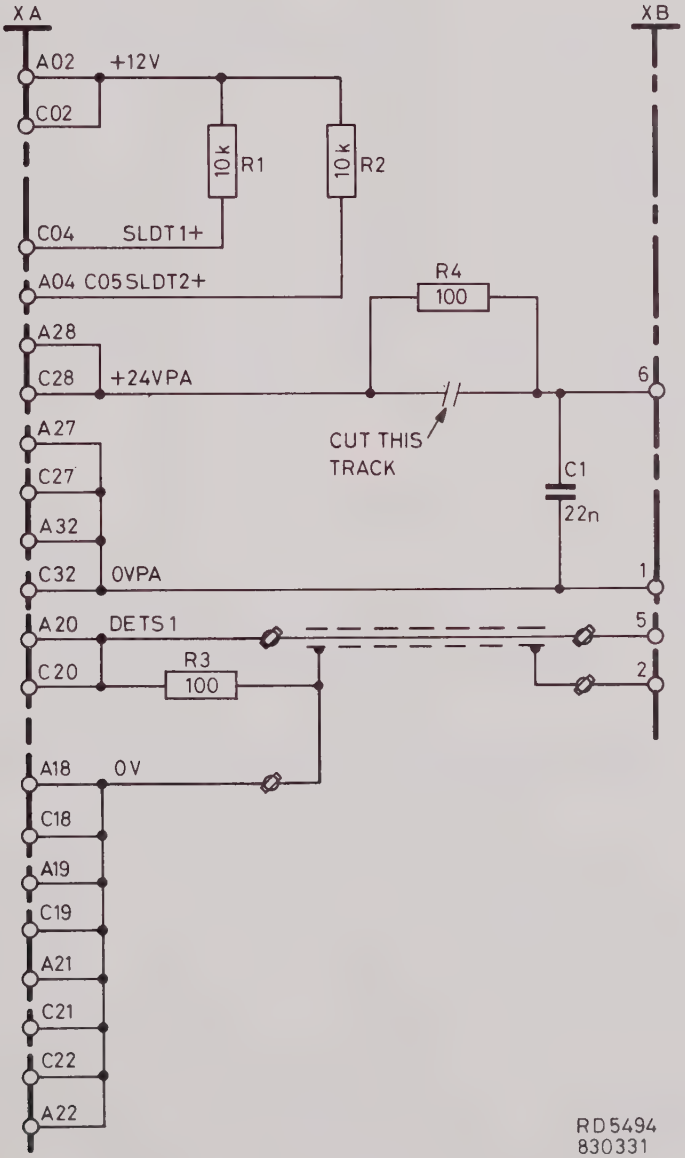

XA
XB
A02
+12V
C02
10k
R1
10k
R2
C04
SLDT1+
A04 C05 SLDT2+
R4
100
A28
C28
+24VPA
6
CUT THIS TRACK
A27
C27
C1
22n
A32
C32
0VPA
1
A20
DETS1
5
C20
R3
100
2
A18
0V
C18
A19
C19
A21
C21
C22
A22
RD5494
830331

Figure 4.47 Cable Card Detector

4.14 HV 2000 CARD

4.14.1 INTRODUCTION

This card provides the high voltage of up to 2000V d.c. for a xenon-filled or scintillation detector. The setting for the output voltage is made off-board on the SECONDARY CONTROL PANEL. The circuits on this card are:

- Reference voltage generator.
- DC-to-DC converter with voltage multiplier, and current and voltage limiter.
- HV output control.

Figure 4.48 shows a simplified block diagram of the card.

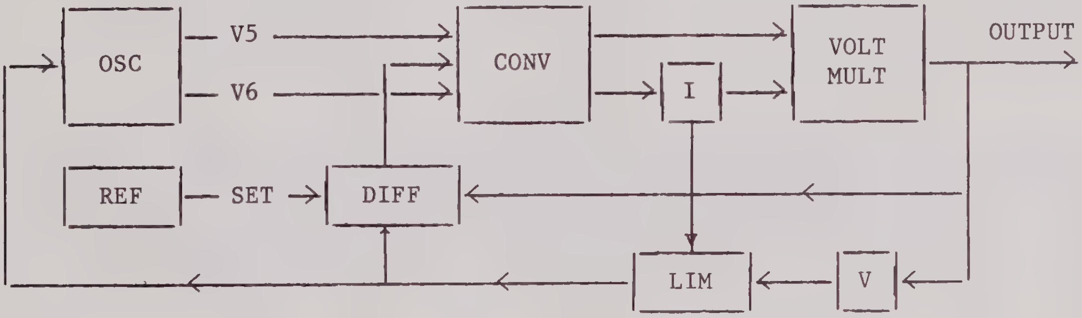


Figure 4.48 HV2000 Card Simplified Block Diagram

The working principle is as follows:

An oscillator driven converter stage is connected to a high voltage transformer. The secondary winding of the transformer generates an a.c. voltage. A voltage multiplying network rectifies and multiplies this voltage.

The output voltage is compared to an adjustable reference voltage (HVSET). To correct the output voltage level, the differential voltage is fed back to a bias generator circuit, influencing the primary voltage of the transformer.

NOTE: When working on this card, take insulating precautions (use insulated trimming tools.

The schematic diagram for this card is shown in figure 4.52, and the layout is given in figure 4.51.

4.14.2 REFERENCE VOLTAGE

An ultra-stable voltage reference diode V25 [E-6] is biased by R34. Opamp D4 and transistor V11 amplify and buffer the reference voltage, and a feedback loop (R32 and R33) provides the necessary stability.

The reference voltage (HVREF) is taken from pin A28. The setting of the high voltage has to be done by means of a potentiometer.

4.14.3 DC-to-DC CONVERTER

4.14.3.1 Oscillator and Transformer

The circuit is driven by an oscillator D1 [C-2]. Capacitor C1 is charged up to a level of approximately 8V, and then starts discharging until it reaches a level of about 4V, when it starts charging again. The resultant square wave at the output of D1 (pin 3) has a frequency of about 160 kHz. This frequency is connected to divider D2. D2 is a Johnson counter, wired as a divide-by-four frequency divider. Pins D2-3 and D2-4 provide non-overlapping clocks.

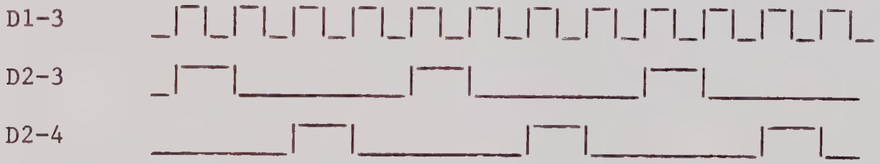


Figure 4.49 D1/D2 Output Waveforms

Complementary transistor pairs V1 + V2, and V3 + V4, drive the power transistors V5 and V6 [C-4]. These transistors are switched on alternatingly, causing an alternating magnetic field in transformer T1 [C-4]. The common-collector voltage (bias voltage), and therefore the primary voltage, is determined by transistor V7 [A-4], which is described in "HV CONTROL".

4.14.3.2 Voltage Multiplier

At power-up, during the first half cycle, the secondary voltage of T1 charges C7 to the nominal peak voltage value. During the next half cycle, V16 is forward biased, and T1 and C7 (which are then connected in series) charge C9 to about twice the nominal peak value. Subsequently C8 and C10 will be charged to respectively about 3 and 4 times the nominal value. This results in a voltage up to 3kV at the junction of V18 and C10. Each following cycle maintains this situation.

4.14.3.3 Current and Voltage Limiter

Two limiting circuits are provided:

1. The a.c. voltage across R22 and R23 [C-5] is rectified by V20 and charges C16 to a voltage, which is proportional to the output current. The maximum value can be adjusted by R23.
2. The very low current allowed by the high resistance (22 m ohm) of R24 causes the gas filled lamp E1 to oscillate, the resultant voltage across R25 and R26 is rectified by V21 and charges C16 to a voltage which is proportional to the output voltage. The maximum value can be adjusted by R26.

Normally, the voltage on C16 [D-5] and the base of V9 [D-4] is +10V d.c. If either the output current or the output voltage reaches its maximum, the voltage on the emitter of V9 becomes +10.7V d.c. or more, and V9 starts to conduct. This turns V10 ON, and D1-4 [C-2] and the output of D3 [A-6] are pulled LOW. D1 stops oscillating V7 and V8 stop conducting, and no current will flow through the primary windings of the transformer.

4.14.4 HV OUTPUT CONTROL

A sample of the output voltage (HVOUT) is attenuated by R15/R16 [B-7], and compared with the adjustable reference voltage HVSET [A-7] in the comparator D3 [A-6]. HVSET is the reference voltage HVREF [E-7] attenuated according to the potentiometer setting on the Secondary Control Panel.

The amplified differential voltage from D3 is buffered by V8 and V7 and used to control the common collector current of V5 and V6. R19 and C20 reduce the gain of D3 at high frequencies.

After a maximum current or maximum voltage situation, the bias voltage starts from zero (controlled by V10 [D-4]) to assure a smooth start of the converter.

4.14.5 CALIBRATION

WARNING: This procedure involves working on a printed circuit board on which up to 2 kV is present at several places. For all adjustments use plastic trimming tools and stand on an insulating mat.

1. Switch off the mains supply.

2. Disconnect the high voltage supply to the detector at the BNC connector.

3. Remove the HV2000 CARD and reconnect it using an extender card.

4. Connect a load resistor of 30 M ohm, 1 Watt, between the BNC connector and pin C24.

5. On the Secondary Control Panel, set switch S6 to GAS, and turn potentiometer R17 fully clockwise (maximum is reached when clicks can be heard).

6. Rotate the potentiometers R23 and R26 on the HV2000 CARD totally counter clockwise.

7. Connect a high voltage meter (Range at least 2000V d.c., input resistance at least 30 M ohm) to the output pins mentioned in (4), and switch ON the mains supply.

8. Connect an oscilloscope to the collector of V5 or V6 [C-4] and check that the signal trace shown in figure 4.50 is observed:

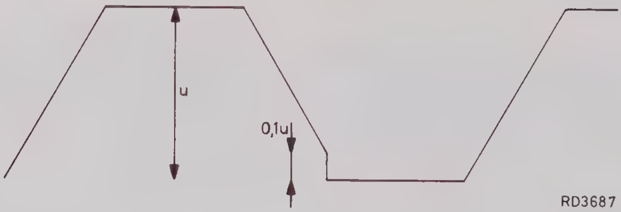


Figure 4.50 V5/V6 Output Waveform

If this signal form is observed, no saturation or unwanted oscillation of the transformer will be present.

If this signal form is not observed, adjust the oscillator potentiometer R2 [B-1] until it is.

9. If the output voltage is not 2000V d.c., change the value of R43 [E-7] until 2000V d.c. is obtained.

10. Measure the voltage on the cathode of V23 [D-4] with the oscilloscope, and record it.

11. Adjust R23 [C-5] until the peak value of the voltage on the anode of V20 as measured with the oscilloscope is the same as found in (10). This sets the maximum current value.

12. Adjust R26 [C-6] until the peak value of the voltage on the anode of V21 as measured with the oscilloscope is the same as found in (10). This sets the maximum voltage value.

13. Connect a capacitor of 10 nF, 3 kV, to the BNC connector and check the ripple on the output. This must be less than 10 mV a.c.

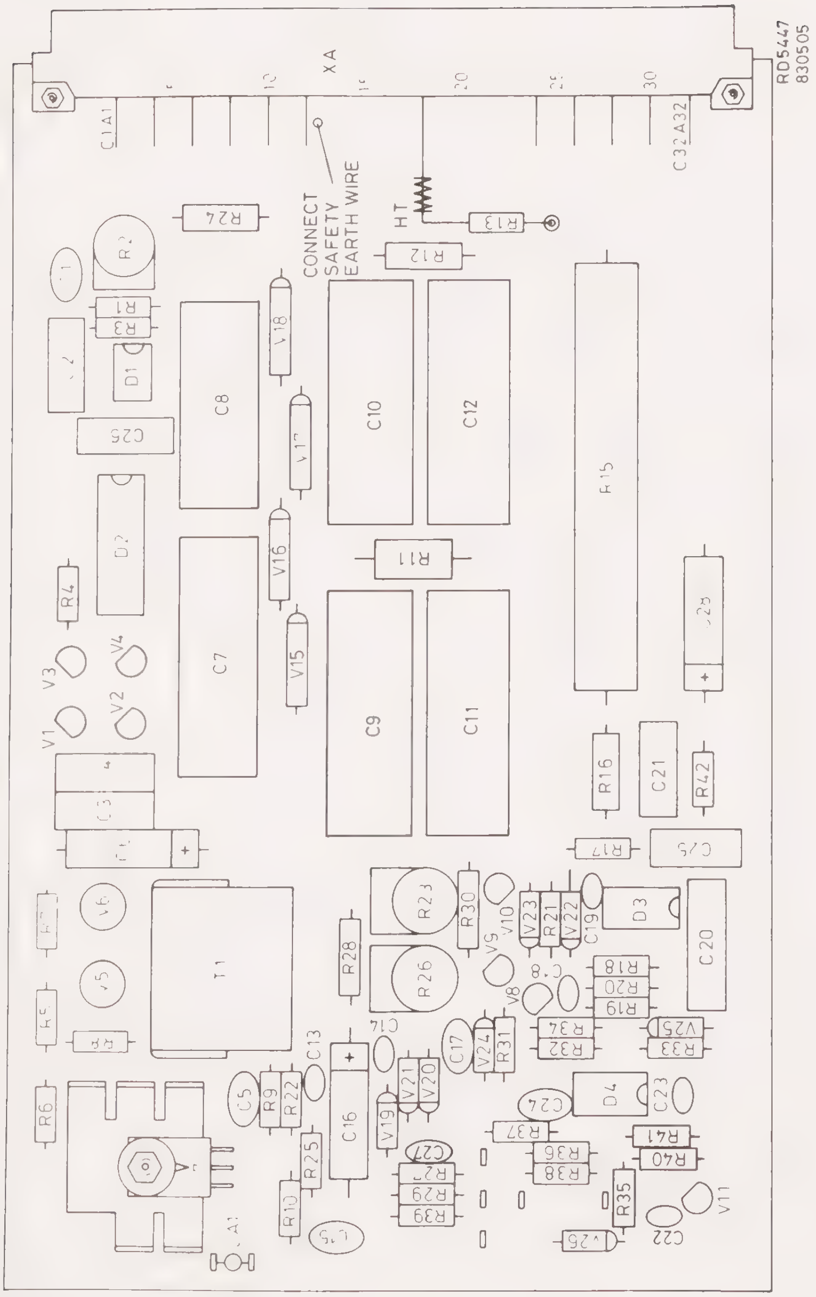

RD5447
830505
XA
C1A1
C32A32
10
20
30
CONNECT SAFETY EARTH WIRE
HT
R13
R24
R12
R1
R3
D1
C25
C8
V18
V17
C10
C12
R15
D2
R11
V16
R4
V15
V3
V4
C7
C9
C11
V1
V2
R16
C21
R42
R17
R23
R30
V10
V23
R21
V22
C19
D3
C20
T1
R28
V9
R18
R20
R26
V8
R19
C14
C17
V24
R31
R34
R32
V25
R33
C13
V21
V20
C5
R9
R22
C16
V19
C24
D4
C23
R6
R37
R41
C27
R36
R40
R25
R29
R38
R35
R10
R39
V11
C22
V26

Figure 4.51 HV2000 Control Card, Layout

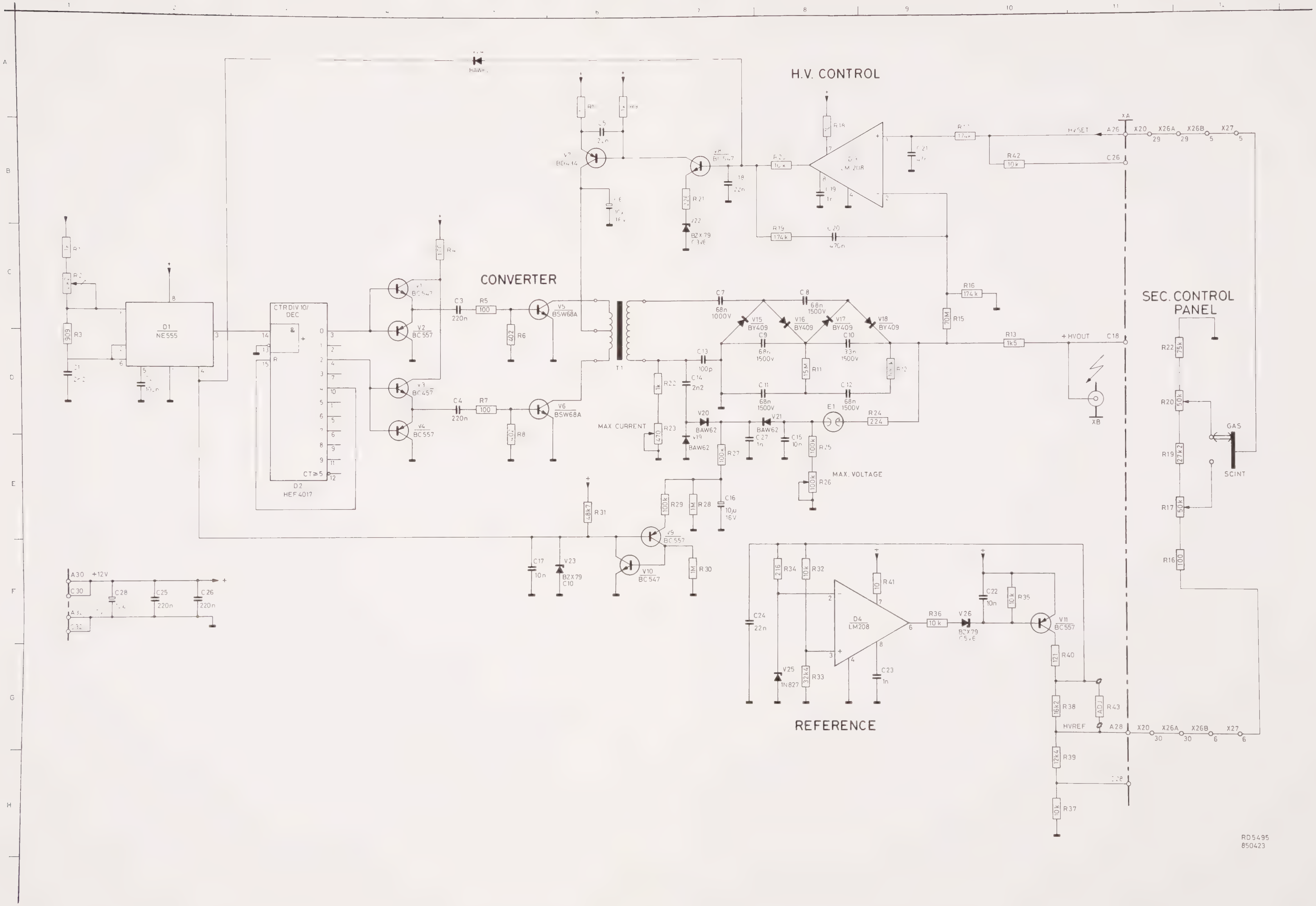

H.V. CONTROL
CONVERTER
SEC. CONTROL PANEL
REFERENCE
D1 NE555
CTRDIV 10/ DEC
D2 HEF 4017
D3 LM 208
D4 LM208
V1 BC547
V2 BC557
V3 BC457
V4 BC557
V5 BSW68A
V6 BSW68A
V9 BC557
V10 BC547
V11 BC557
V15 BY409
V16 BY409
V17 BY409
V18 BY409
V20 BAW62
V21 BAW62
V19 BAW62
V22 BZX79 C3V6
V23 BZX79 C10
V25 1N827
V26 BZX79 C5V6
T1
E1
MAX CURRENT
MAX. VOLTAGE
HVSET
HVREF
+HVOUT
A26
C26
C18
A28
X20
X26A
X26B
X27
XA
XB
GAS
SCINT
A30
C30
+12V
R3 909
R5 100
R6 402
R7 100
R8 402
R13 1k5
R15 70M
R16 174k
R19 174k
R20 50k
R22 75k
R17 50k
R16 100
R19 27k2
R24 22k
R25 100k
R26 100k
R27 100k
R28 1M
R29 100k
R30 1M
R31 48k7
R32 10k
R33 32k4
R34 216
R35 10k
R36 10k
R37 10k
R38 16k2
R39 12k4
R40 121
R41 10
R42 10k
R43 ADJ
C3 220n
C4 220n
C7 68n 1000V
C8 68n 1500V
C9 68n 1500V
C10 33n 1500V
C11 68n 1500V
C12 68n 1500V
C13 100p
C14 2n2
C15 10n
C16 10µ 16V
C17 10n
C20 470n
C22 10n
C23 1n
C24 22n
C25 220n
C26 220n
C27 1n
RD5495
850423

Figure 4.52 HV2000 Control Card, Schematic

4.15 RECORDER CONTROL CARD

4.15.1 INTRODUCTION

The Recorder Control Card controls either the PM8203A recorder or the PM8210/31 recorder, it does this under the control of the micro-processor on the System Control Card. It receives these instructions via the XRA-bus.

The functions on the card are:

- Control of the one-line strip chart recorder PM8203A as a slave
- ControL of the printing strip chart recorder PM8210/31 as a slave
- Generation of paper feed pulses
- Ratemeter time constant selection buffer (PW1710 only)
- Analogue multiplexer for analogue data to the recorder
- Module address comparator, jumper selectable to address 0 to F

The card has two connectors, they are:

XA which is a 64-pin connection to the XRA-bus and other printed circuit boards in the electronics rack.

XB which is a 25-pin connection to the strip chart recorder.

The schematic diagram for this card is shown in figure 4.54, and the layout is given in figure 4.53.

4.15.2 MODULE ADDRESS DECODING [A-3]

D10 [B-2] decodes the 4 module address lines into a card select signal, when the address D82x is present. This signal is used to enable D14 and D15.

The four byte address lines ADRB0 to 3 are decoded by D15 [B-5] into dedicated byte select lines, these, together with either IORED- or IOWRT- from D14 [D-1] are composed in D23 and D21 [B-7, D-7] into the vatious read-byte and write-byte signals.

Table 4.11 lists the functions assigned to the bytes.

Table 4.11 Byte Functions

Byte Address Hex	Direction	Function
0	Write	Pulse train length
1	Write	Analogue voltage selector
2	Read	Status of PM8203A
3	Write	Ratemeter time constant setting
4	Read	Ratemeter time constant (check)
5	Write	Control for PM8203A
6	Read	Control for PM8203A (check)
7	Write	Output data for PM8210/31
8	Read	Input data from PM8210/31
9	Write	Mode/command instruction to USART
10	Read	Status of USART

4.15.3 DATA BUS BUFFER [K-5]

The card uses +5V logic and the XRA-bus uses +12V logic. Therefore level converters are necessary in both directions. D12 [I-5] and parts of D9 [I-4] convert data from the XRA bus from +12V into +5V, while D6 [I-6] drives the card´s BUFFERED DATA BUS.

During a CARD-READ cycle, IORED- goes low (TRUE), this results in D13 [A-7] producing a (READ)+ signal. This (READ)+ signal enables the level converters D11 [J-6] and D5 [L-6]. The outputs of the converters are normally floating, but when the converters are active they convert the +5V from the card data bus into +12V for the XRA bus.

4.15.4 CONTROL OF THE ONE-LINE STRIP CHART RECORDER PM8203A [B-14]

Control of this recorder is via dedicated lines in TTL compatible logic, these lines are as follows:

Output lines to XB [C-22]:

PENLU	analogue pen lift UP
SRVON	servo system ON
FORWD	direction of paper feed FORWARD
DGMEN	degree marker enable (left hand angle indication)
RECON	recorder ON (paper feed) [G-22]

Four of these signals are contained in WRITE byte 6 as follows:

WRITE BYTE 6: command 1

X	X	PENLU+ 1 = UP	SRVON- 0 = ON	FORWD- 0=FORW	DGMEN+ 1=ENABL	X	X

For information about RECON, refer to paragraph 4.15.7.

Input lines from XB [F-1]:

ANPOL	analogue pen-on-line indication
EOPAP	end-of-paper
LOCAL	switch LOCAL/REMOTE on the recorder front panel
RECON	recorder ON (check of output line)
PTBSY	pulse train BUSY (common for both types of recorders)
DEGRM	degree marker (check of output line)
PENLU	analogue pen lift UP (check of output line)
SRVON	servo system ON (check of output line)
FORWD	direction of paper feed FORWARD (check of output line)
DGMEN	degree marker enable

This information is set into READ bytes 2 and 6 as follows:

READ BYTE 2: status 0

ANPOL- 0=TRUE	EOPAP+ 1=TRUE	LOCAL+ 1=TRUE	X	RECON- 0 = ON	PTBSY+ 1=BUSY	X	X

READ BYTE 6: status 1

1	DEGRM- 1=ENERG	PENLU+ 1 = UP	SRVON- 0 = ON	FORWD+ 1=FORW	DGMEN+ 1=ENABL	X	X

4.15.5 CONTROL OF THE PRINTING STRIP CHART RECORDER PM8210/31 [M-18]

This recorder has a RS232C/V24 compatible serial interface, and has to be controlled by means of control characters. For this reason this card has a serial interface built around a 8251A USART (Universal Synchronous/Asynchronous Receiver and Transmitter) D1 [K-14].

This USART converts parallel data from the XRA bus into serial data to the recorder and vice versa. The speed of these actions is determined by an on-card baud rate generator D32 [K-12] with a 2.4576 MHz crystal B1 [K-11]. The baud rate is set by jumpers to 9600 bits/s (jumpers W3 to W6).

READ/WRITE BYTE 8: USART received/transmitted data

X	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

(Bit D7 is immaterial provided the USART is set to 7 bits/character)

In order to configure this versatile chip for its task, initialization of the USART is necessary. Therefore the first instruction after power-up, or a CLEAR, to the control buffer of the IC, is a mode instruction. The settings are free (except for the baud rate factor), they only have to match that of the recorder´s serial interface.

For more information about this chip, refer to the DUAL SERIAL INTERFACE card description given in section 4.3 of this Chapter.

A good format for this mode instruction could be the following:

2 Stop bits, parity EVEN, disable parity, 7 bits/character, factor = 9

WRITE BYTE 9: USART mode (first WRITE after power-up or CLEAR

0	1	1	0	1	0	1	0

All succeeding instructions to the same address are command instructions, controlling the modem and the ability to send or receive.

WRITE BYTE 9: USART command

0	1= RETURN TO MODE	RTSR+ 1 = ON	1=RESET ERROR FLAGS	BREAK+ 1=SEND BREAKS	RCV 1=ENABL	DTRR+ 1 = ON	TMIT 1=ENABL

The status of the USART can be monitored by reading the status register.

READ BYTE 9: USART status

DSRR+ 1 = ON	BREAK 1=DET´D	FRAMING 1=ERROR	OVERRUN 1=ERROR	PARITY 1=ERROR	TMIT 1=EMPTY	RCV * 1=READY	TMIT * 1=READY

* = An interrupt request is generated if either (or both) of the following situations occur:

1. RCV READY in the status register is "TRUE" and the receiver is enabled.
2. TMIT READY in the status register is "TRUE" and the transmitter is enabled.

Interrupts (*) from the USART´s receiver and transmitter are OR-ed in D19 [K-16] and transferred to the XRA bus as INTR4- [J-22].

Output and input levels have to meet EIA specifications, therefore receiver D7 [J-16,M-16] converts EIA levels from the recorder into TTL, and line driver D8 [I-16,L-16] converts TTL levels into EIA compatible levels.

EIA-levels: HIGH >+3V LOW <-3V

Since the recorder behaves like a "data terminal equipment" (DTE), this card has to emulate the "data communications equipment" (modem = DCE). Signal names are given from the DTE´s viewpoint, therefore input for the recorder (which is output from this card) is called "received data" (RxD) and so on.

The signal CLEAR- [E-1], on the XRA bus also clears the recorder.

4.15.6 PAPER FEED PULSES [E-21]

The paper drive signal RCPLS [F-22] is commom for both recorders. Each recorder has an input for external paper feed pulses.

For the PM8203A 30 pulses are required to move the paper 1 mm (in order to achieve this, the CHART SPEED selector on the recorder´s front panel must be in the position 10 and the mode switch must be in the position REMOTE).

For the PM8210/31 18 pulses/mm are required.

Both recorders accept an input frequency up to a maximum of 300Hz. For this purpose, the XRA bus signal 30KHZ [D-18], is twice divided by 10 by D25 [E-19] to provide the 300Hz.

To move the paper, the XRA bus controller must store the required number of pulses into the parallel-load buffer of the cascaded divide-by-n ICs D31 [H-20] and D26 [K-20].

WRITE BYTE 0: paper feed pulse train length (in binary)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

The write cycle command (WRITE BYTE 0)- sets the D-flip-flop D30 [I-21], which enables the 300Hz to pass through gate D19 [F-20] and drive the paper feed circuitry inside the recorder. It also loads the divide-by-n counter D31/D26 in order to synchronize it.

The 300Hz. is also connected (via D19) to D31, which together with D26 counts the required number of pulses according to the state of IOBB 0 to 7. Simultaneously the 300Hz is counted in D31 [H-20] and D26 [K-2-]. Upon reaching the required number of pulses, via the terminal count (TC) of D26, the D-flip-flop D30 [I-20] will be reset and gate D19 [F-20] will be closed.

The XRA bus controller can monitor the pulse train generator by reading PTBSY [G-18] (refer to PM8203A, input lines).

4.15.7 ANALOGUE SIGNAL TO THE RECORDER [H-12]

This circuit consists of an 8-position analogue switch and a buffer plus attenuator, to adapt to the various input voltage spans of the recorders. The analogue switch can select 1 of 8 parameters to be recorded on paper. To select the required parameter, a 3-bit value has to be written to latch D29 [G-9].

WRITE BYTE 2: command 0

					ANALOGUE SIGNAL SELECTION		
				RECON-	BIT 2	BIT 1	BIT 0

At the input of the analogue multiplexer D24 [H-11], 2V represents a full scale value. At the connector [G-1], not all inputs are equal; they differ in span and input impedance because of differences in divider circuits.

The differences are listed below:

#0 Pin C18 (RTMH2). This input has a full scale value of 8V with an internal resistance of 82,5 Kohm. The internal resistance together with R10 and R9 [G-3,H-3] attenuate the voltage by a factor of 4.

#1 Pin A19 (LWLEV). This input has a full scale value of 2V, therefore no dividers are used.

#2 Pin C19 (CASHI). This input has a full scale value of 2V, therefore no dividers are used.

#3 Pin A18 (RTMH1). This input has a full scale value of 8V with an internal resistance of 82,5 Kohm. The internal resistance together with R8 and R7 [G-3,H-3] attenuate the voltage by a factor of 4.

#4 Pin C30 (HVSET). This input has a full scale value of 5V. R26 and R27 [I-10] attenuate the voltage by a factor of 2,5. Opamp D27 [I-10] buffers the input voltage before it is attenuated.

#5 Measurement of the -12V supply. The -12V is converted by D27 [J-9] into a positive voltage. The multiplication factor is such that the nominal value of -12V results in a 90% of full scale deflection of the recorder pen, allowing a 10% deviation from nominal in both directions to be recorded.

#6 Measurement of the +12V supply. The +12V is attenuated by R28 and R29 [J-10,J-11]. The attenuation factor is such that the nominal value of +12V results in 90% of full scale deflection of the recorder pen, allowing a 10% deviation from nominal in both directions to be recorded.

4.15

#7 Measurement of the +5V supply. The +5V is attenuated by R25 and R24 [K-10,K-11]. The attenuation factor is such that the nominal value of +5V results in a 90% of full scale deflection of the recorder pen, allowing a 10% deviation from nominal in both directions to be recorded.

To show the use of the various full scale values, application in the PW1710 is listed in Table 4.12 below:

Table 4.12 Analogue Signal Values

BIT2	BIT1	BIT0	SIGNAL SOURCE
0	0	0	Ratemeter 2
0	0	1	H.V. Setpoint
0	1	0	Cassette Pos.
0	1	1	+12 V SUPPLY
1	0	0	Lower Level
1	0	1	-12 V Supply
1	1	0	Ratemeter 1
1	1	1	+5 V Supply

The output of the analogue switch D24 (the selected voltage rated down to 2V full scale) is passed to opamp D28 [K-14] and transistor V4 [K-15] to buffer the signal. Then via attenuation circuit R47 and R37, or R36 and R37 [H-16] (depending on W2, see the next paragraph) and is made available at connector XB [I-22] as RECHI, recorder "HIGH" signal.

The PM8203A has a full scale input voltage of 100mV. Therefore jumper W2 [H-16], marked "10", has to be left open, resulting in an attenuation factor of 20.

The PM8210/31 has a full scale input voltage of 1V. Therefore jumper W2, marked "10", has to be closed, resulting in an attenuation factor of 2.

4.15.8 TIME CONSTANT OF RATEMETER (FOR USE IN PW1710) [C-10]

The ratemeter card in the PW1710 has no register to accept XRA bus data to select the time constant. The selection is made here by means of dedicated and decoded selection lines (only one bit may be TRUE).

Data is clocked into D17 [B-9] by the (WRITE BYTE 4)- signal, and the buffered output is connected to the inverter D22 [B-11]. D22 drives the output lines [B-22] via zener diodes V6 to V10 [B-12]. The output swing of D22 is between 0 and 5V. The zener diodes bias the output voltage such that a PNP transistor with +12V supply can be turned ON and OFF.

The output of D22 is monitored by the buffer D18 [C-9], and can be clocked onto the internal data bus for checking when the (READ BYTE 4)- signal is generated by D15/D21.

READ BYTE 4: ratemeter time constant setting (PW1710 only)

X	AUTOMATIC	5 S	2 S	1 S	0.5 S	0.2 S	X

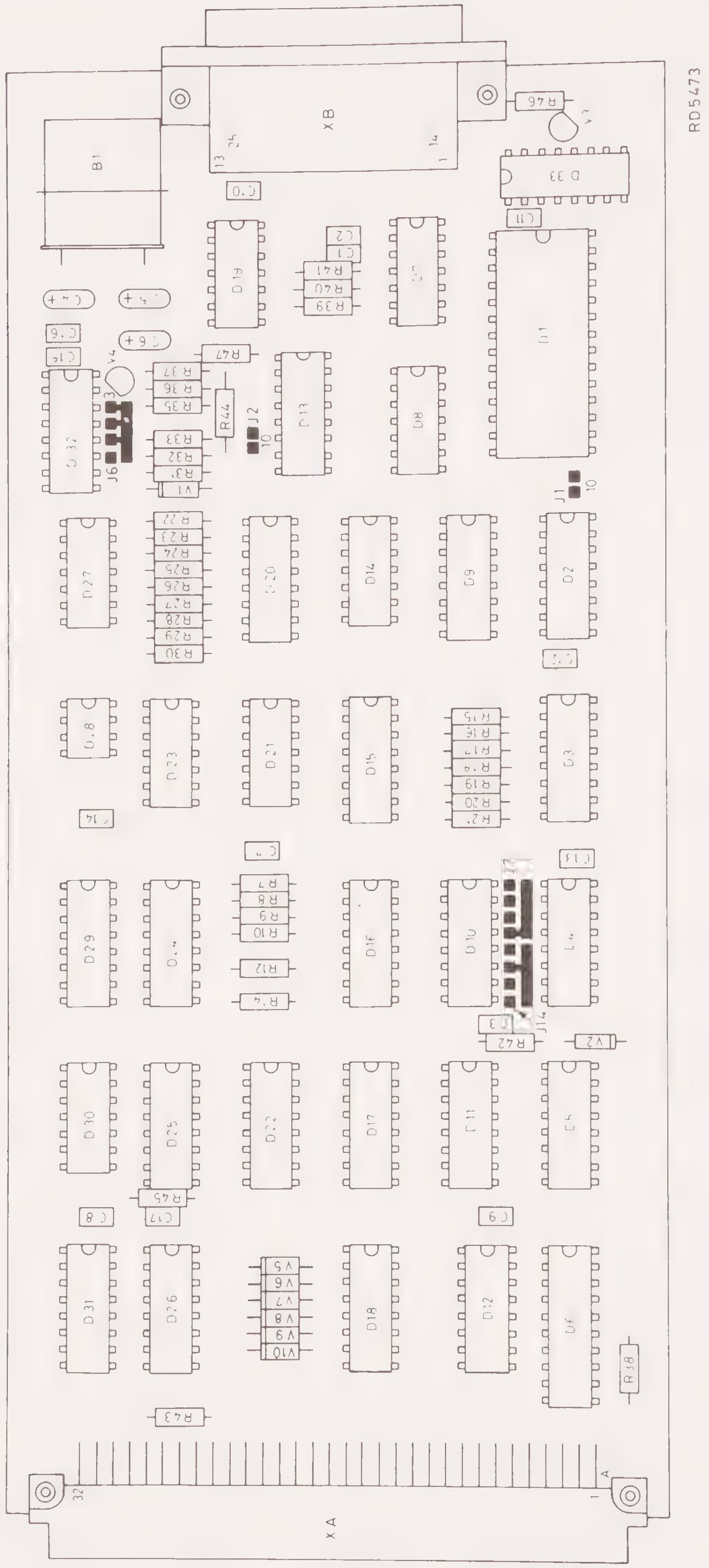

RD5473
XB
B1
D33
D1
D19
D13
D8
D32
J6
J2
J1
D27
D20
D14
D9
D2
D23
D21
D15
D3
D29
D10
D25
D22
D17
D31
D26
D18
D12
R38
R42
R43
R44
R45
R46
R47
XA
32
1
A

Figure 4.53 Recorder Control Card, Layout

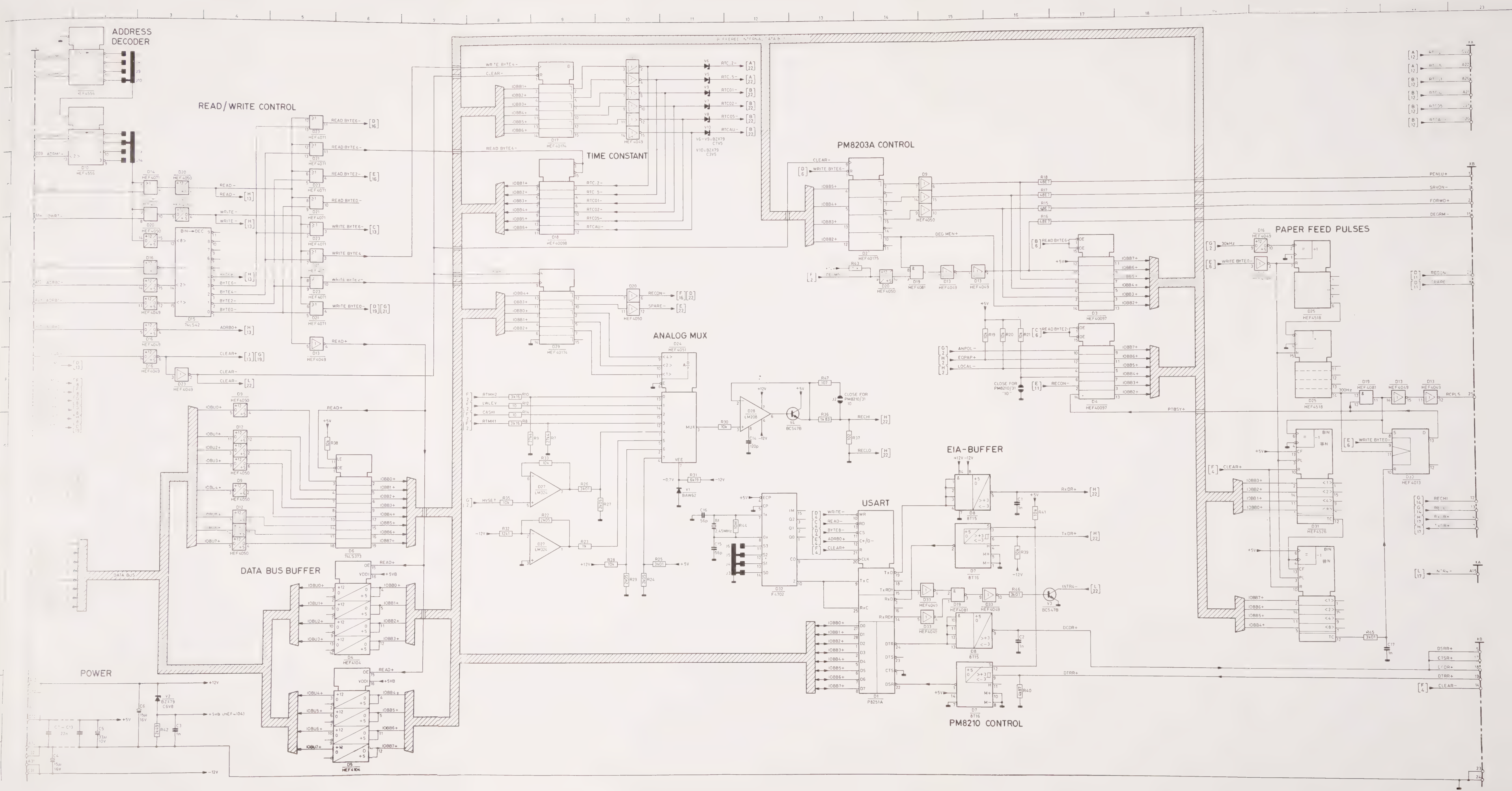

ADDRESS DECODER
READ/WRITE CONTROL
TIME CONSTANT
PM8203A CONTROL
PAPER FEED PULSES
ANALOG MUX
EIA-BUFFER
USART
DATA BUS BUFFER
POWER
PM8210 CONTROL
HEF4556
HEF4071
HEF4050
HEF4049
74LS42
HEF40174
HEF40098
HEF4051
LM208
BC547B
LM324
BAW62
F4702
P8251A
8T15
8T16
74LS373
HEF4104
HEF40175
HEF4081
HEF40097
HEF4518
HEF4526
HEF4013
BZX79 C6V8
PENLU+
SRVON-
FORWD+
DEGRM-
RECON-
SPARE-
RECHI
RECLO
RxDR+
TxDR+
INTR+
DCDR+
DTRR+
DSRR+
CTSR+
CLEAR-
RCPLS
+12V
+5V
-12V
DATA BUS
RD5493 850603

Figure 4.54 Recorder Control Card, Schematic

4.16 PW1170 INTERFACE CARD

4.16.1 INTRODUCTION

This card is an interface between the PW1170 Sample Changer and the XRA-bus controller. It makes full use of the PW1170 possibilities. The following commands are available:

* Cassette one step UP or DOWN
* Cassette RESET (to zero position)
* LOAD or UNLOAD a sample
* Read status

Apart from that, the card provides a sample number indication (a voltage with a value proportional to the sample number).

To achieve the above, the following functions are implemented on this card:

* Address decoder, jumper selected
* Control: latches for all commands
* Interlock system to exclude simultaneous functions
* Maximum timer
* Optocouplers to isolate logic levels from power electronics
* Zero-crossing detector (smooth switching) and motor switches
* Reference voltage for analogue sample number indication
* Status: buffers for all data

The schematic diagram for this card is shown in figure 4.56, and the layout is given in figure 4.55.

4.16.2 ADDRESS DECODER [A-4]

Decoder D14 [A,B-5] decodes the module address (contained in ADRM3 to ADRM0) into a "card selected" signal for decoder D15. By means of jumpers the card address can be selected, in the PW1710 the address is set to 8 (in hexadecimal code, jumpers 4 and 6 closed).

4.16.3 COMMANDS [A-9]

One byte is available for entering a command to this card. If this card is addressed, ADRB1 = LOW and ADRB0 = HIGH, output D15-5 [C-7], goes LOW, this enables D1 [A-9], and its outputs become active and follow the XRA-bus data lines. Under certain conditions (refer to paragraph 4.16.4 "Interlock"), these signals pass through interlock ICs D7 [A-12 and B-12] and D8 [C-12,D-12], and reach the data flip-flops D26 [B-14] and D23 [C-14].

As long as none of the the outputs of D26 or D23 are HIGH, the output of D13-4 [B-17], connected via D28 [A-6] to decoder D15-15, is HIGH and enables this decoder. BYTE2-, connected to D15-14, is LOW, and when IOWRT- goes LOW, output D15-12 also goes LOW. This is the clock signal for flip-flops D26 and D23, which will then store XRA-bus data.

WRITE BYTE 2: command

X	X	RESET ERROR 1=TRUE	BIT D1 0=DOWN 1=RESET	UNLOAD 1 = ON	LOAD 1 = ON	CASSETTE DOWN/RES 1 = ON	CASSETTE UP 1 = ON

NOTE 1: Bit D4 selects the function of bit D1:

If D4 = "0", bit D1 receives the function of "CASSETTE one step DOWN" command.

If D4 = "1", bit D1 receives the function of "CASSETTE to ZERO position" command.

NOTE 2: The XRA-bus signal CLEAR- is not connected on this card. Therefore, at power-up, the XRA-bus controller must write zeros to the action flip-flops on this card.

4.16.4 INTERLOCK [A-12,B-17]

To prevent damage, the data described in "Commands" above is allowed to pass ICs D7 and D8 only under certain conditions. These conditions are given in Table 4.13.

Table 4.13 Interlock Conditions

SIGNAL TO PASS	CONDITIONS	SIGNAL MEANING
STEP UP	D7-11 = HIGH	UNLOADED = TRUE
	D7-10 = HIGH	No actions running, and ERROR = FALSE
	D7-9 = HIGH	LAST SAMPLE = FALSE
STEP DOWN	D7-4 = HIGH	No actions running, and ERROR = FALSE
	D7-2 = HIGH	UNLOADED = TRUE
	D7-3 = HIGH	ZERO = FALSE
LOAD	D8-10 = HIGH	POSITION = TRUE (cassette in position)
	D8-11 = HIGH	No actions running, and ERROR = FALSE
	D8-12 = HIGH	LOADED = FALSE
	D22-9 = HIGH	ZERO = FALSE
UNLOAD	D8-4 = HIGH	No actions running, and ERROR = FALSE
	D8-3 = HIGH	UNLOADED = FALSE
	D8-5 = HIGH	ZERO = FALSE
RESET ERROR	None	
RESET CASSETTE	D7-4 = HIGH	No actions running, and ERROR = FALSE
	D7-2 = HIGH	UNLOADED = TRUE
	D7-5 = HIGH	STEP DOWN = TRUE
	D7-3 = HIGH	ZERO = FALSE

Additional conditions are needed for decoder D13:

CASSETTE UP and CASSETTE DOWN mutually exclude each other.
LOAD SAMPLE and UNLOAD SAMPLE mutually exclude each other.

4.16.5 MAXIMUM TIMER [E-14]

If BUSY+ = HIGH (true), gate D22 [G-14] is enabled and the clock input T of the 12-bit binary counter D24 receives clock pulses.

This clock is derived from the mains frequency. Optocoupler D4 [G-5] and Schmitt trigger D17 [H-6] generate a square wave with the frequency of the mains. After 2048 pulses (about 40 seconds), the 12th bit of the counter goes HIGH and the appropriate Set-Reset flip-flop in D25 [F-8] will be set to zero. ERROR- goes LOW and this indicates an ERROR-situation (40 seconds is longer than any of the mechanical actions will last).

The end of a properly performed mechanical action is indicated by one of the four one-shots in D18 and D19 [E to H-11]. Any of these one-shots will reset the counter temporarily, and at the same moment in D26 or D23 the appropriate Set-Reset flip-flop will be reset. This will stop timing definitively.

The conditions for the triggering of each of the one-shots are given in table 4.14 below:

Table 4.14 One-shot Triggering Conditions

ONE-SHOT	CONDITIONS	MEANING
D19-6	(ERROR)- going LOW, or (LAST SAMPLE)+ going HIGH, or (ZERO)+ going HIGH	Reset at cassette limit (ZERO or LAST)
D18-10	(LOADED)+ going HIGH, or (UNLOADED)+ going HIGH	Reset at LOADED or UNLOADED
D19-10	BUSY = HIGH, and (ZERO)+ going HIGH	Reset at ZERO
D18-6	(POSITION)+ going HIGH	Reset at CASSETTE IN POSITION

The ERROR flip-flop can be reset by a "RESET ERROR" command (refer to 4.16.3).

4.16.6 OPTOCOUPLERS [B-19]

Optocouplers D5, D6, D9 and D10 [A-19 to D-19] are used to isolate the logic circuitry from the 48V a.c. powered circuits (the motor switches).

From this 48V a.c. a -12V d.c. voltage is derived to power D11, diode V2 [G-21] rectifies the a.c. voltage and transistor V4 stabilizes it to -12 V d.c.

4.16.7 ZERO-CROSSING DETECTOR [F-23]

To ensure current-free switching, only at the moment of zero-crossing, are the voltages to the motors inside the sample changers switched ON and OFF.

Transistor V5 [F-22] is the zero-crossing detector. It conducts if 48V~1 is more negative than 48V~2. Therefore the clock input (ZCROS) of D11 receives a square wave at mains frequency. At each zero-crossing, the requested actions are reclocked in D11 [B-21].

The outputs of D11 control triacs V10 to V13 [B-24,C-24] via transistors V6 to V9. A HIGH level (= 0 V) at any of the outputs of D11 will turn the appropriate transistor ON. The gate of the connected triac becomes negatively biased with respect to its common terminal, and the triac start to conduct.
A LOW level (= -12 V) at D11 turns both the transistor and the triac OFF.

4.16.8 REFERENCE VOLTAGE FOR ANALOGUE SAMPLE INDICATION [K-4]

A positive analogue voltage is generated proportional to the sample number.

A reference voltage ATTRV [J-4] is attenuated by R43, R47 and R42, and buffered by opamp D29 [K-5]. The resulting voltage CASRV is connected to potentiometer R1 inside the PW1170 sample changer. The attenuated voltage CASHI (with a voltage of 20 mV d.c. per sample) is directly connected to the XRA-bus connector.

4.16.9 STATUS BUFFERS [F-18]

All information about the status of this card and the sample changer is contained in two bytes on this card. These bytes can be read when the signal IORED- is LOW (TRUE). The bytes are addressed by ADRB0 and 1 as follows:

ADRB1-	ADRB0-	ACTIVE BUFFER	STATUS WORD
HIGH	HIGH	D3 [F-18]	Sample changer status
HIGH	LOW	D2 [H-18]	Card status (check)

Status of the sample changer consists of information about a number of microswitches inside the PW1170:

CASPO	(S3 of PW1170)	cassette in position (a sample is level with the measuring position)
SAMGO	(S4 of PW1170)	sample in goniometer (end of LOAD-cycle)
SAMCA	(S5 of PW1170)	sample in cassette (end of UNLOAD-cycle)

These signals are connected to set-reset flip-flop D25 [F-8], which serves as an anti-bounce device.

CASLS	(S1 of PW1170)	cassette in last-sample position
CASZR	(S2 of PW1170)	cassette in zero position.

READ BYTE 0: status 0 (sample changer status)

X	X	CARD 0=READY 1=BUSY	CASSETTE IN POS. 1=TRUE	UNLOADED 1=TRUE	LOADED 1=TRUE	ZERO POS 1=TRUE	LAST POS 1=TRUE

BUSY = The BUSY flip-flop D26-3 is set, a command has been clocked-in.
CASSETTE IN POS. = The cassette is in one of the positions where loading and unloading is possible.
UNLOADED = The loading mechanism has withdrawn the sample in the cassette.
LOADED = The loading mechanism has put a sample in the measuring position.
ZERO POS = The cassette is in the "zero" position (cassette can be taken out of the sample changer).
LAST POS = The cassette is in the "last sample" position (selected by the screw on the cassette).

READ BYTE 1: status 1 (card status)

X	X	ERROR 0=TRUE	SUPPLY 1=TRUE	UNLOAD 1=TRUE	LOAD 1=TRUE	CASSETTE DOWN/RES 1=TRUE	CASSETTE UP 1=TRUE

ERROR = Contents of error flip-flop
SUPPLY = Check on presence of 48V a.c. supply
UNLOAD = Contents of unload flip-flop (check)
LOAD = Contents of load flip-flop (check)
CASSETTE DOWN/RES = Contents of step down flip-flop (check)
CASSETTE UP = Contents of step up flip-flop (check)

The frequency derived from the 48V a.c. [G-4] supply is used to trigger the retriggerable one-shot D21 [G-8]. When there is a proper supply, this one-shot is continuously triggered.

This card indicates that a sample changer is connected via a cable and an interface to the XRA-bus controller by means of the signal SCHPR. If input SCHPR- [K-4] is not connected, transistor V15 [L-7] is turned OFF, and SCHPR+ [L-24] is LOW. If a sample changer is connected, input SCHPR- is connected to GND, V15 is turned ON, and SCHPR+ is pulled HIGH.

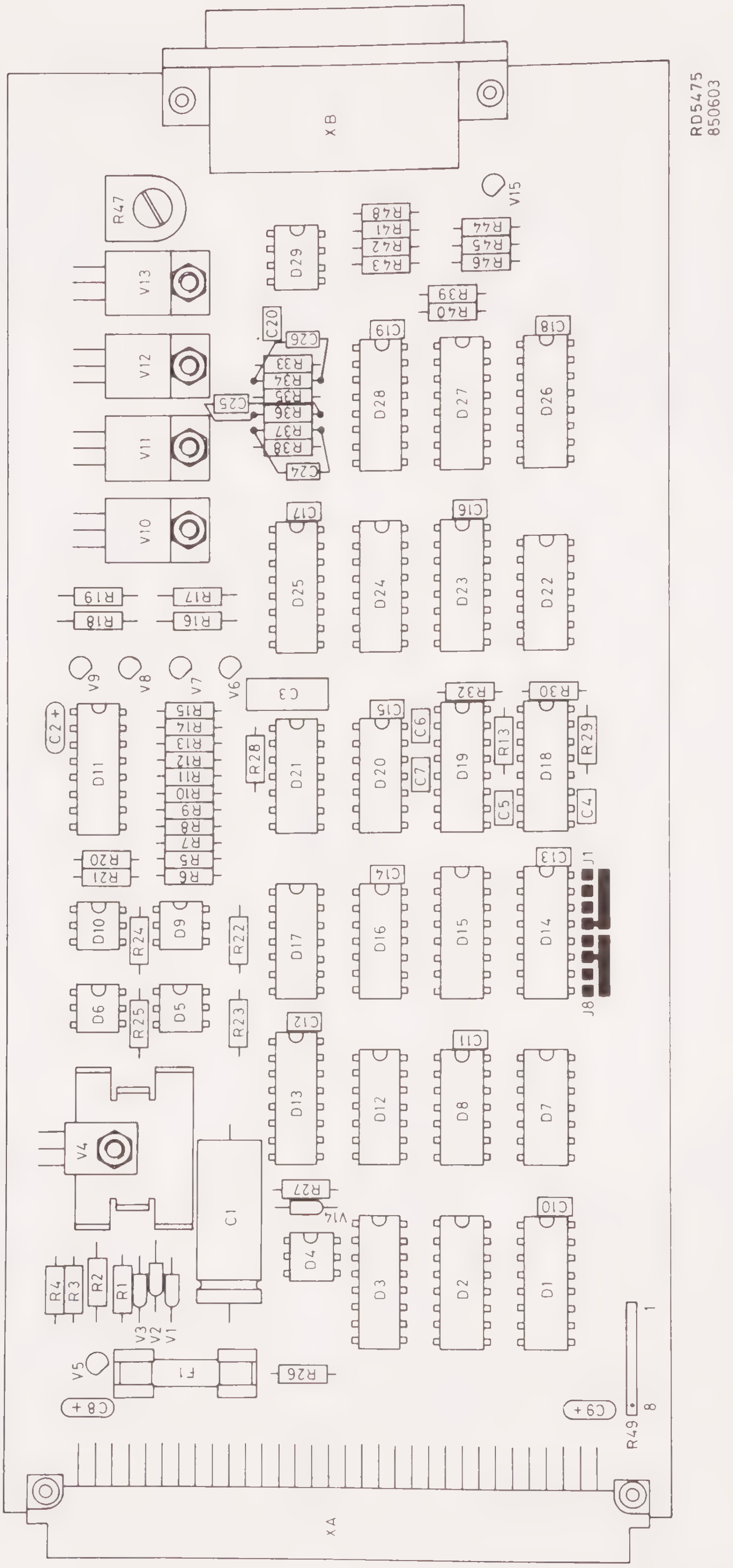
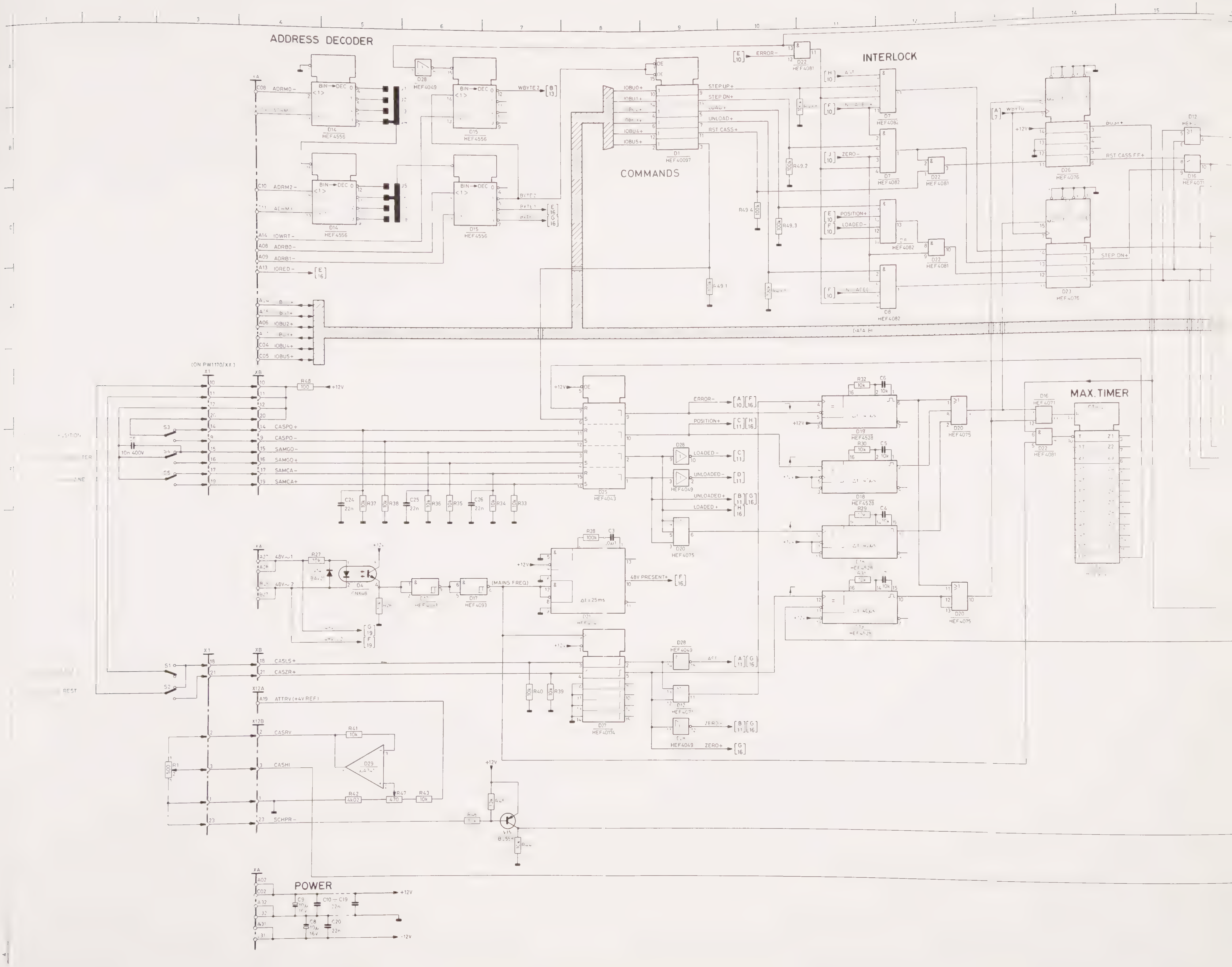

XB
RD5475
850603
R47
V13
V12
V11
V10
D29
R48
R41
R42
R43
V15
R44
R45
R46
R39
R40
C20
C26
R33
R34
R35
R36
R37
R38
C25
C24
C19
C18
D28
D27
D26
C17
C16
D25
D24
D23
D22
R19
R18
R17
R16
V9
V8
V7
V6
C3
R32
R30
C2+
D11
R15
R14
R13
R12
R11
R10
R9
R8
R7
R5
R6
R28
D21
C15
C6
D20
C7
D19
R13
C5
D18
R29
C4
R20
R21
D10
R24
D9
R22
D17
C14
D16
D15
C13
J1
D14
J8
D6
R25
D5
R23
C12
D13
D12
C11
D8
D7
V4
C1
R27
V14
C10
D4
D3
D2
D1
R4
R3
R2
R1
V3
V2
V1
V5
F1
R26
C8+
C9+
R49
1
8
XA

Figure 4.55 PW1170 Interface Card, Layout


ADDRESS DECODER
COMMANDS
INTERLOCK
MAX.TIMER
POWER
D14 HEF4556
D15 HEF4556
D28 HEF4049
D1 HEF40097
D22 HEF4081
D7 HEF4082
D8 HEF4082
D26 HEF4076
D23 HEF4076
D12
D16 HEF4071
D25 HEF4043
D19 HEF4528
D18 HEF4528
D20 HEF4075
D21
D17 HEF4093
D27 HEF40174
D29
D4 CNX48
V15
ADRM0−
ADRM2−
IOWRT−
ADRB0−
ADRB1−
IORED−
IOBU2+
IOBU4+
IOBU5+
IOBU0+
IOBU1+
WBYTE 2
BYTE 2
BYTE 1
STEP UP+
STEP DN+
LOAD+
UNLOAD+
RST CASS+
ERROR−
ZERO−
POSITION+
LOADED−
BUSY+
RST CASS FF+
STEP DN+
DATA BUS
(ON PW1170/XX)
X1
XB
XA
X12A
X12B
CASPO+
CASPO−
SAMGO−
SAMGO+
SAMCA−
SAMCA+
CASLS+
CASZR+
ATTRV (+4V REF)
CASRV
CASHI
SCHPR−
S1
S2
S3
S4
S5
POSITION
ZONE
REST
10n 400V
R48 100
+12V
−12V
ERROR−
POSITION+
LOADED−
UNLOADED−
UNLOADED+
LOADED+
48V∼1
48V∼2
R27
(MAINS FREQ)
48V PRESENT+
Δt = 25ms
R28 100k
C3
R32 10k
C6
R30 10k
C5
R29
C4
R37
R38
R36
R35
R34
R33
C24 22n
C25 22n
C26 22n
R40
R39
R41 10k
R42 4K02
R47 470
R43 10k
R1 500
R49.1
R49.2
R49.3
R49.4
AST
ZERO−
ZERO+
C9 10μ 16V
C10 — C19 22n
C8 10μ 16V
C20 22n
A02
C02
A32
A31
C08
C10
A14
A08
A09
A13
A06
C04
C05
A19
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

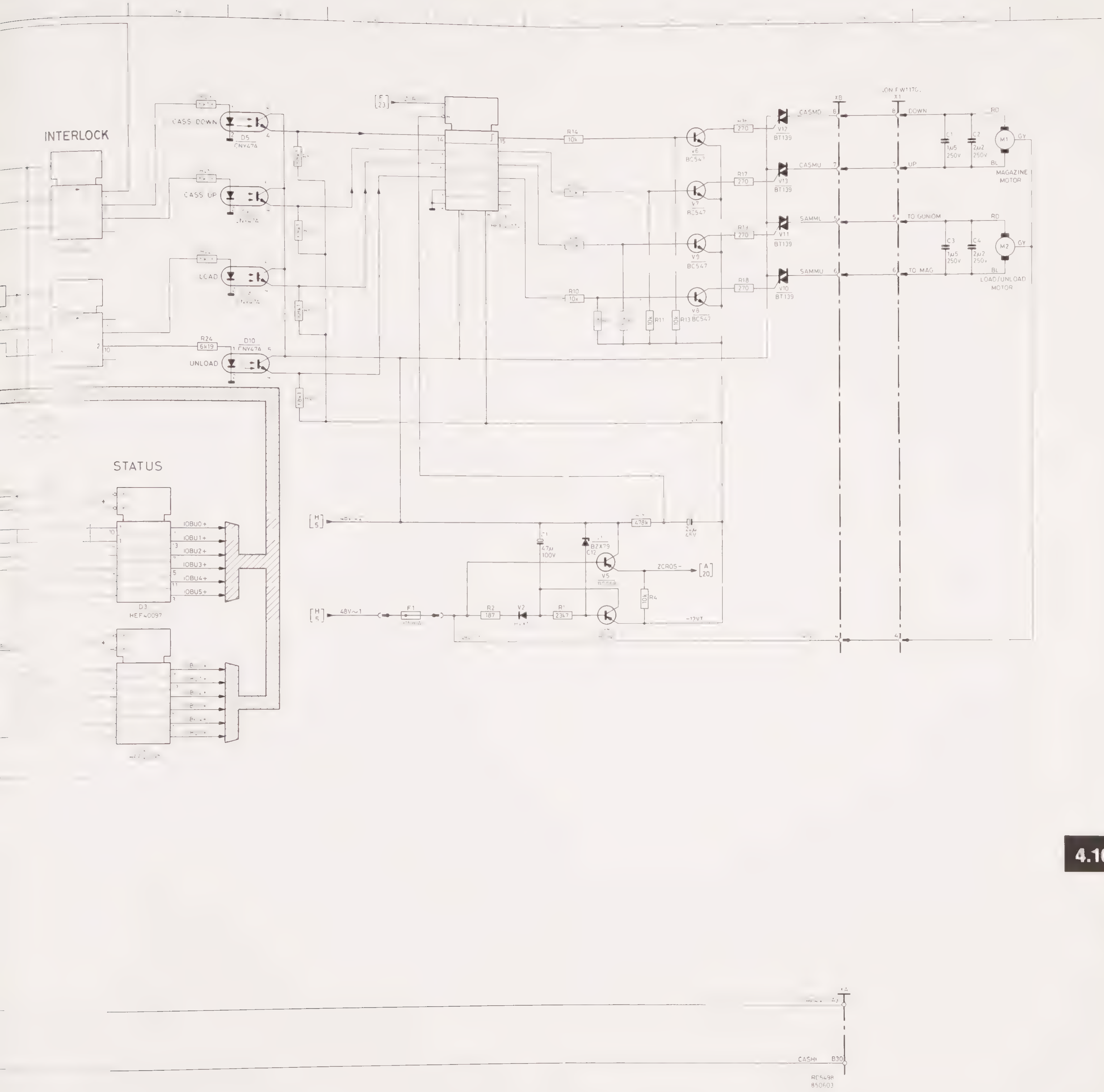

INTERLOCK
CASS DOWN
D5
CNY47A
CASS UP
LOAD
UNLOAD
R24
6k19
D10
CNY47A
STATUS
IOBU0+
IOBU1+
IOBU2+
IOBU3+
IOBU4+
IOBU5+
D3
HEF4009?
F
23
R14
10k
R10
10k
R11
10k
R13
10k
V6
BC547
V7
BC547
V9
BC547
V8
BC547
R17
270
R18
270
270
V12
BT139
V13
BT139
V11
BT139
V10
BT139
CASMD
CASMU
SAMML
SAMMU
XB
ON PW1170
X1
DOWN
UP
TO GONIOM
TO MAG
C1
1µ5
250V
C2
2µ2
250V
C3
1µ5
250V
C4
2µ2
250V
M1
M2
RD
GY
BL
MAGAZINE MOTOR
LOAD/UNLOAD MOTOR
H
5
48V~1
F1
R2
187
V2
23k7
47µ
100V
BZX79
C12
V5
478k
ZCROS-
A
20
10k
R4
-12VT
CASH
B30
RE5498
850603

Figure 4.56 PW1170 Interface Card, Schematic

4.17 CHANGER SPINNER SHUTTER CONTROL CARD

4.17.1 INTRODUCTION

Together with the Shutter Spinner Drive Card, this card is the interface between the XRA-bus controller, the Sample Changer PW1775, the Sample Spinner PW1774 and the shutter circuit inside the tube tower.

Possible commands to this card are:

- MOVE THE MAGAZINE to an indicated position.
- LOAD and UNLOAD a sample, either from or to the magazine or the single sample position.
- FIX or RELEASE the sample in the measuring position by using the lifting mechanism.
- SPIN the sample.
- OPEN and CLOSE the shutter.
- Generate an ANALOGUE SIGNAL, proportional to the magazine position.

For this reason, this card provides the following sub-circuits:

- Address decoder
- Spinner control
- Shutter control
- Magazine control
- Grab control
- Grab rotation control
- Lift control
- Miscellaneous status
- Card status
- Analogue magazine position indicator

The schematic diagram for this card is shown in figure 4.58, and the layout is given in figure 4.57.

4.17.2 ADDRESS DECODER [A-2]

Decoder D39 [A-2,C-2] decodes the module address (contained in ADRM3 to ADRM0) into a "card selected" signal. By means of jumpers the card address can be selected. In the PW1710 the address is set to 8 (in hexadecimal code, jumpers J4 and J6 are closed).

The "card selected" signal is composed with IORED and IOWRT in D23 [B-3] Decoders D34, D35, D29 and D28 [C,E,F,G,H, & J - 4] use the READ signal from D23-11 and the WRITE signal from D23-10 together with the byte address lines to derive the various read-byte and write-byte signals. The functions of these bytes are given in Table 4.15 following:

Table 4.15 Byte Functions

BYTE ADDRESS	MODE	FUNCTION
0	WRITE	data to digital-to-analogue converter
0	READ	magazine type and position
1	WRITE	magazine control
1	READ	magazine status
2	WRITE	grab control
2	READ	grab status
3	WRITE	grab rotation control
3	READ	grab rotation status
4	WRITE	spinner control
4	READ	spinner status
5	WRITE	lift control
5	READ	lift status
6	WRITE	shutter control
6	READ	shutter status
7	READ	miscellaneous status
F	READ	card status

Each write-byte signal triggers one-shot D22 [B-4]. This 500ms one-shot temporarily overrules reset signals from microswitches to the various functions on this card. This enables a particular action flip-flop to be set and drive the appropriate motor for a period of time long enough to release the involved microswitch. Therefore the required action can be completed.

4.17.3 SPINNER CONTROL [M-3]

D-type flip-flop D32 [N-3,0-3] accepts commands during WBYT4.

WRITE BYTE 4: spinner control

X	X	X	X	X	X	SPINH+ 1=FAST	SPINM+ 1 = ON

SPINH = spinner high speed (not supported)
SPINM = spinner motor command

Driver D37 [N-5,0-5] connects these signals to XA via current limiting resistors R26 and R27. A CLEAR = LOW from the XRA-bus resets these flip-flops. Outputs can be checked by D40 [0-5].

READ BYTE 4: spinner status

X	X	X	X	X	X	SPINH+ 1=FAST	SPINM+ 1 = ON

4.17.4 SHUTTER CONTROL [P-3]

The shutter inside the tube tower can be enabled and disabled by a command to flip-flop D38 [P-3]. If enabled, the shutter can be closed and opened by means of switches outside the PW1710 (the 3° θ switch on the goniometer).

WRITE BYTE 6: shutter control

X	X	X	X	X	X	X	SHUTE+ 1=ENABL

SHUTE = shutter control enable

Driver D37 [Q-3] connects this signal to XA via current limiting resistor R25. A CLEAR = LOW from the XRA-bus resets this flip-flop.

The output, the position of the safety circuit relay on the Shutter Spinner Driver Card, and the 3° θ switch on the goniometer can be checked by D9 [Q-5].

READ BYTE 6: shutter status

SHUTC- 0=TRUE	ANGT3- 0=TRUE	ANLE3- 0=TRUE	X	X	X	X	SHUTE+ 1=TRUE

ANGT3 = angle value is greater than 3 °θ
ANLE3 = angle value is less than or equal to 3 °θ
SHUTC = shutter is closed

4.17.5 MAGAZINE CONTROL [S-3]

The magazine is controlled by a command to two flip-flops in D21 [S-3,T-3].

WRITE BYTE 1: magazine control

X	X	X	X	X	X	MAGMD+ 1 = ON	MAGMU+ 1 = ON

MAGMD = magazine motor down command
MAGMU = magazine motor up command

Driver D5 [S-4] connects these signals to XA via current limiting resistors R13 and R12. When data is written to these flip-flops, regardless of the levels of MAGP0+ [U-1] and MAGP1+ to MAGP7+ [V,W-1], INSTP- [Y-2] keeps inputs D21-4 and D21-10 LOW, and the available data can be loaded into the flip-flops. The magazine motor starts running and MAGP0+ will go LOW within the pulse duration of INSTP-. Therefore D21 will be reset only after completion of the required action.

The end of an action is indicated by the combination of any of the signals MAGP1+ to MAGP7+ being HIGH and MAGP0+ going HIGH.

The outputs of the flip-flops are OR-ed by D23 [T-3] to develop a "magazine busy" signal MAGBS+. A CLEAR = LOW from the XRA-bus resets these flip-flops.

The outputs, together with MAGP0+ and MAGBS+, can be checked by D24 [T-5].

READ BYTE 1: magazine status

MAGBS+ 1=BUSY	MAGP0+ 1=TRUE	X	X	X	X	MAGMD+ 1 = ON	MAGMU+ 1 = ON

MAGBS = magazine drive busy
MAGP0 = magazine position bit 0 (1 time per revolution of the driving shaft = 3 times per magazine step)

The magazine position in BCD (binary coded decimal notation) and the magazine type (thin or thick sample holders; switch selected on the sample changer) can be read by D12 and D18 [V,W-5].

READ BYTE 0: magazine type and position

MAG21+ 0 ="42" 1 ="21"	MAGAZINE POSITION (1 to 42 in BCD)						
	MAGP7	MAGP6	MAGP5	MAGP4	MAGP3	MAGP2	MAGP1

MAG21+ = magazine for 21 (thick) sample holders
MAGP* = magazine position bit * (* = 7 to 1)

4.17.6 PICK UP/SET DOWN CONTROL [A-8]

The grab is controlled by a command to two flip-flops in D20 [B-8].

WRITE BYTE 2: grab control

X	X	X	X	X	X	GRBSD+ 1 = ON	GRBPU+ 1 = ON

GRBSD = grab "set down" command
GRBPU = grab "pick up" command

Driver D26 [A-9,B-9] connects these signals to XA via current limiting resistors R24 and R23. When data is written to these flip-flops, regardless ofthe levels of GRBWO+ and GRBWC+ [D-7], INSTP- [E-7] keeps inputs D20-10 and D20-4 LOW, and the available data can be loaded into the flip-flops. The grab motor starts running and the limit switch (GRBWO or GRBWC) will be released (become LOW) within the pulse duration of INSTP-. Therefore D20 will be reset only after completion of the required action. The end of an action is indicated by GRBWC+ or GRBWO+ going HIGH.

The outputs of the flip-flops are OR-ed by D23 [C-9] to develop a "grab busy" signal GRBBS+. A CLEAR = LOW from the XRA-bus resets these flip-flops.

The outputs, together with GRBBS+ and the position of the microswitches, can be checked by D30 [C-10,D-10].

READ BYTE 2: grab status

GRBBS+ 1=BUSY	GRBWO+ 1=TRUE	GRBWC+ 1=TRUE	X	X	X	GRBSD+ 1 = ON	GRBPU+ 1 = ON

GRBBS = grab drive is busy
GRBWC = grab is withdrawn and closed
GRBWO = grab is withdrawn and open

4.17.7 GRAB ROTATION CONTROL [G-8]

The direction in which the grab is to point (magazine, priority position or goniometer) is controlled by two flip-flops in D27 [G-8,H-8].

WRITE BYTE 3: grab rotation control

X	X	X	X	X	X	GRBRG+ 1 = ON	GRBRM+ 1 = ON

GRBRG = grab rotation toward goniometer
GRBRM = grab rotation toward magazine

Driver D26 [G-9] connects these signals to XA via current limiting resistors R32 and R31. When data is written to these flip-flops, regardless of the levels of GRBMA+, GRBSS+ and GRBGO+ [K-7], INSTP- [L-7] keeps inputs D27-4 and D27-10 LOW, and the available data can be loaded into the flip-flops. GRBMA+ and GRBGO+ only prevent the motor from running in the wrong direction.

The grab rotation motor starts running and the limit switch (GRBMA, GRBSS or GRBGO) will be released (becomes LOW) within the pulse duration of INSTP-. Therefore D27 will be reset only after completion of the required action. The end of an action is indicated by GRBMA+, GRBSS+ or GRBGO+ going HIGH.

The flip-flop outputs are OR-ed by D19 [J-9] to develop a "grab rotation busy" signal GRRBS+. A CLEAR = LOW from the XRA-bus resets these flip-flops.

The outputs can be checked by D36 [J-10], together with GRRBS+ and the position of the microswitches.

READ BYTE 3: grab rotation status

GRRBS+ 1=BUSY	GRBGO+ 1=TRUE	GRBSS+ 1=TRUE	GRBMA+ 1=TRUE	X	X	GRBRG+ 1 = ON	GRBRM+ 1 = ON

GRRBS = grab rotation drive is busy
GRBGO = grab is pointing to goniometer
GRBSS = grab is pointing to single sample position
GRBMA = grab is pointing to magazine

4.17.8 LIFT CONTROL [V-8]

The sample lifting mechanism is controlled by two flip-flops in D31 [W,X-8].

WRITE BYTE 5: lift control

X	X	X	X	X	X	LIFMD+ 1 = ON	LIFMU+ 1 = ON

LIFMD = lift motor down command
LIFMU = lift motor up command

Driver D26 [W-9] connects these signals to XA via current limiting resistors R29and R28. The lift motor is energised as long as one of the flip-flops is set.

The outputs of the flip-flops are OR-ed by D19 [X-9] to develop a "lift busy" signal GRRBS+. A CLEAR = LOW from the XRA-bus resets these flip-flops.

The outputs, together with LIFBS+, can be checked by D40 [X-10].

READ BYTE 5: lift status

LIFBS+ 1=BUSY	X	X	X	X	X	LIFMD+ 1 = ON	LIFMU+ 1 = ON

LIFBS = lift drive is busy

4.17.9 MISCELLANEOUS STATUS [L-3]

Some miscellaneous indicators can be read by D10 [L-5]

READ BYTE 7: miscellaneous status

X	X	X	X	X	TESTM+ 1=TEST	SAMGO+ 1=TRUE	SAMMA+ 1=TRUE

TESTM = sample changer is in TEST mode (1 = Test mode, which means that no remote control by the PW1710 is possible)
SAMGO = sample in goniometer (measuring position)
SAMMA = sample in magazine

4.17.10 CARD STATUS [R-8]

The status of all parameters on this card can be read by data bus drivers D17 [R-10] and D11 [S-10].

READ BYTE F: card status

SCHBS+ 1=BUSY	ERROR+ 1=TRUE	X	X	LIFBS+ 1=BUSY	GRRBS+ 1=BUSY	GRBBS+ 1=BUSY	MAGBS+ 1=BUSY

SCHBS = sample changer is busy (magazine, grab or grab rotation)
ERROR = maximum time error in PW1775, or no Power Supply to sample changer

When SCHBS+ goes LOW (card becomes ready), one-shot D8 [V-10] will be triggered and an interrupt INTR4- is generated (in the PW1710 this is not acknowledged by the XRA-bus controller). Also, when ERROR+ goes HIGH, interrupt INTR4- is generated.

As long as SCHBS+ is HIGH, buffer D10 [U-10] pulls the BUSYL-line LOW and switches LED V1 ON. BUSYL- is not connected on the PW1710 motherboard.

4.17.11 ANALOG MAGAZINE POSITION INDICATOR [N-8]

A digital-to-analog converter, controlled by the XRA-bus controller, offers the possibility to generate a d.c. voltage, proportional to the sample number. Six binary units are converted into one voltage unit (20 mV d.c.)

8 Bits of data are clocked into D3 [O-7] and D4 [P-7]. Binary DAC D2 [P-8] converts this bit pattern into a d.c. voltage. Op-amp D1 buffers this voltage, and attenuation network R8, R3 and R5 adjusts its full scale voltage.
At a full scale binary input of FF (in hexadecimal code), the output voltage MAGHI should be adjusted to 850 mV d.c. (each sample step equals six binary units which produces 20 mV).

WRITE BYTE 0: analogue sample position indication DAC

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0

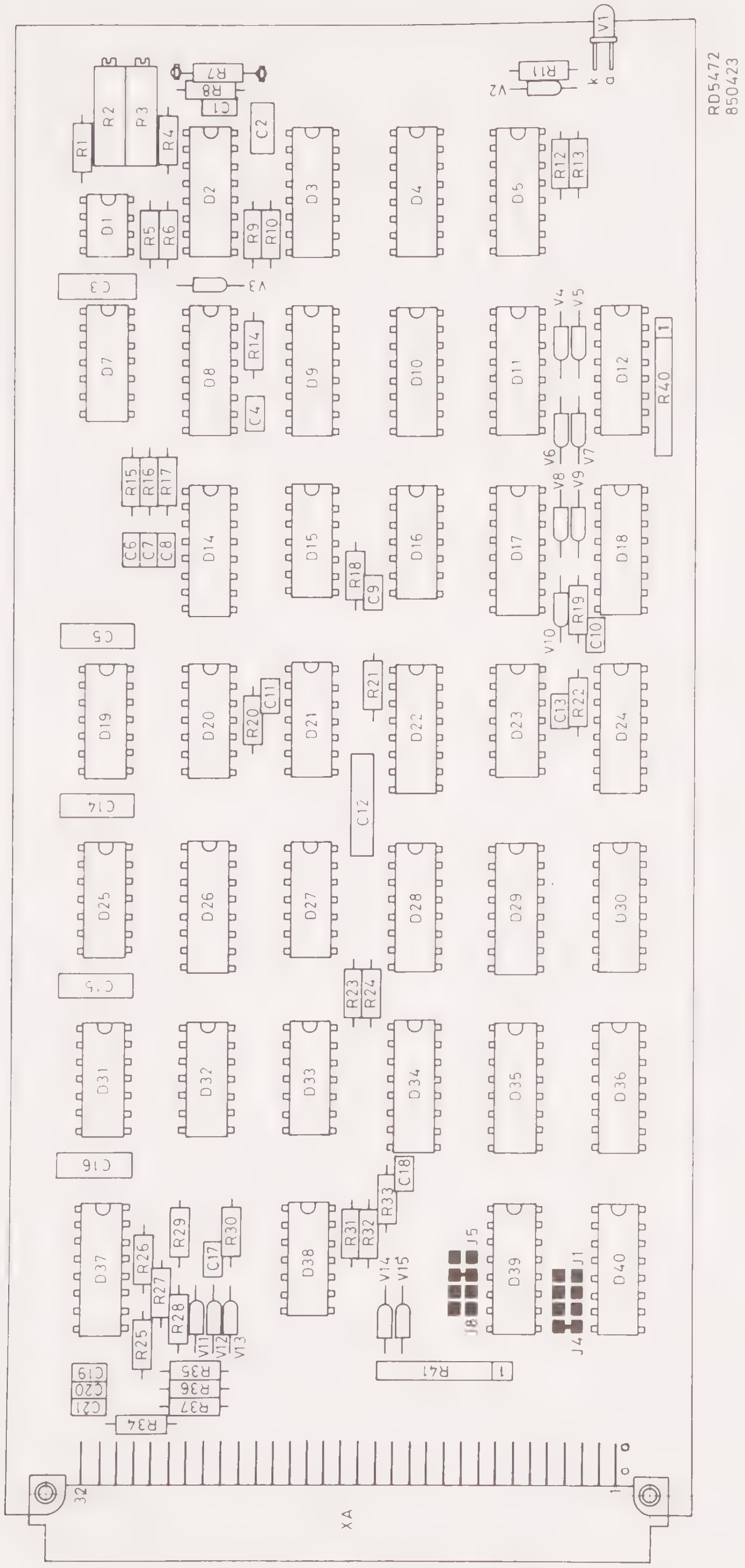

RD5472
850423
V1
k
a
R11
V2
R1
R2
R3
R4
R7
R8
C1
C2
D1
D2
D3
D4
D5
R5
R6
R9
R10
R12
R13
C3
V3
D7
D8
D9
D10
D11
D12
R14
C4
V4
V5
V6
V7
R40
R15
R16
R17
C6
C7
C8
D14
D15
D16
D17
D18
R18
C9
V8
V9
V10
R19
C10
C5
D19
D20
D21
D22
D23
D24
R20
C11
R21
C13
R22
C12
C14
D25
D26
D27
D28
D29
D30
C15
R23
R24
D31
D32
D33
D34
D35
D36
C16
C18
R33
D37
D38
D39
D40
R25
R26
R27
R28
R29
R30
C17
V11
V12
V13
R31
R32
V14
V15
J5
J8
J1
J4
R41
C19
C20
C21
R35
R36
R37
R34
32
1
XA

Figure 4.57 Changer/Spinner/Shutter Control Card, Layout

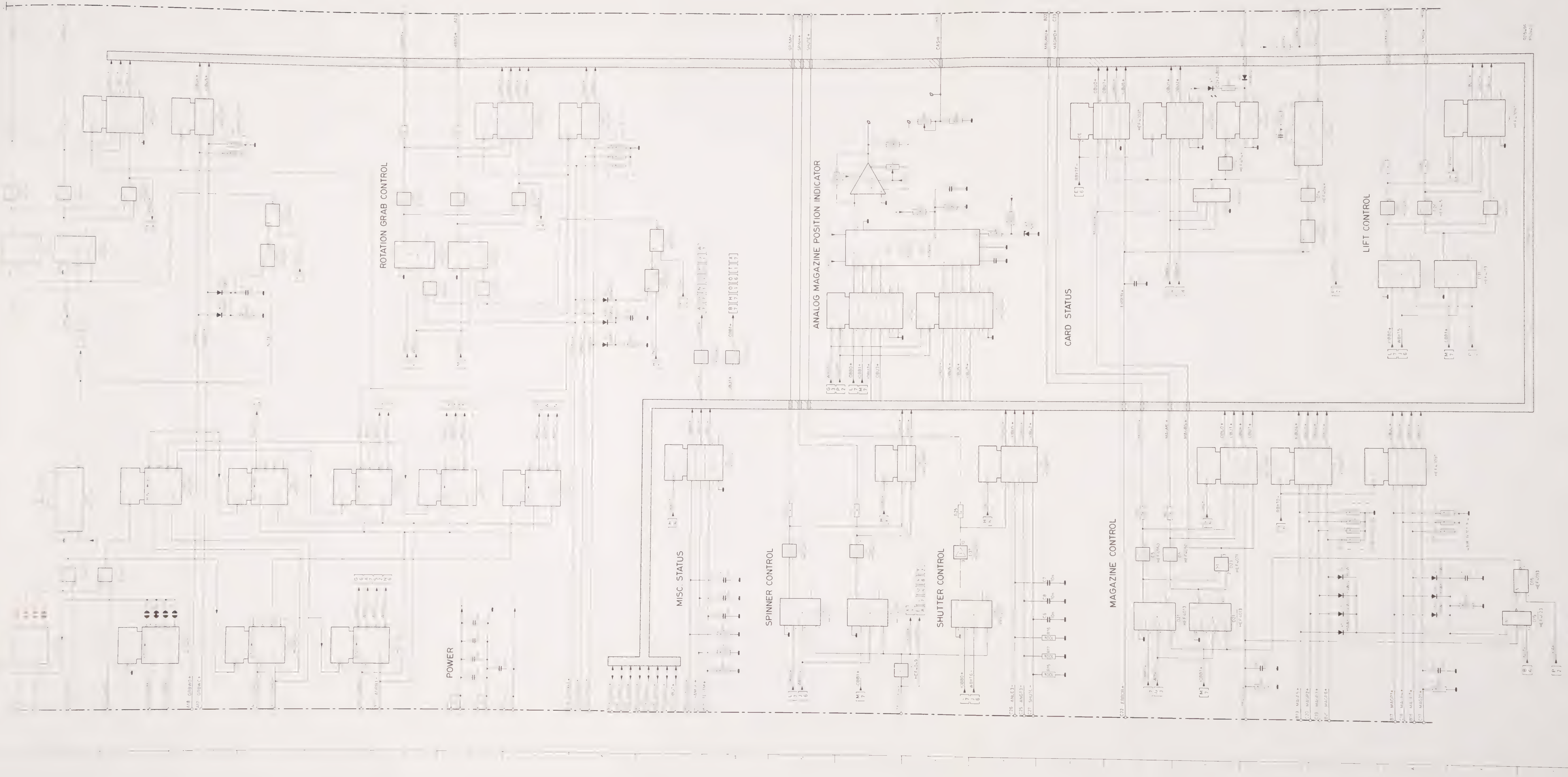

ROTATION GRAB CONTROL
ANALOG MAGAZINE POSITION INDICATOR
CARD STATUS
LIFT CONTROL
MISC STATUS
SPINNER CONTROL
SHUTTER CONTROL
MAGAZINE CONTROL
POWER

Figure 4.58 Changer/Spinner/Shutter Control Card, Schematic

4.18 SHUTTER SPINNER DRIVE CARD

4.18.1 INTRODUCTION

This card serves two purposes:

1. When the PW1775 Sample Changer Spinner is used, together with the CHANGER SPINNER SHUTTER CONTROL CARD, it supplies and controls a shutter inside the tube tower via connector XB and the SHUTTER SELECTOR which is box mounted inside the generator.

   Switches, connected to this Shutter Spinner Drive card, can open and close the shutter, provided the CHANGER SPINNER SHUTTER CONTROL card allows them to do so, and a number of safety requirements have been met.

2. When only a PW1774 sample spinner is used (without the PW1775 sample changer), this card supplies and controls the sample spinner, connected to connector XC of this card.

To perform the required functions, the following circuits are provided:

* SHUTTER SUPPLY AND CONTROL
* SPINNER SUPPLY AND CONTROL

4.18.2 SHUTTER SUPPLY AND CONTROL

Three types of shutter circuits can be connected to the SHUTTER SELECTOR (in each case a line focus is available):

*	PW1316/10	Controls shutter number 3. For this tube tower, the cable between shutter circuit and the SHUTTER SELECTOR must be modified.
*	PW1316/90	Controls shutter number 4. This tube tower can be connected to the SHUTTER SELECTOR by means of a standard one-to-one cable.
*	PW1316/91	Controls shutter number 4. As PW1316/90.

Two supply voltages are required:

300V d.c. is necessary to move the shutter from the closed to the opened position.

42V d.c. is sufficient to keep the shutter - once it is opened - in the opened position.

NOTE: In the following description, the flow in the shutter circuit is explained with a PW1316/91 connected to the SHUTTER SELECTOR. Shutter number 4 is controlled automatically by the PW1710; the others must be controlled in the usual way (on the generator's front panel).

4.18

For safety reasons, a number of parameters affect the shutter control system.

To allow the shutter to be opened, several conditions as shown in the following list must be satisfied: (Refer to adjacent figure 4.59).

In the power line:

* +42V d.c. available
* Lamps "X-rays on" in PW1775 in good condition
* Lamps LA1 and LA2 in PW1316 in good condition
* SK1 in tube tower closed by lid of radiation shield PW1771
* Switches MS8, MS7 and MS16 in PW1775 closed
* Shutter switch S15 in PW1775 not in position OFF
* Receiving slit in PW1771 safe
* +300V d.c available

In the control logic:

* 3° switch S14 in PW1771 installed

To finally open the shutter, both the "shutter enable" signal from the SYSTEM CONTROLLER via the CHANGER SPINNER SHUTTER CONTROL card must be TRUE, and the goniometer must be at an angle over 3°.

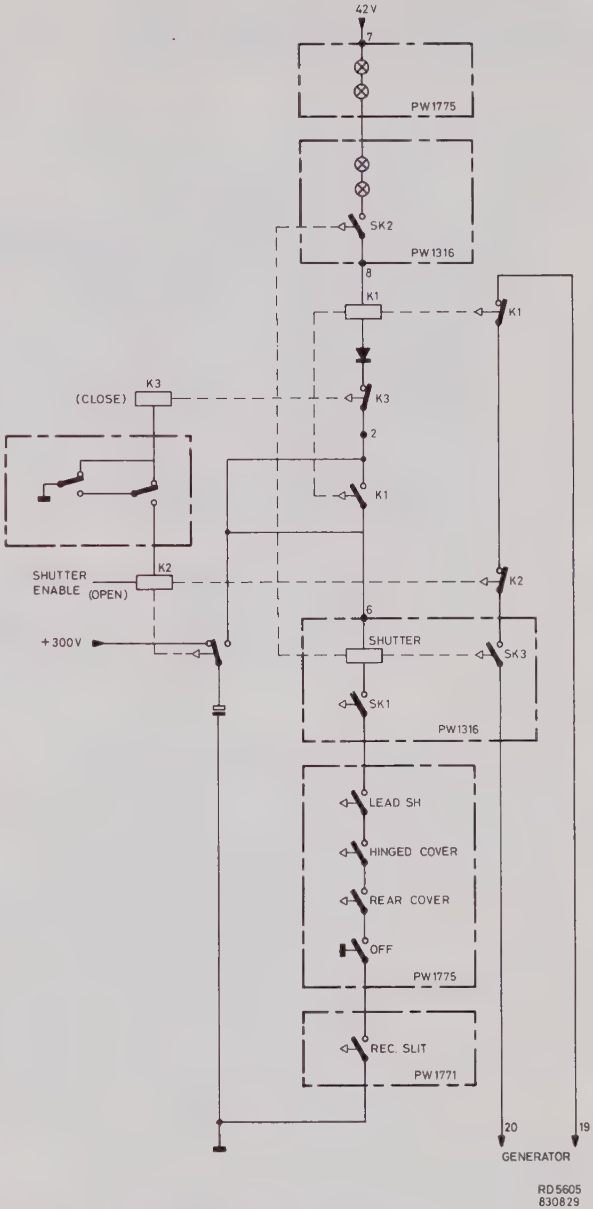

42V
7
PW1775
SK2
PW1316
8
K1
K1
K3
(CLOSE)
K3
2
K1
SHUTTER ENABLE
K2
(OPEN)
K2
6
+300V
SHUTTER
SK3
SK1
PW1316
LEAD SH
HINGED COVER
REAR COVER
OFF
PW1775
REC. SLIT
PW1771
20
19
GENERATOR
RD5605
830829

Figure 4.59 Shutter Control

By means of jumpers 18-10, 17-9 [F-14], 15-23, 16-24 [G-14] and 22-14 [F-11] on the SHUTTER SELECTOR, shutter number 4 [B-14] is connected to the SHUTTER SPINNER CARD, XB [F-9]. Normally, relay K2 [K-8, F-5] is not energised and capacitors C3 and C4 [F-5] are charged to about +300V d.c.

Figure 4.61 shows a schematic diagram of the Shutter Driver Control while figure 4.62 shows all the connections, relays, solder points and so on in the shutter circuit. Figure 4.60 shows the layout of this card.

To open the shutter, two signals are necessary:

SHUTE+ [J-4] = shutter enable (from the CHANGER SPINNER SHUTTER CONTROL)
SHUTO+ [J-4] = shutter open (from the PW1771 radiation shield)

The action of the latter of the two signals going high (which of them it is, is immaterial), causes D4 [J-5] which is built as a set-reset flip-flop to be set, such, that a negative going edge occurs on D3-5 [J-6]. This one-shot activates relay K2 [K-8] via V14 for about 0.5 seconds. Contact K2 [F-5] connects the voltage across C3 and C4 via X2-6 and jumper 17-9 to shutter number 4. V11 [F-7] prevents current from flowing to the failsafe relay K1 and associated components in the wrong direction.

Now, current can flow through the shutter, provided the receiving slit switch [F-1] indicates a safe situation, and switch S15 [E 1,2] is closed, and in the PW1775 switches MS8, MS7 and MS16 are closed. The energy in C3 and C4 is sufficient to energise the shutter coil and to open the shutter.

As a consequence of the shutter opening, SK2 [B-14] is closed and via the lamps in the PW1775 [E-3] and both LA1 and LA2 [A-14], +45V d.c. is applied continuously to the shutter, which will hold it in the opened position.
Current-driven relay K1 [F-8] also becomes energized, and contact K1 [H-5] allowes the CHANGER SPINNER SHUTTER CONTROL card to read the shutter´s status bit SHUTC+ [H-4] (shutter closed).

To close the shutter, either SHUTE+ or SHUTO+ must go LOW. When SHUTO+ goes LOW, SHUTO- goes HIGH and set-reset flip-flop D4 is set such that a negative going edge occurs on D3-11 [K-7]. Relay K3 [K-9] becomes energized for about 0.5 s and contact K3 [F-7] interrupts the current flowing through the shutter. This causes the shutter to close. When SHUTE+ goes LOW, one-shot D3 [K-7] is overruled and K3 is energized directly and continuously, preventing current from flowing through the shutter.

If the shutter failed to close after a "close" command, this will be indicated to the generator by a closed contact between pins 19 and 20 [H-14], this causes the relay K18 in the generator to be short circuited and the HT is switched off.

SK3 [A-14], K2 and K1 [G-8] are connected in series via jumpers 15-23 and 16-24 [H-14]. When the shutter is open, SK3 and K2 are closed, but K1 is open, so there is an open contact between pins 19 and 20. When the shutter is to be closed, relay K3 switches the shutter OFF (and after a delay - caused by C8 [E-8] - K1 OFF). SK3 will open and (after a delay) K1 will close, and as a result the contact between pins 19 and 20 is still open.

If the shutter failed to close, even after removal of the supply voltage, SK3 will remain closed, and this results in a closed contact between pins 19 and 20, indicating a faulty situation to the generator. Uncertainties during shutter switching could look like a fault condition, to prevent this occurring K2 [G-8] temporarely opens this circuit during the shutter opening.

4.18

4.18.3 SPINNER SUPPLY AND CONTROL (Refer to figure 4.63)

Without a PW1775 sample changer, the PW1774 sample spinner is supplied and controlled via connector XC. The controlling command comes directly from the system controller card (SPINM-).

The control circuit is powered from the 48V a.c. When the spinner cable is connected [C-8], XC-7 and XC-6 are interconnected. V8 [C-2] rectifies and C9 [B-2] buffers the voltage. R14 and V9 [B-3] stabilizes this unregulated voltage to -12V d.c., which powers D1 [B-5]. Led V17 [B-6] indicates the presence of this voltage.

Transistor V5 [A-4] is configured as a zero crossing detector to guarantee smooth switching. If 48V~2 is more positive than 48V~1, V5 conducts and pulls D1-3 HIGH (0V). If 48V~2 is more negative than 48V~1, V5 is reverse biased and D1-3 is LOW (-12V). This square wave is the clock signal for D1.

R8 and V7 [B-4] perform a power-up reset function. At a supply voltage below 3V d.c., V7 will not conduct and D1-4 is relatively HIGH (=reset). At higher supply voltages, this level is fixed to 3V d.c. At 12V d.c., this level is relatively LOW (= no reset).

A LOW on SPINM- [D-1] causes the transistor in optocoupler D5 [C-2] to conduct. The voltage across R13 [D-2] makes the voltage on D1-5 [B-5] relatively HIGH (0V), and at the next trigger pulse on D1-3, a "1" will be clocked into the flip-flop. D1-2 becomes LOW (-12V), both V4 and V1 [A-6] start to conduct.

The spinner motor inside the PW1774 will be powered. This power is detected by optocoupler D6 [B-7] which generates a square wave with mains frequency over R28. This frequency triggers and retriggers one-shot D2 [D-7], which generates a continuous "HIGH" on SPNBY+ [E-1] (spinner busy). This signal can be checked by the SYSTEM CONTROLLER CARD.

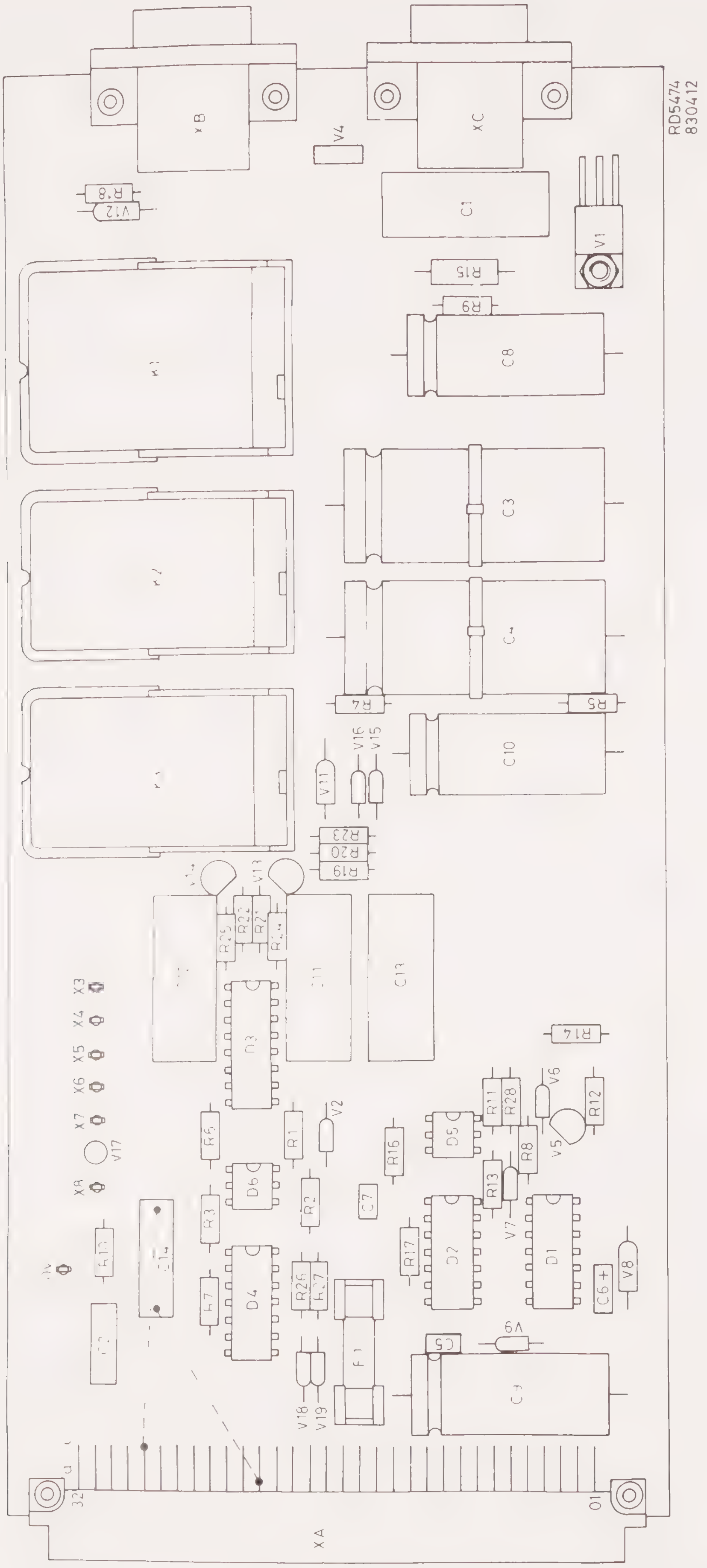

RD5474
830412
XB
XC
V4
R8
V12
C1
V1
R15
R9
C8
C3
C4
R4
R5
V16
V15
V11
C10
R23
R20
R19
V14
V13
R25
R22
R21
R24
D3
R14
V6
R11
R28
R12
V5
R8
D5
R13
V7
R16
R1
V2
R6
X3
X4
X5
X6
X7
V17
X8
D6
R3
R2
C7
R17
D2
D1
V8
C6 +
R26
R27
D4
C5
V9
F1
V18
V19
32
01
XA

Figure 4.60 Shutter/Spinner Driver Control Card, Layout

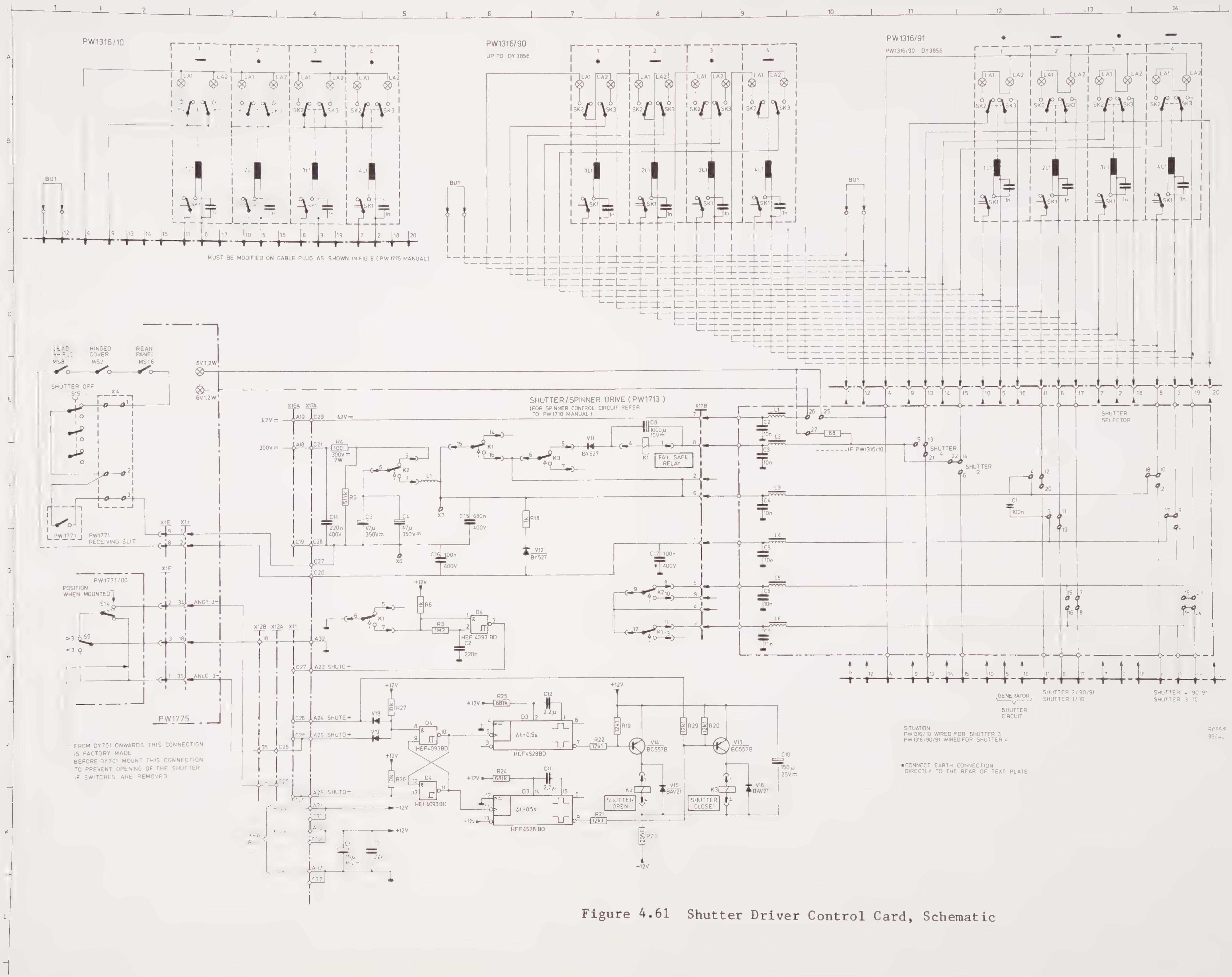

PW1316/10
PW1316/90
UP TO DY3856
PW1316/91
PW1316/90 DY3856
BU1
LA1
LA2
SK1
SK2
SK3
1L1
2L1
3L1
4L1
1n
MUST BE MODIFIED ON CABLE PLUG AS SHOWN IN FIG 6 (PW 1775 MANUAL)
LEAD SHIELD MS8
HINGED COVER MS7
REAR PANEL MS16
SHUTTER OFF S15
X4
6V1,2W
PW1771
PW1771 RECEIVING SLIT
X1E
X1J
X1F
PW1771/00
POSITION WHEN MOUNTED
S14
S9
>3
<3
PW1775
– FROM DY701 ONWARDS THIS CONNECTION IS FACTORY MADE BEFORE DY701 MOUNT THIS CONNECTION TO PREVENT OPENING OF THE SHUTTER IF SWITCHES ARE REMOVED
SHUTTER/SPINNER DRIVE (PW1713)
(FOR SPINNER CONTROL CIRCUIT REFER TO PW1710 MANUAL)
X16A
X17A
X17B
42V
300V
R4 100 300V 7W
R5 511k
C14 220n 400V
C3 47µ 350V
C4 47µ 350V
C15 680n 400V
C16 100n 400V
C17 100n 400V
C8 1000µ 10V
K1
K2
K3
L1
V11 BY527
V12 BY527
R18 1k
FAIL SAFE RELAY
X6
X7
R6 1k
R3 1M2
D4 HEF 4093 BD
C2 220n
ANOT 3
ANLE 3
X12B
X12A
X11
A23 SHUTC+
A24 SHUTE+
A29 SHUTO+
A25 SHUTO−
+12V
−12V
R27 10k
R26 10k
V18
V19
HEF4093BD
R25 681k
R24 681k
C12 2,2µ
C11 2,2µ
D3
Δt = 0,5s
HEF4528BD
R22 12k1
R21 12k1
R19 12k1
R29 12k1
R20 12k1
V14 BC557B
V13 BC557B
V15 BAV21
V16 BAV21
C10 150µ 25V
R23 205E
SHUTTER OPEN
SHUTTER CLOSE
L2
L3
L4
L5
C1 100n
68
IF PW1316/10
SHUTTER 1
SHUTTER 2
SHUTTER SELECTOR
GENERATOR
SHUTTER CIRCUIT
SHUTTER 2/90/91
SHUTTER 1/10
SHUTTER 4 90 91
SHUTTER 3 10
SITUATION
PW1316/10 WIRED FOR SHUTTER 3
PW1316/90/91 WIRED FOR SHUTTER 4
• CONNECT EARTH CONNECTION DIRECTLY TO THE REAR OF TEXT PLATE

Figure 4.61 Shutter Driver Control Card, Schematic

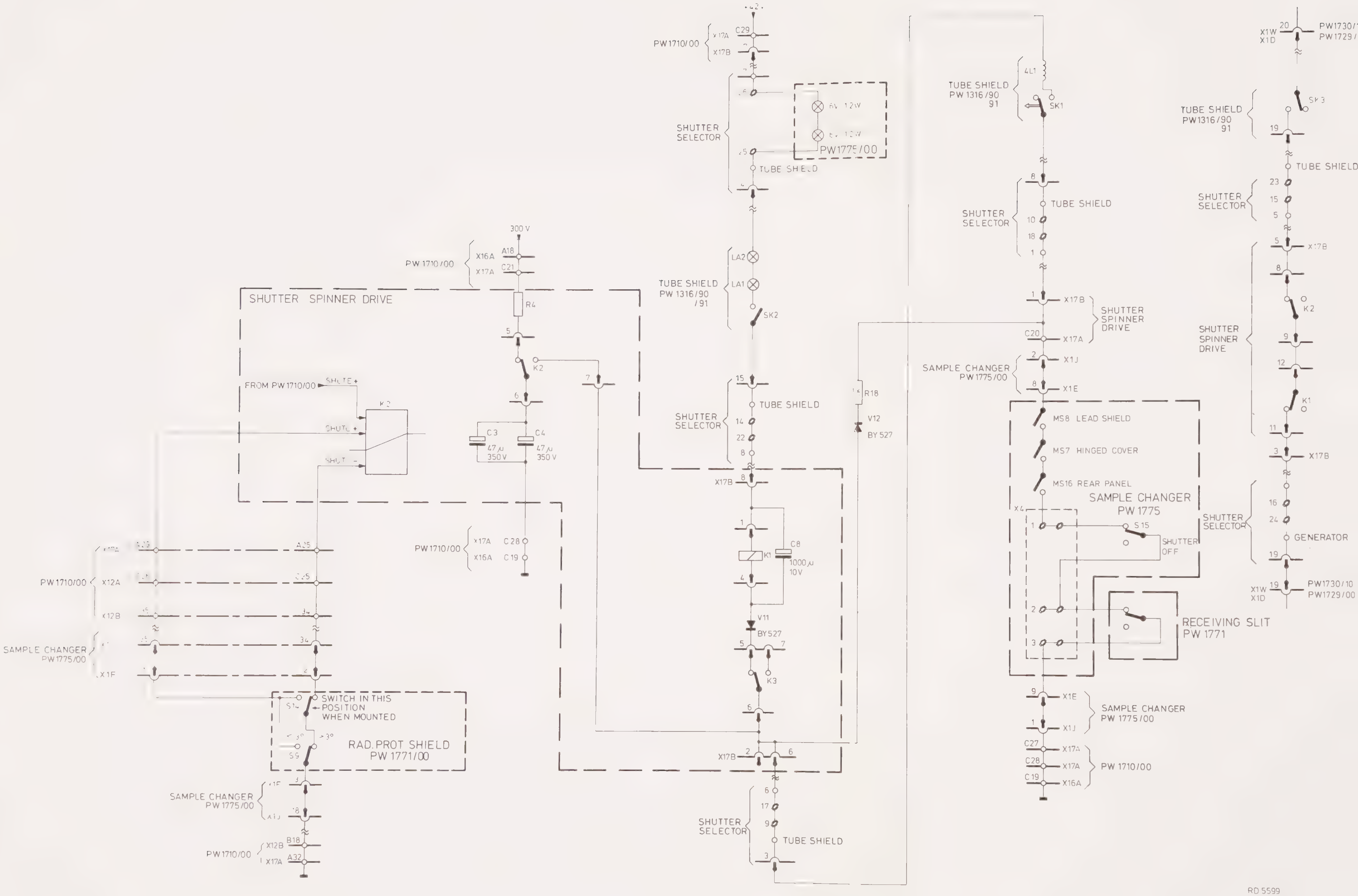
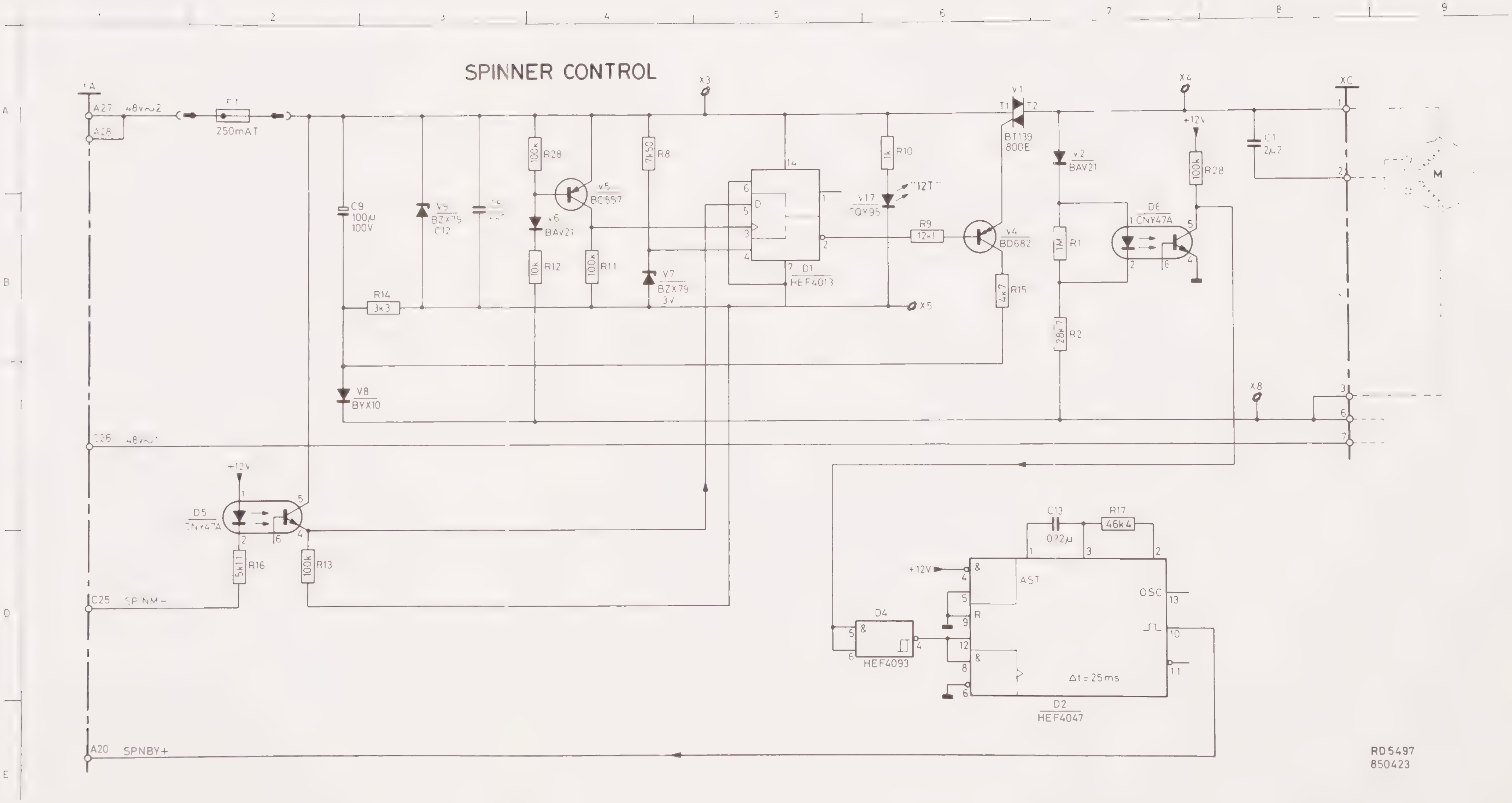

+42V
PW1710/00
X17A
X17B
C29
SHUTTER SELECTOR
6V 12W
6V 12W
PW1775/00
TUBE SHIELD
LA2
LA1
TUBE SHIELD PW 1316/90 /91
SK2
300 V
PW 1710/00
X16A
X17A
A18
C21
SHUTTER SPINNER DRIVE
R4
K2
FROM PW1710/00
SHUTE +
SHUTC +
SHUT −
C3
47 µ 350 V
C4
47 µ 350 V
PW1710/00
X17A
X16A
C 28
C 19
PW1710/00
X12A
X12B
A25
C25
34
SAMPLE CHANGER PW1775/00
X1F
SWITCH IN THIS POSITION WHEN MOUNTED
S14
< 3°
> 3°
S9
RAD.PROT SHIELD PW 1771/00
SAMPLE CHANGER PW1775/00
PW1710/00
X12B
X17A
B18
A32
15
TUBE SHIELD
SHUTTER SELECTOR
14
22
8
X17B
K1
C8
1000 µ 10V
V11
BY527
K3
X17B
SHUTTER SELECTOR
6
17
9
TUBE SHIELD
3
R18
V12
BY 527
4L1
TUBE SHIELD PW 1316/90 91
SK1
SHUTTER SELECTOR
TUBE SHIELD
10
18
1
X17B
C20
X17A
SHUTTER SPINNER DRIVE
SAMPLE CHANGER PW1775/00
X1J
X1E
MS8 LEAD SHIELD
MS7 HINGED COVER
MS16 REAR PANEL
SAMPLE CHANGER PW 1775
X4
S 15
SHUTTER OFF
RECEIVING SLIT PW 1771
X1E
X1J
SAMPLE CHANGER PW 1775/00
C27
C28
C19
X17A
X17A
X16A
PW 1710/00
X1W
X1D
20
PW1730/1
PW1729/
SK3
TUBE SHIELD PW1316/90 91
19
TUBE SHIELD
SHUTTER SELECTOR
23
15
5
X17B
K2
SHUTTER SPINNER DRIVE
9
12
K1
11
3
X17B
SHUTTER SELECTOR
16
24
GENERATOR
19
X1W
X1D
PW1730/10
PW1729/00
RD 5599
830907

Figure 4.62 Shutter Control Line Ci


SPINNER CONTROL
1 2 3 4 5 6 7 8 9
A B D E
A27 48V~2
A28
F1 250mAT
C9 100µ 100V
V9 BZX79 C12
R28 100k
V5 BC557
V6 BAV21
R12 10k
R11 100k
R8 7k50
V7 BZX79 3V
R14 3k3
D1 HEF4013
X3
X5
R10 1k
V17 CQY95 "12T"
R9 12k1
V4 BD682
R15 4k7
V1 T1 T2 BT139 800E
V2 BAV21
R1 1M
R2 28k7
D6 CNY47A
+12V
R28 100k
C1 2µ2
X4
XC
M
V8 BYX10
X8
C26 48V~1
D5 CNY47A
R16 5k11
R13 100k
C25 SPNM−
C13 0.22µ
R17 46k4
D4 HEF4093
AST
OSC
R
Δt = 25ms
D2 HEF4047
A20 SPNBY+
RD5497
850423

4.18

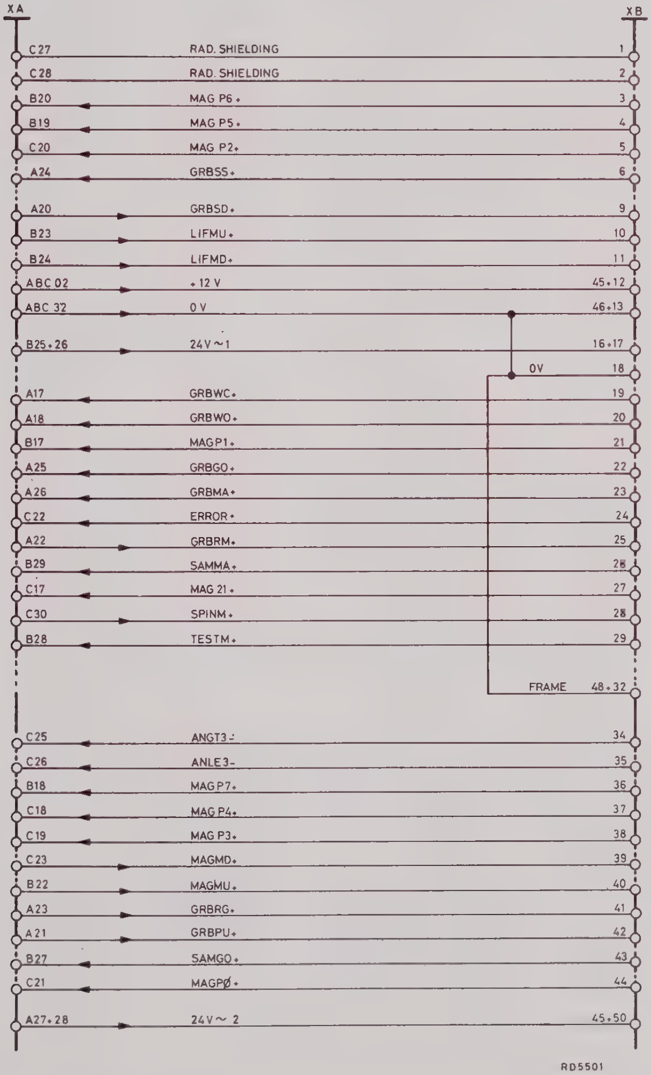
Figure 4.63 Spinner Driver, Schematic

4.19 CABLE CARD "SHUTTER/CHANGER"

4.19.1 INTRODUCTION

This cable card carries signals and voltages to and from the Changer/Spinner cable and the motherboard.

Figure 4.64 shows the wiring for this cable card.


XA
XB
C27 RAD. SHIELDING 1
C28 RAD. SHIELDING 2
B20 MAG P6+ 3
B19 MAG P5+ 4
C20 MAG P2+ 5
A24 GRBSS+ 6
A20 GRBSD+ 9
B23 LIFMU+ 10
B24 LIFMD+ 11
ABC 02 +12 V 45+12
ABC 32 0 V 46+13
B25+26 24V~1 16+17
0V 18
A17 GRBWC+ 19
A18 GRBWO+ 20
B17 MAGP1+ 21
A25 GRBGO+ 22
A26 GRBMA+ 23
C22 ERROR+ 24
A22 GRBRM+ 25
B29 SAMMA+ 26
C17 MAG 21+ 27
C30 SPINM+ 28
B28 TESTM+ 29
FRAME 48+32
C25 ANGT3- 34
C26 ANLE3- 35
B18 MAGP7+ 36
C18 MAG P4+ 37
C19 MAG P3+ 38
C23 MAGMD+ 39
B22 MAGMU+ 40
A23 GRBRG+ 41
A21 GRBPU+ 42
B27 SAMGO+ 43
C21 MAGP0+ 44
A27+28 24V~ 2 45+50
RD5501

4.19

Figure 4.64 Cable Card Shutter Control

4.20 MULTIPLE OUTPUT POWER SUPPLY CARD

4.20.1 INTRODUCTION

This card - together with the POWER UNIT - provides all the necessary supply voltages for the PW1710 with all its options. Some of the voltages are only passed by this card to the motherboard of the system. Others are regulated andmonitored. A visual indication of the presence of all the voltages is provided.

The following circuits are provided:

+5V for TTL-compatible logic (4.20.2)
+12V for XRA-bus compatible logic and Opamps (4.20.3)
-12V for Opamps (4.20.4)
+24V for pre-amplifiers in detectors (4.20.5)
+24V for current loop interfaces (4.20.6)
Voltage monitor (4.20.7)
Presence indication for miscellaneous voltages (4.20.8)
  300V d.c. and 45V d.c. for the shutter circuit
  20V a.c. and 5V a.c. for the stepping motor
  24/48V a.c. for the sample changer
  40V a.c. and 9V a.c. for the display

The schematic diagram for this card is shown in figure 4.67, and the layout is given in figures 4.65 and 4.66.

4.20.2 +5V d.c. SUPPLY

This circuitry comprises a voltage regulator (except the power transistor), a current limiter with foldback, and a crowbar. The function is based on a /uA723 voltage regulator D4 [B-3]. This chip needs a supply voltage on V+ (pin 12) of at least +9.5V d.c.

A built-in reference provides +7.15 V d.c. at Vref (pin 6). Resistors R50, R49 and Radj attenuate this voltage to a setpoint value of +5V d.c. at the non-inverting input pin 5 (Vni).

A comparator in the i.c. compares this setpoint to the measured value, connected to the inverting input Vi (pin 4). The result of the comparison is tranferred to the control output Vout (pin 10), which is connected to the base of the power transistor in the POWER UNIT.

The output current is measured accross R63, R64 and R65 [A-4] (together making a resistance of 0.4 ohm). At the maximum current value of 4A, the voltage drop across these resistors is 1.6V d.c., therefore the voltage on the divider circuit R52 and R53 is +6.6V d.c. This results in a voltage at input Vcl (pin 2) of +5.8V d.c.

The output voltage is also connected to Vcs. When the voltage difference between Vcl and Vcs exceeds 0.8V d.c., the control output voltage at Vout will be reduced, and a lower output voltage at XB pins A01, B01 and C01 is the result. If this output is completely short-circuited to ground, R52, R53 and R54 reduce the maximum output current to 2A (foldback characteristic), this protects the series regulator transistor from being destroyed by excessive heat.

A crowbar is built around thyristor V36 [B-2]. If for any reason the output voltage exceeds +6.5V d.c., transistor V38 [B-5] starts to conduct, and triggers V36. V36 short-circuits the input voltage Vin until the fuse in the POWER UNIT is blown. Delay circuit R56 and C12 [A-4] prevents the thyristor from being fired by spikes.

The optical indication of this +5V d.c. is described in the VOLTAGE MONITOR circuit description (paragraph 4.20.8).

4.20.3 +12V d.c. SUPPLY

The unregulated voltage enters the card via XA pin 4 [D-1]. The 7812 three-terminal positive voltage regulator V43 [D-2] stabilizes this voltage to +12V d.c. and limits the output current to about 1A. At full short-circuit to ground, the output current will be limited to about 0.35A.

A crowbar is built around thyristor V41. If for any reason the output voltage exceeds +15.7V d.c., transistor V40 starts to conduct, and triggers V41. V41 short-circuits the output voltage. Delay circuit R60 and C16 prevents the thyristor from being fired by spikes.

The optical indication of this +12V d.c. is described in the VOLTAGE MONITOR circuit description (para 4.7.1.8).

4.20.4 -12V d.c. SUPPLY

The unregulated voltage enters the card via XA pin 9 [F-1]. The 7912 three-terminal negative voltage regulator V16 [F-1] stabilizes this voltage to -12V d.c. and limits the output current to about 1A. At full short-circuit to ground, the output current will be limited to about 0.35A.

A crowbar is built around thyristor V22 [F-4]. If for any reason the output voltage exceeds -16V d.c., transistor V19 [F-3] starts to conduct, and triggers V22. V22 short-circuits the output voltage. Delay circuit R8 and C3 [F-3] prevents the thyristor from being fired by spikes.

The optical indication of this -12V d.c. is given by LED V8 [F-5]. At voltages more negative than -10V d.c., transistor V23 [F-5] conducts and V8 is switched ON.

4.20.5 +24V d.c. SUPPLY

The unregulated voltage enters the card via XA pin 22 [G-1]. The 7824 three-terminal negative voltage regulator V31 [G-1] stabilizes this voltage to +24V d.c. and limits the output current to about 1A. At full short-circuit to ground, the output current will be limited to about 0.15A.

A crowbar is built around thyristor V33 [G-4]. If for any reason the output voltage exceeds +34V d.c., transistor V32 [G-3] starts to conduct, and triggers V33. V33 then short-circuits the output voltage. Delay circuit R33 and C6 [G-3] prevents the thyristor from being fired by spikes.

The optical indication of this +24V d.c. is given by LED V5 [G-5]. At voltages over +19V d.c., transistor V34 [G-5] conducts and V5 is switched ON.

4.20.6 CURRENT LOOP SUPPLY

This circuit generates a voltage of approximately +24V. At output voltages below +25.5V d.c., zener diode V28 [I-2] does not conduct, and therefore transistor V35 is fully turned ON. Over +25.5V d.c. the base voltage of V35 is limited and this reduces the output voltage to approximately +24V d.c.

A coarse optical indication is provided by LED V9.

4.20.7 VOLTAGE MONITOR

Two levels are specified for the +5V d.c. supply:

an upper limit of +5.25V d.c.

a lower limit of +4.75V d.c.

When the +5V d.c. is out of specification, the RESET+ signal [J-9] is pulled HIGH.

If the +12V d.c. is sufficiently high to power D4 [B-3] properly, it (the +12V) also turns transistor V30 [J-1] ON. LED V13 [K-1] is switched ON, providing the optical indication for the +12V d.c. The ultra-stable voltage reference diode V25 [K-2] is also biased. R30, Radj and R29 [K-2] attenuate this voltage such that at opamp output D2-7 [K-3], a voltage of +5.25V d.c. is available (upper limit). This voltage is divided by R25 and R22 [L-3] to generate +4.75V d.c. (lower limit).

Via D2-3 and D2-9 [K-4] the +5V d.c. is compared to these limits. If the +5V d.c. is within these limits, both D2-1 and D2-8 are HIGH. Transistor V24 [L-5] is turned ON and LED V24 [L-5] is switched ON, providing the optical indication for the +5V d.c. (PON). Transistor V42 [J-9] is turned OFF and RESET+ is LOW.

Resistors R26 and R23 provide a positive feedback for the +5.25V d.c. limit detector (hysterysis effect). Resistors R21 and R20 provide a positive feedback for the +4.75V d.c. limit detector.

A number of voltages only use this card as a connection between the POWER UNIT and the MOTHER BOARD. This card provides a coarse optical indication of them by single phase rectifiers and LEDs, and one gas discharge tube. The voltages involved are:

300V d.c. and 45V d.c. for the shutter circuit

20V a.c. and 5V a.c. for the stepping motor

24/48V a.c. for the sample changer

40V a.c. and 9V a.c. for the display

4.21 POWER UNIT PW1710

4.21.1 INTRODUCTION

This 19" wide unit, together with the MULTIPLE OUTPUT POWER SUPPLY card, provides all the power for the PW1710 and all its options.

The unit derives all the required voltages from a 220V a.c. mains supply, it consists of the following parts:

- Mains filter - mains switch - mains fuses
- Voltage transformers
- Secondary fuses
- Rectifiers - buffer capacitors - series regulator transistor (+5V d.c.)
- Connector for optional table-top cabinet.

The schematic diagram for this unit is shown in figure 4.69, and the layout is given in figure 4.68.

4.21.2 PRIMARY CIRCUIT

Mains voltage is applied to the two voltage transformers via the mains filter Z100 [A-3] and mains switch S100. Two mains fuses F100 [A-3] and F101 [D-3] are also in the circuit. The transformers have thermal protection.

The optional table-top cabinet PW1719 can be connected to the 220V a.c., via connector X.103.

4.21.3 +5V a.c. SUPPLY

Output S2 [S-4] of the upper transformer provides the a.c. voltage for the +5V d.c. circuit. It is rectified by rectifier V100 and connected to the darlington power transistor V101 [A-7] via buffer capacitors C102 to C105 and fuse F119. Transistor V101 [A-7] regulates the voltage, the base of the transistor (+5V ctrl) is controlled via X102-3.

The AC voltage from S2 is also connected to the RECTIFIER CARD [D-6] where optocouplers V4 and V5 perform a zero-crossing detector function. However, its output is not used in the PW1710.

4.21.4 SAMPLE CHANGER SUPPLY

Outputs S5A and S5B of the upper transformer provide either, 24V a.c. or 48V a.c. for the various sample changers. Selection of the required voltage is made by connecting X103-14 to either F115 (24V a.c.) or F114 (48V a.c.).

In early versions of the POWER UNIT, only one fuse is available, and selection is made by connecting tap 16 (24V a.c.) or 20 (48V a.c.).

4.21

4.21.5 LOW-VOLTAGE SUPPLIES

Outputs S3, S4 and S6 of the upper transformer provide a.c. voltages for the +12V d.c., -12V d.c. and +24V d.c. circiuts. Rectifiers are provided by the RECTIFIER CARD (V2 and V3 are connected in parallel to meet the current requirements). Some of the buffer capacitors are also on the Rectifier Card.

4.21.6 MISCELLANEOUS d.c. VOLTAGES

Outputs S4, S5 and S7 of the lower transformer provide a.c. voltages for the current loop interface and the shutter circuit. Rectifiers and buffer capacitors are provided by the RECTIFIER CARD.

4.21.7 MISCELLANEOUS a.c. VOLTAGES

Outputs S2, S6 and S3 of the lower transformer provide a.c. voltages for the stepping motor supplies and the display supply.

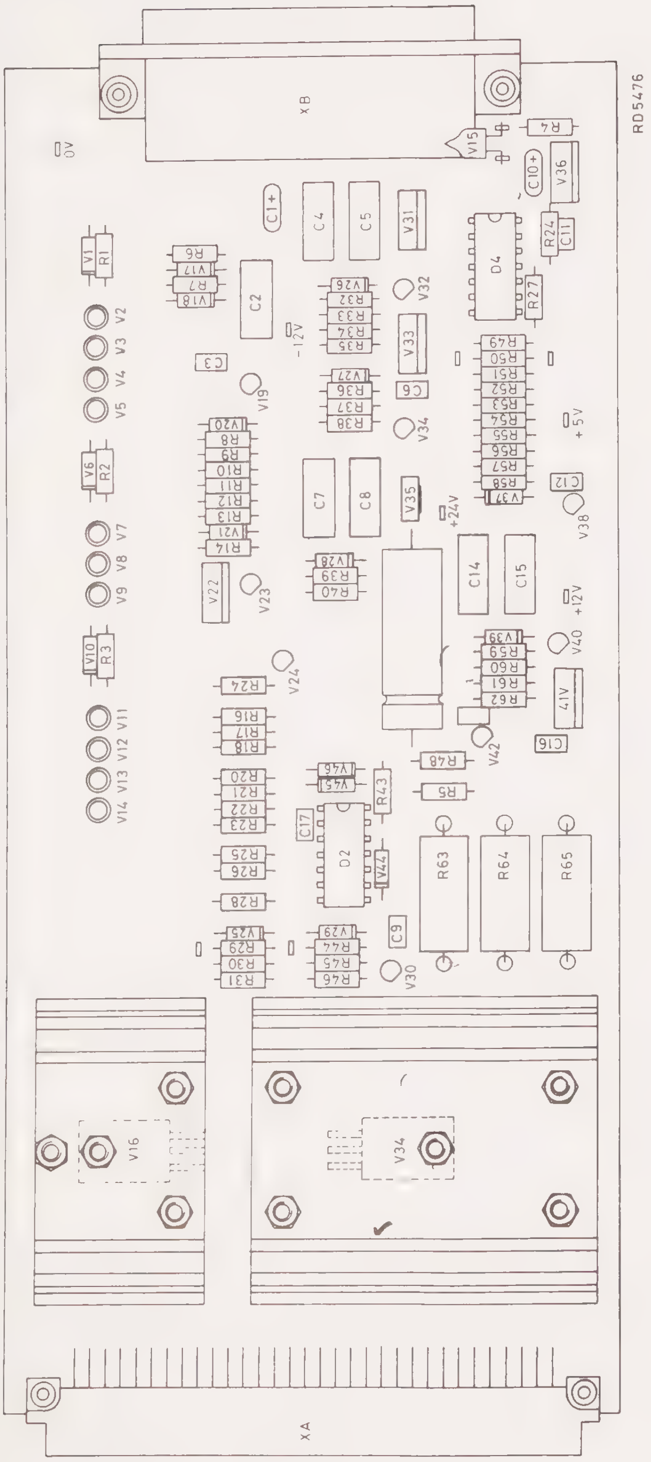
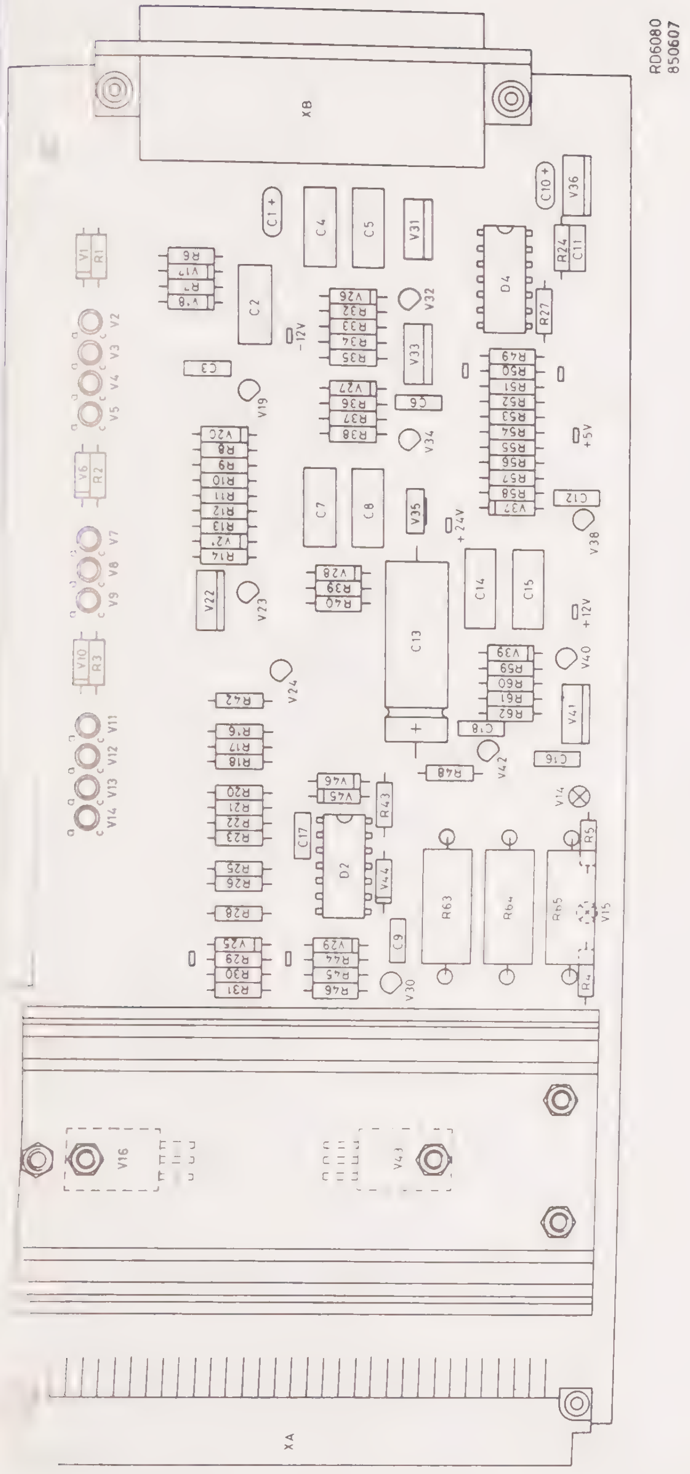

RD5476
XB
XA
0V
-12V
+5V
+24V
+12V
C1+
C2
C3
C4
C5
C6
C7
C8
C9
C10+
C11
C12
C14
C15
C16
C17
D2
D4
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R16
R17
R18
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R43
R44
R45
R46
R48
R49
R50
R51
R52
R53
R54
R55
R56
R57
R58
R59
R60
R61
R62
R63
R64
R65
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
V11
V12
V13
V14
V15
V16
V17
V18
V19
V20
V21
V22
V23
V24
V25
V26
V27
V28
V29
V30
V31
V32
V33
V34
V35
V36
V37
V38
V39
V40
V41
V42
V44
V45
V46

Figure 4.65 Multiple Output Power Supply (Old version), Layout


RD6080
850607
XB
XA

igure 4.66 Multiple Output Power Supply (New version), Layout

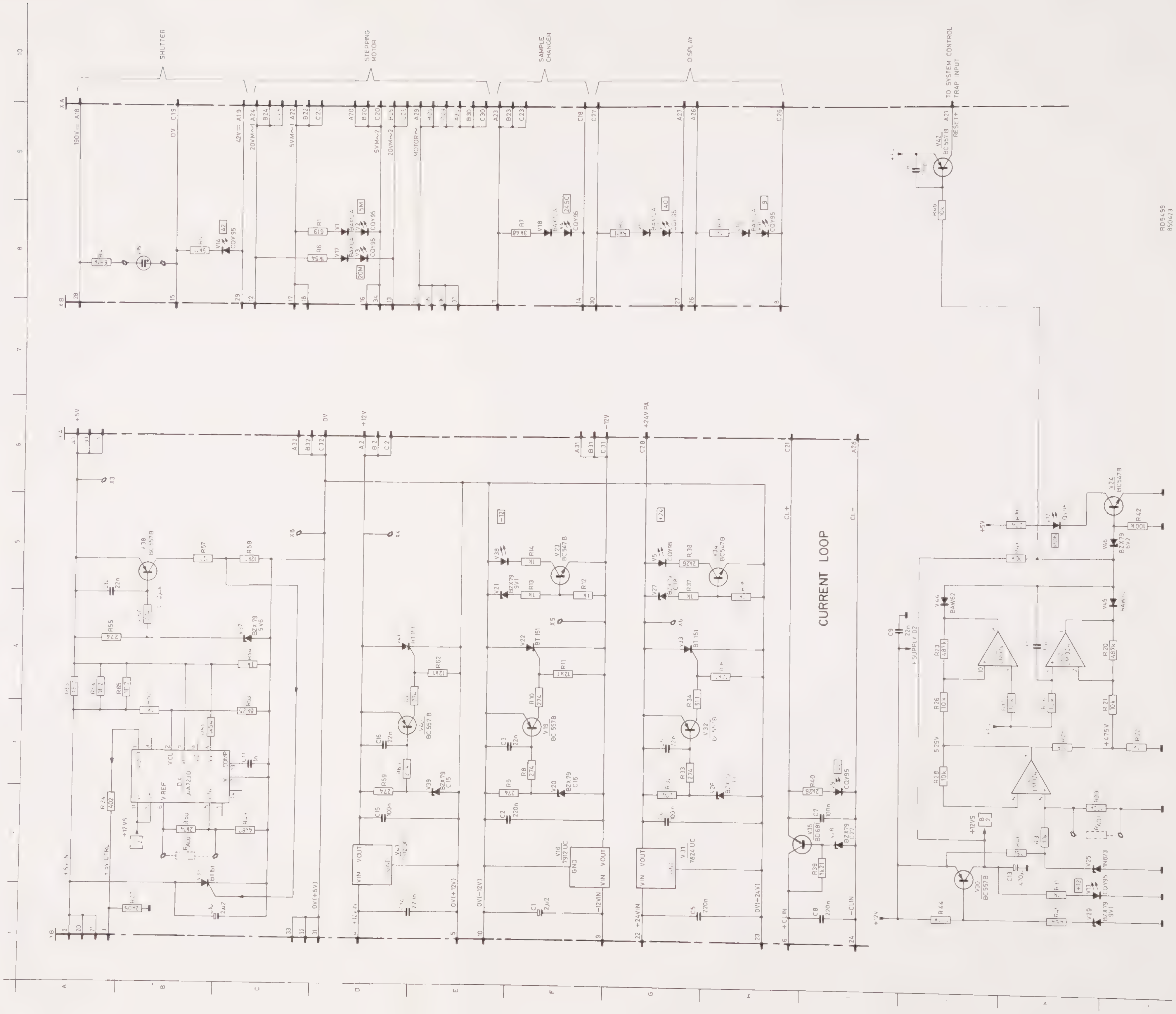
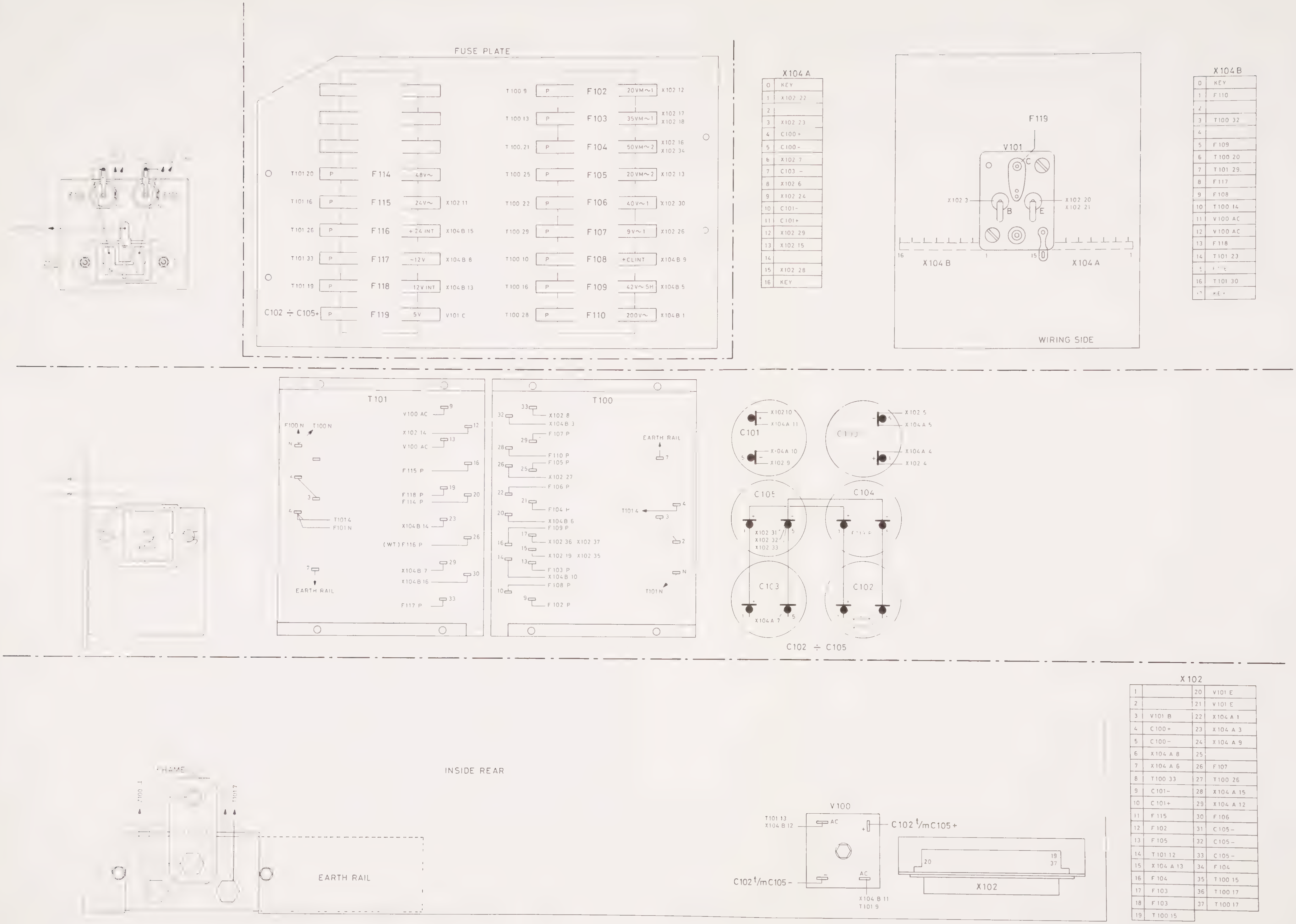

SHUTTER
STEPPING MOTOR
SAMPLE CHANGER
DISPLAY
TO SYSTEM CONTROL TRAP INPUT
CURRENT LOOP

Figure 4.67 Multiple Output Power Supply, Schematic


FUSE PLATE
T101 20 P F114 48V~
T101 16 P F115 24V~ X102 11
T101 26 P F116 +24 INT X104B 15
T101 33 P F117 -12V X104B 8
T101 19 P F118 12V INT X104B 13
C102 ÷ C105+ P F119 5V V101 C
T100 9 P F102 20VM~1 X102 12
T100 13 P F103 35VM~1 X102 17 X102 18
T100 21 P F104 50VM~2 X102 16 X102 34
T100 25 P F105 20VM~2 X102 13
T100 22 P F106 40V~1 X102 30
T100 29 P F107 9V~1 X102 26
T100 10 P F108 +CLINT X104B 9
T100 16 P F109 42V~5H X104B 5
T100 28 P F110 200V~ X104B 1
F119
V101
X102 3
B
E
C
X102 20
X102 21
X104 B
X104 A
WIRING SIDE
T101
T100
EARTH RAIL
C101
C100
C105
C104
C103
C102
C102 ÷ C105
INSIDE REAR
EARTH RAIL
V100
C102 +/m C105 +
C102 +/m C105 −
X102

X104 A

0	KEY
1	X102 22
2	
3	X102 23
4	C100+
5	C100-
6	X102 7
7	C103 -
8	X102 6
9	X102 24
10	C101-
11	C101+
12	X102 29
13	X102 15
14	
15	X102 28
16	KEY

X104 B

0	KEY
1	F110
2	
3	T100 32
4	
5	F109
6	T100 20
7	T101 29.
8	F117
9	F108
10	T100 14
11	V100 AC
12	V100 AC
13	F118
14	T101 23
15	[illegible]
16	T101 30
17	KEY

X102

1		20	V101 E
2		21	V101 E
3	V101 B	22	X104 A 1
4	C100+	23	X104 A 3
5	C100-	24	X104 A 9
6	X104 A 8	25	
7	X104 A 6	26	F107
8	T100 33	27	T100 26
9	C101-	28	X104 A 15
10	C101+	29	X104 A 12
11	F115	30	F106
12	F102	31	C105-
13	F105	32	C105-
14	T101 12	33	C105-
15	X104 A 13	34	F104
16	F104	35	T100 15
17	F103	36	T100 17
18	F103	37	T100 17
19	T100 15		

Figure 4.68 Power Supply Assembly, Layout

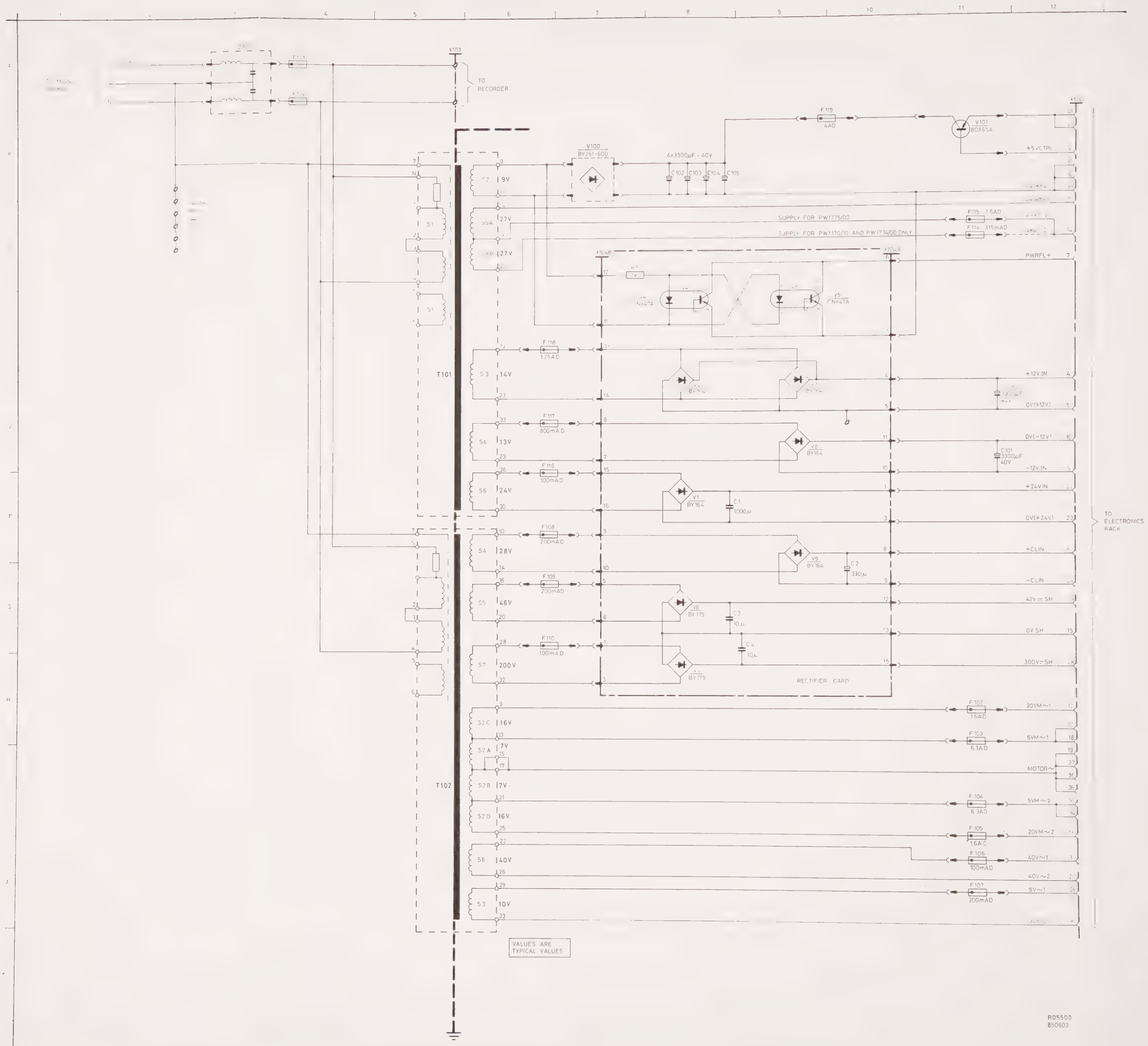

X103
TO RECORDER
V100
BY261-600
4x3300µF - 40V
C102
C103
C104
C105
F119
4AD
V101
BDX65A
+5VCTRL
SUPPLY FOR PW1775/00
SUPPLY FOR PW1170/10 AND PW1774/00 ONLY
F115 1.6AD
F114 315mAD
PWRFL+
V5
CNY47A
F118
1.25AD
F117
800mAD
F116
100mAD
F108
200mAD
F109
200mAD
F110
100mAD
T101
S1
S3
14V
S4
13V
S6
24V
S4
28V
S5
46V
S7
200V
9V
27V
27V
+12V IN
0V(+12V)
0V(−12V)
C101
3300µF
40V
−12V IN
+24V IN
0V(+24V)
+CLIN
−CLIN
42V SH
0V SH
300V SH
V8
BY164
V1
BY164
C1
1000µ
V9
BY164
C2
330µ
V6
BY179
C3
10µ
C4
10µ
BY179
RECTIFIER CARD
TO ELECTRONICS RACK
T102
S2C
16V
S2A
7V
S2B
7V
S2D
16V
S6
40V
S3
10V
F102
1.6AD
20VM~1
F103
6.3AD
5VM~1
MOTOR~
F104
6.3AD
5VM~2
F105
1.6AD
20VM~2
F106
100mAD
40V~1
40V~2
F107
200mAD
9V~1
VALUES ARE TYPICAL VALUES
RD5500
850603

Figure 4.69 Power Supply Assembly, Schematic

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5.1 GENERAL

5.1.1 OVERVIEW

The PW1710 is the Control Unit of a diffractrometry installation. All the data and control signals for that installation are routed through the PW1710 micro-processor, which in turn receives commands from an operator´s terminal, or a computer, or the PW1710 front panel. Every instrumental command can be set by a keyboard command. Any sequence of commands can be stored in memory under a program number and executed with a single start command.

Part of the PW1710 memory can be reserved for the storage of measuring data. Calculator functions are available to enable simple calculations to be performed. They also allow the format of the output to be specified.

5.1.2 COMMAND FORMAT, ERROR CORRECTION AND RESET

When the main power is switched on, the PW1710 micro-processor starts automatically and executes the initialization routine described in Section 5.7.

The message "C=" on the terminal is a sign that commands can be entered.

The general format for a command is a three or four letter abbreviation, usually followed by a numerical argument, and terminated by a carriage return.

Two characters have been defined to allow correction of input errors:

<-- (left arrow) to delete the last character
↑ (up arrow) to delete the last line

Once the carriage return has been pressed, the command is executed and no more corrections can be given.

Execution of a command can always be terminated by typing / CR which is the general reset command.

// CR restarts the micro-processor. The initialization procedure as described in Section 5.7 is executed.

5.1.3 "START ACTION" and "SET PARAMETER"

Two types of command can be distinquished: one that starts an action immediately, and one that merely defines a parameter for a later action.
An example of the first type is:

SAN 20 (Set two-theta angle at 20°).

This command contains all the necessary information, and can be executed at once.

An example of the second type of command is:

SPE 0.2 (Set the scan speed at 0.2 degrees/second).

No action is taken. This is because it is only specifying a parameter for use in another command. For instance, before a goniometer scan can be started, you have to specify: the scan speed, ratemeter range, speed of the recorder and so on. Therefore the command "scan" has to be preceded by commands that set all the required parameters.

In the detailed command descriptions in Section 5.4, it can be seen which parameters have to be set before a certain action is started. Parameters keep their value until a new setting is given for them, therefore, it is not necessary to specify a parameter for each action. Parameters that rarely change, like the lower and upper levels of the pulse height discrim-inator, are best set by using a special program.

As well as commands being immediately effective, they can be stored in memory (assembled as a program) and be used later on for greater convenience in a routine environment.

5.1.4 SELECTION OF HARDWARE OPTIONS

Several hardware options of the PW1710 are available, but the software remains constant for all the options.

There are eight hardware option selection switches on the Secondary Control Panel (located behind the Front Panel). These switches must be set to reflect the hardware status of the system. Table 5.1 lists these switches.

Table 5.1 Hardware Switch Position.

HWS SW	SWITCH POSITION "0"	SWITCH POSITION "1"
0	Sample Changer PW1775	Sample Changer PW1170
1	2k byte RAM	4k byte RAM
2	Perform Memory Test (during initialization)	Skip Memory Test
3	NO second counting channel	Second counting channel PW1748 present
4	SPARE	
5	Printing recorder PM8210/31 present.	Recorder PM8203A present.
6	NO one-theta drive	One-theta drive PW1747 present.
7	NO two-theta drive	Two-theta drive present.

5.2 PW1710 DISPLAY

The PW1710 display can show two parameters simultaneously. The front panel pushbuttons are used to select the parameters. When in the remote mode the pushbuttons act as follows:

The L and R pushbuttons select which part of the display is used:

L the following buttons refer to the left half of the display (until R is pressed).

R The following buttons refer to the right half of the display (until L is pressed.

The other buttons select the parameter itself:

B	the contents of the beginning of the output buffer (see note 3)
C	command under execution
D	lattice spacing
F	fluorescence scaler contents or ratemeter (see note 1)
G	goniometer angle (two-theta value)
M	contents of the memory (address defined by DME) (see note 2)
O	switches this display off
P	current program number
S	sample changer magazine position
T	theta angle (if a second motor drive is connected)
W	wait condition (the peripheral that the PW1710 is waiting for)
X	scaler contents or ratemeter (see note 1)

NOTE 1: X and F have two modes. When the scaler is on during a measurement, the number of counts collected is shown. The number is preceded by XC or FC (counts). The rest of the time the display shows the countrate (counts per second). The number shown is preceded by XI or FI (intensity). The sampling time is 0.5 seconds.

NOTE 2: The memory address can by defined in two ways:

1 by using the DME command

2 by using the three pushbuttons as follows:

. (decimal point)	*rotate the digit pointer one to the right*
- (minus sign)	*decrement the indicated digit by one*
ENTER	*increment the indicated digit by one*

NOTE 3: The combination of DPL B and DPR O uses the whole display to show the first 20 characters in the output buffer.

The display can also be controlled by the terminal by means of the commands DPL and DPR. When the front panel is used to input the commands the display has some additional functions which are described in Section 5.3.

The three indication lamps next to the display have the following meaning:

BUSY	This lamp is lit during initialization and the execution of a command, and during program assembly. While it is lit the PW1710 will not accept new commands (accept for program assembly). The BUSY lamp flashes intermittently while the PW1710 is in the manual mode (see the command MAN in Section 5.3).
ASSEMBLY	This lamp is lit while programs are being assembled. While it is lit, the PW1710 does not execute commands that are input, but stores them in memory.
REMOTE	This lamp is lit when a terminal or a computer is the command input device.

5.3 COMMAND INPUT VIA THE FRONT PANEL

In a minimum configuration without a terminal, it is possible to use the front panel as the input device. Because of the absence of certain keyboard functions, the following changes take effect:

Terminal	Front Panel
CR	ENTER
/CR (stop)	STOP
//CR (reset)	Press the reset button on the Secondary Control Panel
delete character	CLEAR
delete line	Does not exist
space	. . (two decimal points)
DIV	DIU
DVC	DUC
SQR	SOR
WAV	WAU

The display has multiple functions as follows:

1. During the input phase of a command (between pressing the first key and ENTER) the front panel input is shown on the display. You can use the CLEAR button to erase the last character.

2. In the assembly mode, the display simultaneously shows both the current command in the assembled program and the remaining free space in memory.

3. In an error situation, the display shows the error message. The ENTER button has to pressed to clear the display and resume the program.

4. In all other cases the display shows the parameters that are selected by the DPL and DPR commands. The short display selection with single buttons is not possible in front panel mode.

If the front panel has been selected as the input device, all output to terminal 1 is suppressed. The command PRP is ignored, however, the output of PAR and PMM is shown on the diplay (per line, scrolling is possible with ENTER).

5.4 COMMANDS

5.4.1 GENERAL PROGRAMMABLE COMMANDS

Command	Action and comments.
(CLP) p	Call program p. (p = 0 to 255). With this command, the actual execution of a program can be started. This command can also be programmed. This makes it possible to call other programs within a program, up to a nesting level of 6. The characters CLP may be ommitted (except within a program); the PW1710 interpretes a single integer followed by a CR or ENTER as a CLP command. Program 0 is executed after initialization, and should be reserved for for that purpose.
CNE p	Call program p when the contents of the accumulator are negative, (<0), otherwise proceed with the next command.
CPO p	Call program p when the contents of the accumulator are zero or positive (>=0), otherwise proceed with the next command.
REP p n	Repeat program p n times. p and n between 0 and 255. n = 0 means infinite recycling.
DPL x	Show parameter x on the left hand half of the display. For the argument x, the same characters are valid as for the front panel. Refer to section 5.2.
DPR x	Show parameter x on the right hand half of the display. For the argument x, the same characters are valid as for the front panel. Refer to section 5.2.
WAV w	Set wavelength at value w. This is used in the display program to calculate the d-value, in CSP and SAD. (WAU w at the PW1710 front panel).
HLT	Halt. This command interrupts a running program until <cr> or ENTER is typed in. The halt state is not specifically indicated.

5.4.2 PROGRAMMABLE COMMANDS FOR DIFFRACTOMETER CONTROL

Command	Action and comments
LWL i	Set lower level at I %. The value i can be between 0 and 99.
UPL i	Set upper level at I %. The value i can be between 0 and 99, in fact between 1 and 99, as 0 = infinite (in practice about 150%).
RFS iEj	Ratemeter full scale is i x 10 exp j counts per second. i can be 1, 2 or 5. j can be 2, 3, 4 or 5.
RON	Ratemeter on. The ratemeter is normally connected to the recorder during execution of the, commands CSC, CSP, SSC and MSA. When this is not required you must give the command ROF.
ROF	Ratemeter off.
RTC x	Ratemeter time-constant. x can be: .1, .2, .5, 1, 2 or 5 seconds. or: F where the time-constant = 10 000/full scale (set by RFS). or: S where the time-constant = 0.01/scanspeed (set by SPE). When either F or S have been selected as the argument, the time-constant is rounded to the nearest value of .1, .2, .5, 1, 2 or 5.
RLF	Recorder paper line feed. (PM8203A only).
RSP s	Recorder speed is s mm per degree two-theta. s = 0 to 50 in steps of 1mm (0 = no feed). The pen is automatically lifted when the recorder stops. This command is only valid for the CSC, CSP, SSC and MSA commands. The DAC command defines another recorder speed. Note that the maximum recorder speeds are as follows: 10 mm/s for the PM8203A and 16.7 mm/s for the PM8210. When the combination of SPE and RSP results in a higher speed, the recorder maximum is taken and no error message is issued.
SON	Spinner on.
SOF	Spinner off.
SAN a	Set the two-theta angle at a degrees. a = 0 to 327.675^{o}(0.005^{o} will be the step size). When a is lower than the current angle, a loop of 0.5 degree is made so that the new angle is always approached from the low angle side.
IAN ±a	Increment the two-theta angle with a degrees. a can be from -163.830^{o} to $+163.830^{o}$ in steps of 0.005^{o}. When a is negative, an approach loop is made as in SAN.
SAD d	Set angle at 2 arcsin (WAV/2d).

SPE a	Scanspeed is a degrees two-theta per second. a = 0.001 to 0.127 in steps of 0.001, or 0.01 to 1.27 in steps of 0.01. When the argument is typed with three decimals, the first range is taken. When the argument has two or less decimals, the second range is taken. Used in the CSC, CSP and MSA commands. It is also used in the SSC command to determine the recorder speed.
INT t	Sampling interval time is t seconds. t = 0 to 3276.75 seconds in steps of 0.05. Used in commands CSC, CSP and SSC. (For INT=0 see CSC).
STP da	Stepsize in degrees two-theta. da = 0.005 to 163.830 in steps of 0.005. Used in the SSC command.
CSC da	Make a continuous scan from current angle a upwards to a+da. da = 0.005 to 163.830 in steps of 0.005. The ratemeter signal is connected to the recorder (see ROF), the scanspeed is defined by SPE. Every INT the current angle and the scaler contents are sent to serial output 1 and the scaler is cleared. The commands DON and DOF control the ouput to interface 2. No sampling takes place when INT=0. Other commands that can effect the working of CSC are: UPL, LWL, RFS, RTC, RSP, SON and SOF.
SSC da	Make a stepscan upwards from current angle a to angle a + da. da = 0.005 to 163.830 in steps of 0.005. Stepsize is defined by STP, measuring time per step by INT. At each step, the angle and counts are sent to serial output 1. The commands DON/DOF control the output to interface 2. When RON is selected, the ratemeter is connected to the recorder and the paper speed is defined by SPE and RSP. Other commands that can influence the working of SSC are: UPL, LWL, SON and SOF.
BGM x BGT t	Two commands to specify commands MSA and MST. BGM x is background mode. x can be: 0 = No backgrounds. 2 = Two backgrounds (either side of scan). L = One background at low side of scan. H = One background at high side of scan. BGT t is backround measuring time in seconds. t = 0.05 to 3276.75 seconds in steps of 0.05 seconds.

MSA da Measure area from current angle a upwards to angle a + da. da = 0.005 to 163.830 degrees two-theta in 0.005 degree steps. The procedure is as follows:

1. Measure background if BGM = L or 2 for BGT seconds, and save the results as counts/second in BLOW register.
2. Make a continous scan to angle a+da, scanspeed = SPE (INT has no influence), and save the result as counts/second in SUM register. When the parameters da and SPE are selected such that the total measuring time is greater than 3276.75 seconds, a time overflow error message will be printed, and further execution of the command is stopped.
3. Measure background if BGM = H or 2, for BGT seconds, and save the result as counts/second in BHIG register.
4. Calculate the net result of SUM-BLOW-BHIG and save this in the software accumulator for further processing. (Refer to Section 5.4.3).
   When BGM = 2, the result = SUM - (BLOW + BHIG)/2.

RON/ROF control the ratemeter output to the recorder.
Other commands that influence the working of MSA are:
UPL, LWL, SON and SOF.

MES t Measure at current angle for t seconds.
t = 0.05 to 3276.75 seconds in steps of 0.05 seconds.
The scaler contents divided by measuring time is saved in the software accumulator for further processing. (Refer to Section 5.4.3).
Other commands that influence the working of MES are:
UPL, LWL, SON and SOF.
The recorder is off.

MXN i
MXS da
MXT t

Three commands define parameters for the MAX-procedure.
i = the number of measuring points (2 to 100) on both sides of centre.
Therefore the total number of measuring points = 2i + 1.
da = the interval between two points in degrees. It can be between 0.005 and 1 degree two-theta in 0.005 degree steps.
t = the measuring time per point, it can be between 0.05 and 3276.75 seconds in steps of 0.05 seconds.

MAX Search for maximum intensity around the current angle. The procedure followed is:

1. The goniometer is set at (current angle - MXN x MXS) with an angle approach loop.

2. A stepscan is made from this point upwards, the step size = MXS, the measuring time per step = MXT, and the total number of steps = 2 x MXN + 1.
   At each step the scaler reading for the last three steps are summed. That total divided by 3 x MXT, is sent to Serial Output 1 together with the two-theta angle for the center of the three steps. The goniometer is set to the maximum angle with an angle approach loop. When the maximum is found at one of the edges of the scan, an asterisk (*) is added to the output.

MST	Measure top. The procedure MAX is executed around the current angle with the parameters MXN, MXS and MXT. The output of angle, counts and * is suppressed. Backgrounds (in c/s) are measured according to the parameters BGM and BGT, at angle positions -BGA and +BGA degrees from the top. The net result TOP-BLOW-BHIGH is calculated and saved in the accumulator. When BGM = 2, the result = TOP - (BLOW + BHIGH) / 2. The recorder is OFF. Other commands that influence MST are: UPL, LWL, SON and SOF.
CAN a	Calibrate angle. a = 0° to 327.675° (0.005° will be the smallest actual angle). The value a is assigned to the current position of the stepping motor. The difference between the zero point and the hardware calibration point is saved as the correction angle. this value must be between -2.56 and +2.56 degrees, otherwise an "out of range" error will be given.
CSP da	Start a continous scan with peak-labelling from the current angle (a) upwards to the angle (a + da). da = 0.005° to 163.830° in steps of 0.005°. The scan speed is defined by SPE. Every INT sec the scaler is read and a numerical process is applied to the last 9 readings: the data obtained is smoothed and the second derivative is calculated in order to find peaks on a slowly varying background. Angle, d-value and peak intensity in c/s are sent to the terminal and the second output device. The d-value is also sent to the PM8210 (this can be inhibited by POF). The ratemeter signal is sent to the recorder (this can be inhibited by ROF). Other commands that affect CSP are WAV, UPL, LWL, RFS, RTC, RSP, SON, SOF, DON and DOF. NO action is taken if INT = 0. When the following combination is selected: FRONT PANEL MODE POF DOF (DPL B or DPR B) then the CSP command starts a scan until a peak is found. The recorder stops and the display will show what normally will be sent to the terminal. The scan will continue after the ENTER key has been pressed.

5.4.3 PROGRAMMABLE COMMANDS FOR CALCULATIONS AND OUTPUT

For simple quantitative applications, the net intensity of a peak or an intigrated scan is not enough. Some data handling is necessary, but a large variety of formulae can be required. The most versatile solution to the problem is to provide the user with a set of commands to handle data and to specify the output, so that he can program his own application.

Measuring results from the commands MSA (integrated scan with background correction), MST (peak with background correction), and MES (peak measurement), are stored as counts per second in a software accumulator. From there, they can be either printed, or saved in memory for further processing. In order to do this, registers have to be defined for that purpose.

Command	Action and comments
NRG n	Assign a number of registers. n = 0 to 255. Each register takes 4 bytes of memory at the cost of programming space. Assigned registers are automatically set to zero. *NOTE: This is the only command that is already executed during the assembly stage, so that the display always shows the net free space available for programming.*
STR n	Store register. The contents of the accumulator are transferred to register n. The contents of the accumulator remain unchanged.
RCL n	Recall register. The contents of register n are transferred to the accumulator. The contents of the register remain unchanged.
RCT	Recall counts. The number of counts is transferred to the accumulator. This is the total number of counts collected during the last measurement (MES, MSA, MST, MAX).
RIN	Recall intensity. The intensity (c/s) is transferred to the accumulator. This is the counts per second from the last measurement. This action is included in the execution of MES, MSA, MST and MAX. The command RIN can be used after RCT, and vice-versa. *NOTE: After MSA and MST with background measurement, RCT and RIN recall the last background result rather than the result of the total measurement.*
GAN	Get angle. The actual two-theta angle is transferred to the accumulator.
GAD	Get d-value. The actual d-value is transferred to the accumulator.
CLR n	Clear register n. Register n is filled with all zero.

ADD n	Add register. The contents of register n are added to the contents of the accumulator. The contents of register n remain unchanged.
SUB n	Subtract register. The contents of register n are subtracted from the accumulator. The contents of register n remain unchanged.
MUL n	Multiply register. The contents of the accumulator are multiplied with the contents of register n. The contents of register n remain unchanged.
DIV n	Divide register. The contents of the accumulator are divided by the the contents of register n. The contents of register n remain unchanged.
SQR	Square root. The value in the accumulator is replaced by its square root.
ADC con	Add constant. The defined constant is added to the accumulator.
SUC con	Subtract constant. The defined constant is subtracted from the accumulator.
MUC con	Multiply constant. The contents of the accumulator are multiplied by the defined constant.
DVC con	Divide constant. The contents of the accumulator are divided by the defined constant.
LDC con	Load constant. The defined constant is put into the accumulator.
	The constant is a number which may contain a minus sign, a decimal point, and up to a maximum of 9 digits. Scientific notation is not accepted. So the actual modulo range is from 10 exp -8 to 10 exp +9. Calculation accuracy is 7 decimal places.
DON DOF	Dual output ON. Dual output OFF. The output of certain commands can also be sent to output interface 2. The commands DON and DOF enable and disenable this function. It affects the commands CSC, CSP, HED, PAR, PMM, PRP, PTA, PTR and SSC.
PON POF	Printing recorder ON. Printing recorder OFF. These commands have the same effect as DON/DOF (except CSC), but they are now for the printing recorder PM8210/31.

HED Print heading on terminal (and on output 2 or PM8210 if asked for). The heading is one line of print containing sample identification (as given by IDT), date, time, sample position in magazine (when a changer is connected), and the current program number.

DEC i Required number of decimals in the output specified by BFR and PTR. i can be from 0 to 7.

BFR n Store contents of register n with DEC decimals in the output buffer, but do not print.

PTR n Store contents of register n with DEC decimals in the output buffer, and print the whole buffer on the terminal. (Also on output 2 and/or PM8210 if requested).

NOTE 1: The accumulator is register 0.

NOTE 2: Fieldwidth for BFR and PTR is 10 places. Asterisks are printed when the total number of digits , minus sign and decimal point exceeds 10, or when the value to be printed is greater than 2 exp 31 - 1 (= 2147483647).

BFA xxx Store the following string xxx of maximum 16 alphanumeric characters in the output buffer, but do not print them.

PTA xxx Store the following string xxx of maximum 16 alphanumeric characters in the output buffer and print the whole buffer on the terminal. (Also on output 2 and/or the PM8210 if requested).

WTD Wait for display.
This command can be used in programs after a BFR or BFA command, to temporarily display the contents of the output buffer (delay is 2 s).

5.4.4 PROGRAMMABLE COMMANDS FOR SAMPLE CHANGER CONTROL

SCH i j The sample changer can be programmed with the commands SCH i j (sample NXSchanger start) and NXS (next sample). These commands have the same function as a DO-loop in a Fortran program. All commands between SCH i j and NXS are executed first for the sample in magazine position i and next for the sample in position i+1 and so on, up to and including position j.
The necessary sample loading and unloading and the magazine transport is performed automatically.
When i is 0, that means: begin at the first non-empty position.
When j is =, that means: stop at the first empty position.

NOTE: The commands SCH and NXS can only be used in programs, and must appear in the same program. When NXS is not preceeded by SCH, an error is produced during program execution.

The following five commands cause an error when used within a SCH-NXS loop, but can be used for special applications, for instance for a monitor measurement.

LSM	Load sample from magazine.
USM	Unload sample to the magazine.
LSS	Load from the single sample position.
USS	Unload the sample to the single sample position.
MAG i	Set the magazine at position i.

NOTE 1: The PW1710 automatically sets the goniometer at the required angle for loading and unloading.

NOTE 2: When the recorder is a PM8203A, and the parameter RON is selected, the sample number is sent as an analog signal to the recorder during the sample load phase in the commands SCH and LSM. (In LSS, the analog signal sent to the recorder is equal to 42.5 scale divisions on the recorder).

NOTE 3: Exceptions when the sample changer is a PW1170:

- *i = 0 and/or j = 0 in SCH are not allowed.*
- *Commands LSS and USS cause an error.*
- *MAG 0 means: Go to magazine exchange position. The command MAG 0 can be used to initialize the sample counter.*

5.4.5 PROGRAMMABLE COMMANDS FOR SECOND MOTOR DRIVE

In all the diffractrometer control commands described in Section 5.4.2, it was assumed that the two-theta and theta shafts are coupled by gear wheels. The angle parameters referred to the two-theta angle. When a seperate theta motor drive option is fitted, extra commands to control the two shafts are available.

STT a	Set two-theta at a degrees. a = 0 to 327.675 degrees. (0.005° will be the step size). When a is smaller than the current angle, a loop of 0.5 degrees is made so that the angle is always approached from the low angle side.
ITT da	Increment two-theta angle by da degrees. da can be from -163.830 to +163.830 degrees in steps of 0.005°. When da is negative an approach loop is made.
STH a	Set theta at a degrees. a = 0 to 327.675 degrees. (0.005° will be the step size).When a is smaller than the current angle, an approach loop is made.
ITH da	Increment theta angle by da degrees. da can be from -163.830 to +163.830 degrees in steps of 0.005°. When da is negative an approach loop is made.
SAN a IAN da	The commands SAN and IAN have the same meaning as in Section 5.4.2. The shafts are coupled in the software. a and da refer to the two-theta angle and theta is set at two-theta divided by 2.

MOD i Define scan mode.
i = 1 means: Scan with theta, two-theta fixed.
i = 2 means: Scan with two-theta, theta fixed.
i = 3 means: Scan with both shafts (the shafts are coupled in the software).

This parameter affects the following commands:

CSC da	Continuous scan.
CSP da	CSC with peak labelling.
SSC da	Stepscan.
MSA da	Measure area.
MST	Measure top.
MAX	Search for maximum around current angle.
MAN	Manual mode.

When MOD = 1, all angular input parameters (da, SPE, STP, MXS and BGA) and printed angles (CSC, SSC and MAX) refer to the theta shaft.
When MOD = 2 or 3, all angular values are in degrees two-theta.

CTT a Calibrate two-theta at a degrees.
For further details see CAN.

CTH a Calibrate theta at a degrees.
For further details see CAN.

5.4.6 PROGRAMMABLE COMMANDS FOR SECOND COUNTING CHANNEL

When a second counting channel is connected, the following commands are available. The suffix "F" means fluorescence or fixed channel.

LWLF i Set lower level at i%.
The value i can be between 0 and 99%, in 1% steps.

UPLF i Set upper level at i%.
The value i can be between 0 and 99%, in fact between 1 and 99% as 0 is equal to infinite (in practice about 150%).

RFSF iEj Full scale ratemeter is i x 10 exp j c/s.
i can be 1, 2 or 5.
j can be 2, 3, 4 or 5.

RINF Recall intensity. The channel 2 intensity (in counts per second) is placed in the accumulator.

RCTF Recall counts. The counts registered in channel 2 are placed into the accumulator.

During execution of the commands CSC, MAX, MES, MST, and SSC; the counts measured in the second channel are collected in a seperate scaler. The scaler is cleared at the start of the command. After execution, the result in counts or counts per second is available until another of the above commands is given.

PHDF Pulse height distribution curve, not programmable. Refer to 5.4.7.

5.4.7 NON-PROGRAMMABLE COMMANDS

ASS n	Assemble program, n = 0 to 255. In fact the first available program number is 1, as 0 is reserved, refer to Section 5.5.
DEL	Delete this command.
INS	Insert the following commands until a / is given. DEL and INS can only be given when you are in the assembly mode.
DLP n	Delete program n.
PMM	Print memory map on terminal (also on output 2 and/or PM8210 if requested).
PRP (n)	Print program n (or all programs if n is omitted) on the terminal. (Also on output 2 and/or the PM8210 if requested).
NLC l c	Number of lines and columns per page, for PRP. l = 1 to 255; i = 1 to 4.
WME	Write memory contents to cassette.
RME	Read memory from cassette.
PHD	Make a pulse height distribution curve on the recorder; with the parameters: window 2%, lower level in steps of 2% from 0 to 98%, measuring time per step 2 sec., and a recorder speed of 2mm/sec.
PHDF	PHD for the second counting channel.
DAT d m y TIM h m	Set date and time. They are printed when the command HED is executed. Example: DAT 25 12 82; TIM 14 45.
IDT xxx	Sample identification is: (maximum 12 characters). It is also printed with the command HED. When a sample changer is in use, the position of the magazine is added to the identification.
SIP n	Single step execution of program n. Used for test purposes. Each command appears on the screen and is executed when the carriage return key is pressed.
DAC f l	Digital to analog conversion. Numbers from the terminal are converted into an analog signal for the recorder. f is full scale value, and l is paper transport per step which can be 0 to 5mm. (In practice the smallest amount is 0.05mm per step). After each step, the PW1710 answers with D= so that a new series of numbers can be given. This action is terminated by a /. More than one character may be given on one line (maximum 140 characters). Outrange numbers are limited to 100%.
PAR	Print parameters. A print out of all the parameters and their last setting is given on the terminal. (Also on output 2 and/or the PM8210 if requested).

DME A	Memory address A (four hexadecimal characters). Thus command specifies the memory address of which the contents are shown in hexadecimal code on the display when M is selected. Refer to Section 5.2.
WBS A B	Write byte B to bus address A. Used for test purposes only. Both A and B are written in two hexadecimal characters.
TST	Jump to the TEST MONITOR (Refer to Section 5.8). This command is only valid if the HWS 2 is set to 1 (skip memory test). Used for test purposes only, and is only possible from a terminal.
MAN	Manual control of the stepping motor and recorder. Terminal input is switched off; only limited front panel input is possible. The BUSY lamp blinks. The following input can be given:

da ENTER	Change motor settings da degrees. da = -163.830^{o} to $+163.830^{o}$ in steps of 0.005^{o}.
ENTER	Change the motor settings with the last given increment.
F iEj ENTER	Equal to the command RFS iEj.
T x ENTER	Equal to the command RTC x.
M i ENTER	Equal to the command MOD. i = 1 means: step with theta. i = 2 means: step with two-theta. i = 3 means: step with both in 1:2 ratio.
L x ENTER	Equal to the command DPL.
R x ENTER	Equal to the command DPR.
P s ENTER	Paper speed for the strip chart recorder is s mm/sec. s can be 0 (in practise 0.005) till maximum recorder speed. P without an argument stops the paper drive, the pen goes up, but the recorder signal remains active. This command is necessary for the recorder PM8210/31 which has no front panel speed selector.
STOP	End of manual mode. Return to command mode: "C=".

5.5 PROGRAM ASSEMBLY

5.5.1 GENERAL

With the command ASS n (n can be between 0 and 255), a program numbered n can be assembled. From when ASS is entered until a / is given, the PW1710 is in assembly mode; the ASSEMBLY lamp is lit, and input commands are not executed, but stored in sequence in memory. The program thus assembled can later be executed by giving the command CLP n (call program n).

Whilst a program is being assembled, the four right-most digits of the PW1710 display will show the number of free bytes remaining in memory (for example, A1234).

There are two possibilities for the ASS command:

1. n is unknown (not previously entered). When n is unknown, a new program will be assembled.
2. n is known. This is when the command ASS is used to alter an existing program.

5.5.2 ASSEMBLY OF A NEW PROGRAM

To assemble a new program you must give the command ASS with a program number to put the PW1710 into assembly mode. When a new command can be entered, the PW1710 answers each input line with A=, or with an error message followed by A= when the previous input is not accepted. All the commands typed in are stored in consecutive memory bytes. The assembly is ended by typing a /.

Programs are stored sequentially in memory according to their number.

5.5.3 CHANGING AN EXISTING PROGRAM

To change an existing program you must give the command ASS with the number of the program that you wish to change. When the PW1710 says that it is ready for input by giving A=, there are four options available:

1.	CR	No change, step to the next command.
2.	(command) CR	The new command that you have just given will replace the old command. Then the next command is shown.
5.	DEL CR	Delete this command and then show the next command.
4.	INS CR	Insert commands before the one that is shown. From this point on the PW1710 asks I= and one or more commands can be inserted. This mode has to be terminated with a / CR. A second / CR terminates the assembly mode.

5.5.4 DISPLAY OR PRINT PROGRAMS

Two commands are available to enable the programs stored in the memory to be printed on the terminal. The commands are:

PMM	Print memory map. All progam numbers are printed (displayed), together with the number of registers reserved for data storage, and the available free space. When the command was entered via the front panel and the information is displayed on the front panel, scrolling (reading through) is by means of the ENTER button.
PRP n	Print program n. (Print all the commands that make-up this program). When n is omitted, all programs are printed. (Use the command ASS n to view a program on the PW1710 front panel).

When the list of programs is to be displayed on a VDU, there is a parameter for the PRP command:

NLC l c	Number of lines and columns per page. l can be between 1 and 255, and c can be between 1 and 4. After each page the message "NEXT PAGE" is printed, this must be answered with CR. The commands DON and DOF control the output to the second terminal.

5.5.5 BACK-UP TO CASSETTE RECORDER PM4202

Two commands are present to enable the memory contents to be written to and read from a cassette recorder:

WME	Write memory to cassette. All the programs in memory are written onto a cassette tape followed by an "end of data" gap. The recorder must be in STANDBY and the cassette in "begin of tape" or in a "end of data" gap. Several data banks can be written after each other, each seperated by an "end of data" gap.
RME	Read memory from cassette. The recorder must be in STANDBY and the cassette in "begin of tape" or in a "end of data" gap. The first data bank is read and stored in memory. The registers and their contents are not affected. Following (successive) data banks can be read by successive RME commands.

5.6 ERROR MESSAGES

There are 24 error messages that can be produced by the PW1710, they are as follows:

nn Text	Meaning
01 ILLEGAL ARGUM.	The argument specified in the last command is either: missing, or has the wrong format, or is outside the specified range.
02 UNKNOWN COMMAND	The command (mnemonic) that you have just given cannot be found in the command list.
03 MEMORY OVERFLOW	The available memory area is filled, too many programs, and/or too many registers have been specified.
04 ILLEGAL COMMAND	The last command given is known, but not allowed in this situation.
05 LIST OVERFLOW	The program you are writing is too long (maximum length = 255 bytes), split it into parts and link them.
06 STACK OVERFLOW	Too many program calls have been nested (maximum = 6).
07 NOT IN MEMORY	One of the programs involved is not in memory.
08 UNKNOWN CODE	During PLP or CLP, a command code is found that cannot be translated into a command. Error in memory chip.
09 TRANSM.ERROR	A parity, framing or overrun error has occurred in a transmission with a terminal or a computer.
10 BATTERY ERROR	Back-up battery empty, all the programs are lost and all the parameters are cleared. Refer to paragraph 5.7.6.
11 OUT OF RANGE	In a the command just given to set an angle, the angle requested is either negative or out of range.
12 ILLEGAL REGIST.	The register addressed has not been declared.
13 GONIOMETER LIMIT	One of the goniometer limit switches has been activated.
14 NO 2ND OUTPUT	Output to a second output device is not possible; switch the device on or give a DOF command.
15 RECORDER ERROR	The strip chart recorder is in local mode or has no paper or is not connected.
16 TIME OVERFLOW	The total measuring time is more than 3 276.75 seconds.
17 CHANGER ERROR	A Sample Changer error: it can be, a mechanical defect, or the command has not been allowed because of the sample changer status.

18 NO CHANGER	The sample changer is not connected.
19 SAMPLE IN GON.	Sample already in goniometer (load command not allowed).
20 SAMPLE IN MAG.	Sample in magazine (unload command not allowed).
21 NO SAMPLE	Load command given, but there is no sample available.
22 NO I/O DEVICE	There is no cassette recorder (RME and WME).
23 CASSETTE ERROR	The recorder was not in STANDBY, or the cassette was not in a "end of data" gap, or no cassette was mounted, or a cassette with a write disable plug was mounted.
24 NO DATA ON TAPE	The RME command was given, but there were no PW1710 programs on the cassette.

5.7 INITIALIZATION ROUTINE

After a POWER UP or a hardware RESET the following initialization routine takes place:

5.7.1 STEP 1A

- If SID switch = 0: Proceed with 5.7.2
- If SID switch = 1: LED SOD on, and
  - If all switches on Memory Extension Card = 0: Jump to the TEST MONITOR.
  - If any switch on Memory Extension Card = 1: Jump to address 5FFDH in the optional ROM 6.

5.7.2 STEP 1B

- LED SOD off, LEDs BUSY, ASSEMBLY, and REMOTE on.
- Save DPL x and select DPL W.
- If HWS switch 2 = 1: Skip memory check (proceed with 5.7.4).

5.7.3 MEMORY CHECK

RAM size is selected by means of HWS switch 1.
- If HWS 1 = 0: RAM size is 2Kbytes
- If HWS 1 = 1: RAM size is 4Kbytes

The result of the memory check is briefly visible on the display just after switching on or RESET. The format is: cc,cc,cc,cc,cc,-,a,b,c,d,e
The checks are as follows:

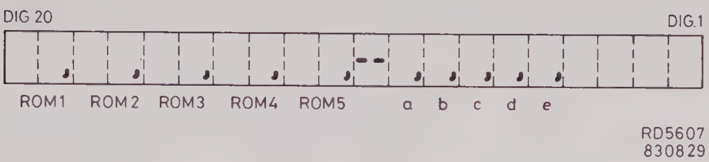

Figure 5.1. Memory Check on Display

ROMs: Calculate the checksum per ROM and compare it to the appropriate checksum in the first ROM. Start with ROM number 1.

If proper checksum: (per ROM) cc = space space
If improper checksum: (per ROM) cc = calculated checksum

RAMs: Save per byte the contents. Write 55H to the location, read it back and compare. Write AAH, read that back and compare, then restore the original contents.

If proper test result: a,b,c,d and e = space
If improper test result: a,b,c,d and e = x

Where:
a = first 1K low nibble RAM (D13)
b = first 1K high nibble RAM (D9)
c = second 1K low nibble RAM (D12)
d = second 1K high nibble RAM (D8)
e = second 2K RAM (D11) on Memory Extension Card (only if 4K RAM is present).

In the second production series of the PW1710, the four RAM ICs listed above were replaced by a 2K (D9). Therefore in this case, the characters a, b, c and d all point to D9.

If any error in ROM or RAM has been detected, the micro-processor will enter the HALT state. The only escape from this state is to rectify the fault.

5.7.4 STEP 2

- Timer interrupt: 20 Hz.
- Serial interface 1: Baud rate, mode, handshake on, receiver on (re-initiation without hardware reset possible).
- Serial interface 2: Baud rate, mode, handshake on, receiver on, (re-initiation without hardware reset possible).
- Printing Recorder interface: Mode, handshake on, receiver on.

Proceed with Section 5.7.5.

If the entry was via // (double slash):

- Restart Goniometer control 1 microprogram
- Restart Goniometer control 2 microprogram

5.7.5 STEP 3

- LEDs on Front Panel: BUSY on, ASSEMBLY off, REMOTE off.
- 3 MHz. for goniometer control on, select detector 1, spinner off.
- Enable interrupts.

5.7.6 COMMUNICATION PARAMETERS

- Display and print VSx.x TERMINAL=
- Wait for input; read, and if no hex. code, restart 5.7.6.
- Store communication parameters if any are present.

When an external computer is connected to interface 1 instead of a terminal, the message VSx.x TERMINAL= is sent to the computer. The question can now be answered by a string of up to 18 hexadecimal characters and a CR. This enables the computer to define special communication features. When the answer contains less than 18 characters, the default values are filled in.

Character	Meaning	Default value
1 - 4	Start of record	FF0A linefeed (Notes 1 & 2)
5 - 8	End of record	0DFF carriage return (Notes 1 & 2)
9 - 10	MCOFF	FF no MCOFF defined (Notes 1 & 3)
11 - 12	MCON	FF no MCON defined (Note 1)
13 - 14	Echo flag	FF look at echo jumper (Notes 1 & 4)
15 - 16	Delay	FF no delay between records (Ns 1+5)
17 - 18	Question mark	FF (Notes 1 & 6)

NOTE 1: FF means not applicable, or no ASCII character defined.

NOTE 2: For the start and end of record, 0, 1 or 2 ASCII characters may be defined.

NOTE 3: With the MCOFF character, the computer can withhold further micro-processor output, and it can release the output with the MCON character. MCOFF can be sent at any time, even in the middle of a record.

NOTE 4: Echo flag: 00 = do not echo input,
01 = echo input,
FF = look at the jumper on the interface board.

NOTE 5: Delay: The minimum delay time between two records can be given in units of 50ms. The number of units is hexadecimal, the maximum is 7FH = 127 x 50ms. = 6.35s.

NOTE 6: Question mark: Any value not equal to FF indicates that questions from the micro-processor must be terminated by "? end-of-record". An exception is the first message "VSx.x TERMINAL=", which ends with CR LF.

- If control is via terminal: LEDs BUSY and ASSEMBLY off, REMOTE on.
- If control is via the front panel: LEDs BUSY, ASSEMBLY and REMOTE off.

5.7.7 PARAMETER BANK

- Check the RAM reference location.
- Check if the position of the HWS switch has been altered during POWER DOWN or RESET.
- If either of the above mentioned occured:
  - Clear the RAM (user´s parameters set to zero)
  - Display and print ** BATTERY ERROR
  - Assign the following values to the user´s parameter bank:
    SPE = 0.001 LWL = 20 LWLF = 20 RFS = 5E5
    RFSF = 5E5 MOD = 3 NLC = 20 3
  - Select DPR G and DPL G

5.7.8 STEP 4

- Set the following parameters according to the user´s parameter bank:
  RFS, RFSF, LWL, LWLF, UPL, UPLF and RTC.
- Recorder control: select ratemeter 1, pen up, servo killed.
- If a Sample changer is connected:

  Type PW1775 (HWS 0 = 0):
  - If the magazine is in an in-between position, it is directed to the adjacent lower discrete position, according to type of magazine.
  - If the grab is holding a sample, the sample will be set down into the magazine if possible, or else it will be set into the single sample position. Finally the grab will point to the magazine.

  Type PW1170 (HWS 0 = 1):
  - If the magazine is in any of the discrete positions, no further initialization action occurs.
  - If the magazine is in the zero position, one step UP is made, and the sample number is set to 1.
  - If the magazine is in an in-between position, it is directed to the adjacent higher position. The sample counter needs to be corrected.

- Goniometer control 1:
  If closed loop: - Slew to zero position.
  - Correct for zero offset.
  - Set two-theta at 5 degrees.

  If open loop: - Display and print "THETA="
  - Transfer answer from console to display and angle register.
  - Select half speed mode.

5.7.9 STEP 5

If no communication parameters have been set up and program 0 is in memory: execute that program (it can be used for initialization purposes).

Restore original DPL.

5.7.10 STEP 6

Digital ratemeter on, LED BUSY off, Print C=.

5.8 TEST FACILITIES

The test facilities comprise, a TEST MONITOR, software commands (WBS and DME)which can be used for test purposes, and the error messages given in Section 5.6.

5.8.1 TEST MONITOR

A series of test commands are available for the PW1710 micro-processor, these commands are contained within a TEST MONITOR. The TEST MONITOR can only be used if terminal 1 is connected.

The TEST MONITOR provides the following possibilities:

- The reading of data from an indicated address
- The writing of data to an indicated address
- The starting of a program at an indicated address

The monitor should be accessed by using the TST command (the hardware selection switch SW2 on the Secondary Control Panel must be set to 1). Once you have given the TST command you remain in the TEST MONITOR until Q is given. This means that you do not have to give TST for every command.

NOTE: The TEST MONITOR can also be accesssed after a power up, or a hardware Reset (RESET button), if the SID switch on the System Control card is set to 1, and, all the switches on the Memory Extension Card are set to 0. This method does not initialize the complete system, and should not be used in the field.

Before using the TEST MONITOR, read the following notes:

1. Before writing to RAM, find an empty RAM area for this purpose. Look in the area 9600 to 9700. To look in this area, use the command:
   ```
   R 9600 0100
   ```
   A block of zeroes indicates an available area.
   If an error occured because you have a 2K system, refer to XRA 207 to update your system to 4K.

2. Instead of C=, the TEST MONITOR gives the prompt: TEST:

3. All interrupts are disabled and only USART 1 is initialized (for I/O). Therefore only terminal 1 is available for input and output.

4. Spaces have been allowed: before, between and after the arguments of a command to increase readability.

5. In the commands described in this section, aaaa, llll and dd are hexadecimal numbers.

6. If you try and give an improper input, the following error message is issued: "** <bell> ERROR INPUT".

5.8.2 TEST MONITOR INSTRUCTIONS

The actual TEST MONITOR instructions are as follows:

R aaaa <CR>	Read data from address aaaa.
C R aaaa <CR>	Continuously read data from address aaaa. Exit from this commazd by typing in any character.
C C R aaaa <CR>	Read data from address aaaa each time a <CR> is typed in. Exit from this command by typing in any character other than a <CR>.
R aaaa 1111 <CR>	Read a block of data from address aaaa to address aaaa + 1111 - 1.
C R aaaa 1111 <CR>	Continuously read a block of data from address aaaa to address aaaa + 1111 - 1. Stop this command by typing in any character.
C C R aaaa 1111 <CR>	Read a block of data from address aaaa to address aaaa + 1111 - 1 each time a <CR> is typed in. Exit from this command by typing in any character other than a <CR>.
W aaaa dd	Write data dd to address aaaa. *NOTE: Each byte is stored immediately after completion. The action is terminated by typing ^CR".*
W aaaa dd .. dd	Write a block of data to address aaaa, aaaa + 1, aaaa + 2 and so on. *NOTE: Each byte is stored immediately after completion. The action is terminated by typing ^CR".*
C W aaaa dd	Continuously write data dd to address aaaa. Exit from this command by typing any character.
C C W aaaa dd .. dd	Each byte dd is written to address aaaa immediately after it has been typed. The action is terminated by typing <CR>.
E aaaa <CR>	Execute the machine code (subroutine) starting at address aaaa.
C E aaaa <CR>	Continuously execute the subroutine located at address aaaa. Exit from this command by typing any character.
C C E aaaa <CR>	Execute the subroutine which starts at address aaaa every time that <CR> is typed. Typing anything other than <CR> terminates the action.
Q	Quit. If the TEST MONITOR was accessed via the TST command, a jump is made to the address 0000H (return to normal software and VSx.x TERMINAL= should appear on the terminal or VDU.

5.8.3 TEST MONITOR INSTRUCTION EXAMPLES

This page provides an example of each of the test commands:

R 8800 <CR>	This causes the contents of RAM address 8800 to be sent to the terminal where it is printed or displayed.
C R 8800 <CR>	This causes the contents of RAM address 8800 to be continuously sent to the terminal, where they are continuously printed or displayed.
C C R 8800 <CR>	This causes the contents of RAM address 8800 to be continuously sent to the terminal, where it is printed or displayed each time that a <CR> is given.
R 8800 0010 <CR>	This causes the contents of RAM from address 8800 to address 880F to be sent to the terminal where they are printed or displayed.
C R 8800 0010 <CR>	This causes the contents of RAM from address 8800 to address 880F to be sent to the terminal where they are printed or Zisplayed continuously block after block.
C C R 8800 0010 <CR>	This causes the contents of RAM from address 8800 to address 880F to be sent to the terminal, where they are printed or displayed a block at a time, each time a <CR> is given.
W D810 41	(41 is the ASCII code for capital A) This causes a capital A to be sent to terminal 1 where it is printed or displayed. This is executed immediatly the 1 of 41 is typed.
C W D810 41	(41 is the ASCII code for capital A) This causes a capital A is continuously sent to terminal 1 where it is printed or displayed.This is executed immediatly the 1 of 41 is typed.
C C W D8C0 F7 39 79	This causes a capital A to be written to the right-most digit of the PW1710 display after the 7 of F7 is typed in. Typing 39 changes the A to a C, and typing 79 changes the C into E. Typing <CR> terminates this action.
W D8C0 3F 00 3F 00 00 24 3F 00 06 00 01 27 06 00 36 30 F3 00	This causes PW1710/00 to be displayed on the PW1710 display.
E 8C00	This causes the program stored in RAM starting at address 8C00 to be executed.
C E 8C00	This causes the program stored in RAM starting at address 8C00 to be continuously executed.
C C E 8C00	This causes the program stored in RAM starting at address 8C00 to be executed every time that a <CR> is given.
Q	This causes the PW1710 to leave the TEST MONITOR and return to the normal routine.

5.8.4 CARD ADDRESSES

If a card in the PW1710 can be addressed, it has its own specific address, these addresses are essential for addressing cards individually to test a function on that card. The cards that can be addressed and their addresses are as follows:

Dual Serial Interface	D81
Display Keyboard Control	D8C0 to D8FF
Secondary Control Panel	D8F
Goniometer Control	D87
Second Goniometer Control	D83
Window Control	D84
Second Window Control	D89
4 Digit Counter	D86
Second 4 Digit Counter	D8B
Ratemeter	D85
Recorder Control	D82
PW1170 Interface	D88
Changer/Spinner/Shutter Control	D88

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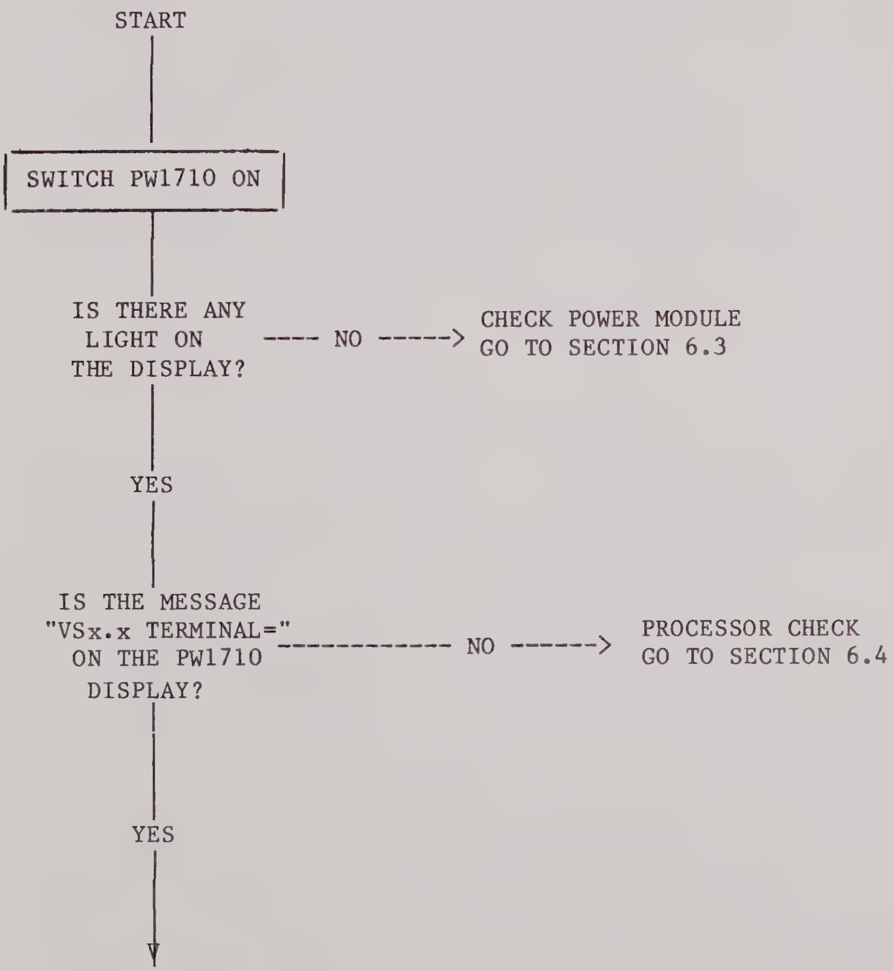
6.1 TROUBLE-SHOOTING GUIDE

If the system is not functioning properly, carefully follow the diagnostic procedure below.

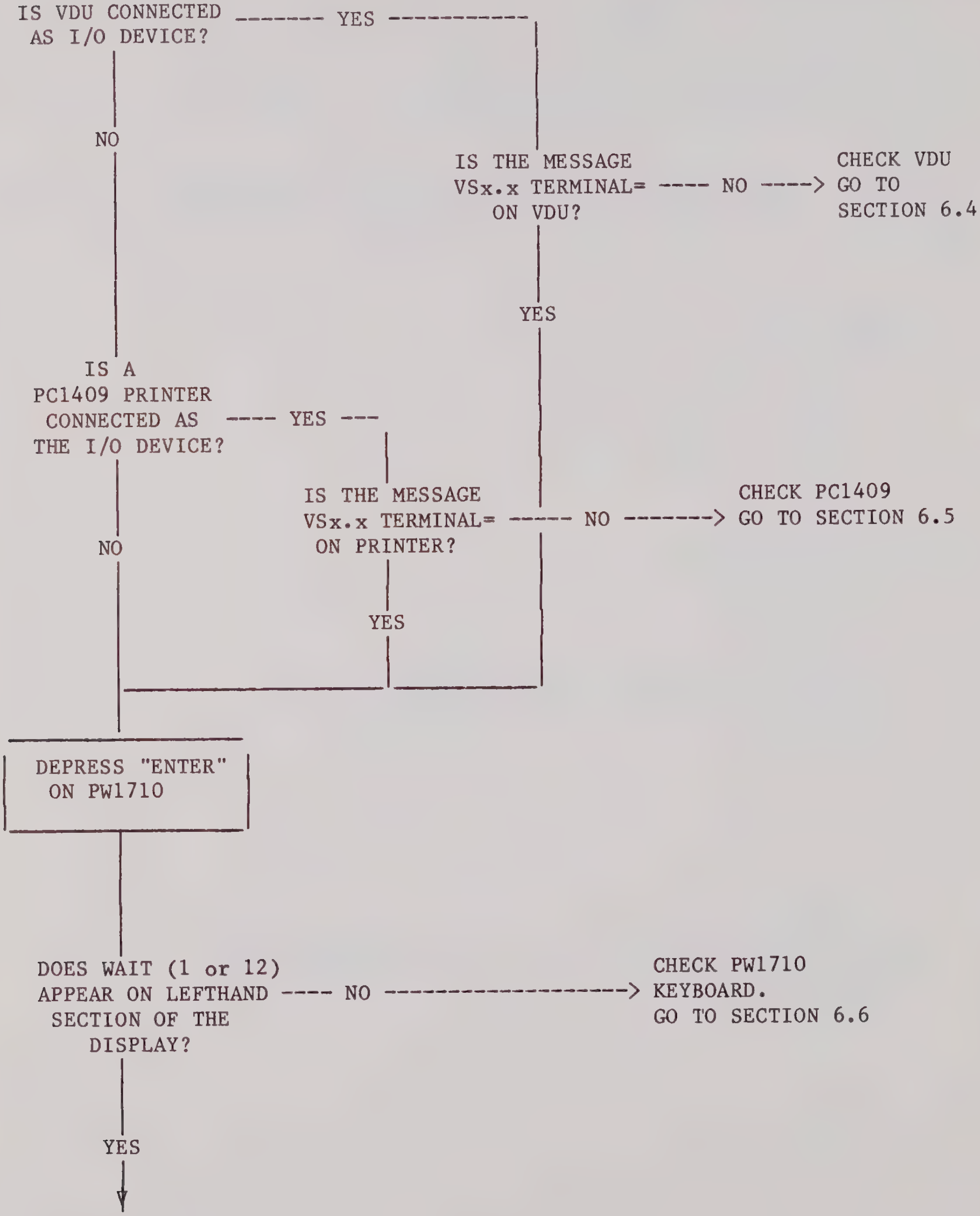
You will be directed to an operating mistake, a wrong connection or a hardware defect.

In order to rectify hardware problems, a PW1718 spare parts kit should be available, as the procedure can only determine a defective printed circuit board.

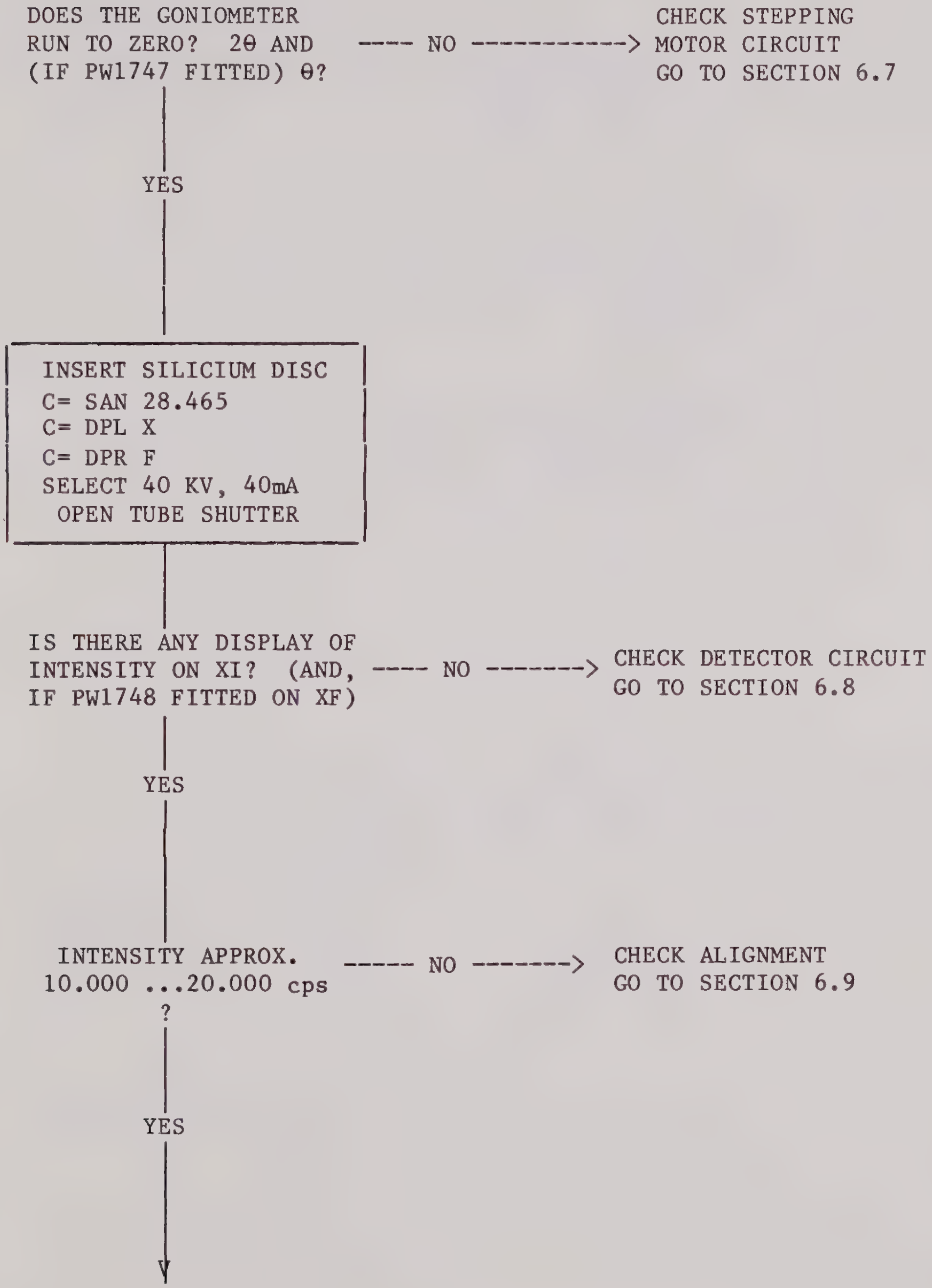
6.2 SYSTEM CHECK


START
SWITCH PW1710 ON
IS THERE ANY LIGHT ON THE DISPLAY?
NO
CHECK POWER MODULE GO TO SECTION 6.3
YES
IS THE MESSAGE "VSx.x TERMINAL=" ON THE PW1710 DISPLAY?
NO
PROCESSOR CHECK GO TO SECTION 6.4
YES

continue on next page


IS VDU CONNECTED AS I/O DEVICE?
YES
NO
IS THE MESSAGE VSx.x TERMINAL= ON VDU?
NO
CHECK VDU GO TO SECTION 6.4
YES
IS A PC1409 PRINTER CONNECTED AS THE I/O DEVICE?
YES
NO
IS THE MESSAGE VSx.x TERMINAL= ON PRINTER?
NO
CHECK PC1409 GO TO SECTION 6.5
YES
DEPRESS "ENTER" ON PW1710
DOES WAIT (1 or 12) APPEAR ON LEFTHAND SECTION OF THE DISPLAY?
NO
CHECK PW1710 KEYBOARD. GO TO SECTION 6.6
YES

continue on next page



DOES THE GONIOMETER RUN TO ZERO? 2θ AND (IF PW1747 FITTED) θ? ---- NO ----> CHECK STEPPING MOTOR CIRCUIT GO TO SECTION 6.7

YES

INSERT SILICIUM DISC
C= SAN 28.465
C= DPL X
C= DPR F
SELECT 40 KV, 40mA
OPEN TUBE SHUTTER

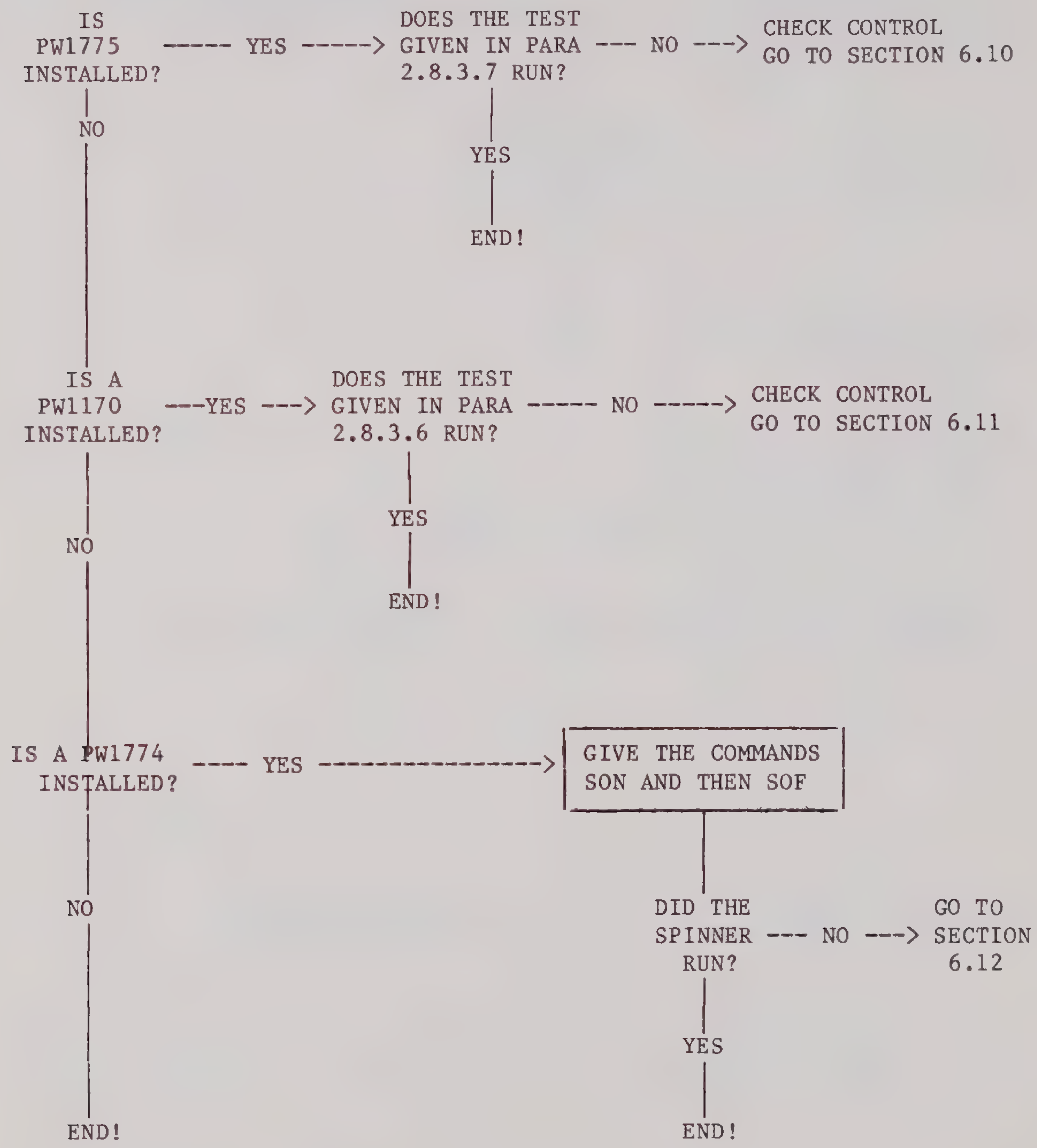
IS THERE ANY DISPLAY OF INTENSITY ON XI? (AND, IF PW1748 FITTED ON XF) ---- NO ----> CHECK DETECTOR CIRCUIT GO TO SECTION 6.8

YES

INTENSITY APPROX. 10.000 ...20.000 cps ? ----- NO ----> CHECK ALIGNMENT GO TO SECTION 6.9

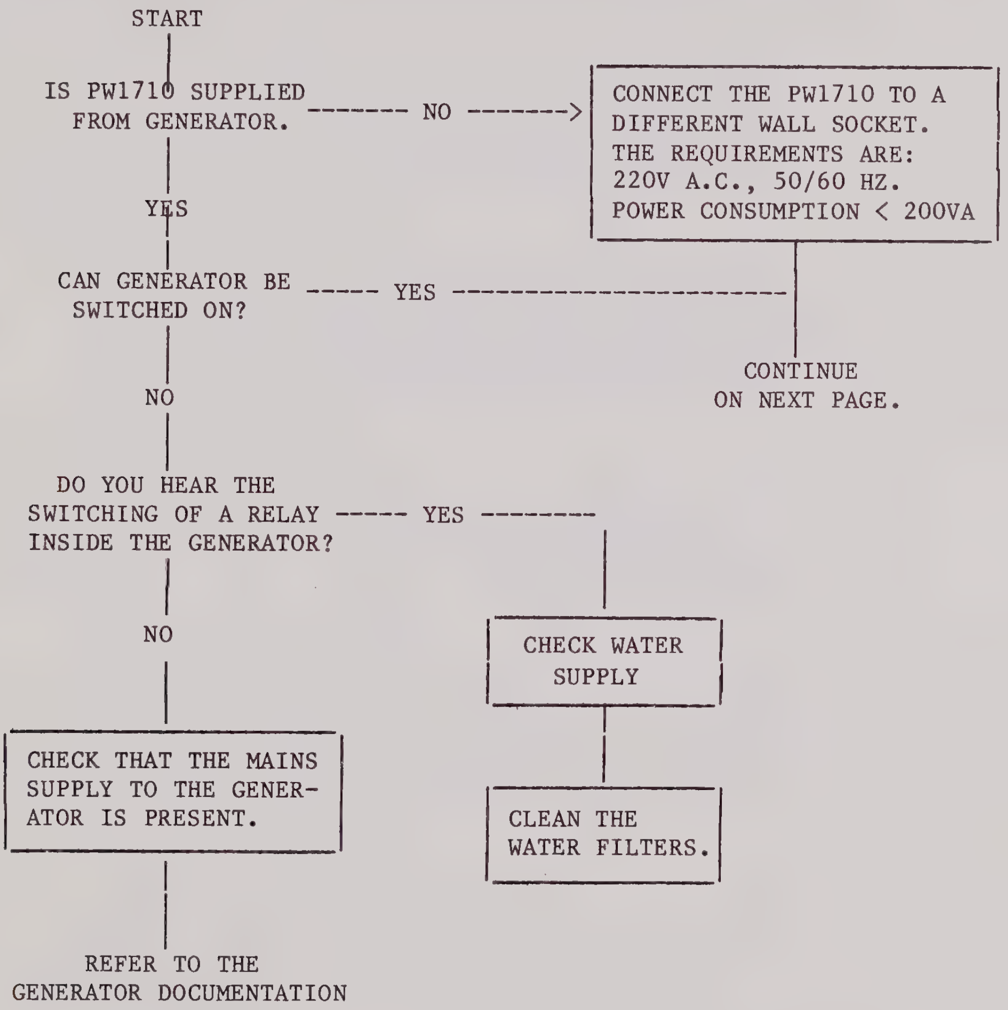
YES

continue on next page


IS PW1775 INSTALLED?
YES
DOES THE TEST GIVEN IN PARA 2.8.3.7 RUN?
NO
CHECK CONTROL GO TO SECTION 6.10
YES
END!
NO
IS A PW1170 INSTALLED?
YES
DOES THE TEST GIVEN IN PARA 2.8.3.6 RUN?
NO
CHECK CONTROL GO TO SECTION 6.11
YES
END!
NO
IS A PW1774 INSTALLED?
YES
GIVE THE COMMANDS SON AND THEN SOF
DID THE SPINNER RUN?
NO
GO TO SECTION 6.12
YES
END!
NO
END!

6.3 CHECK OF POWER MODULE

REQUIREMENT : A MULTIMETER (for example: PHILIPS PM2517)


START
IS PW1710 SUPPLIED FROM GENERATOR.
NO
CONNECT THE PW1710 TO A DIFFERENT WALL SOCKET. THE REQUIREMENTS ARE: 220V A.C., 50/60 HZ. POWER CONSUMPTION < 200VA
YES
CAN GENERATOR BE SWITCHED ON?
YES
CONTINUE ON NEXT PAGE.
NO
DO YOU HEAR THE SWITCHING OF A RELAY INSIDE THE GENERATOR?
YES
CHECK WATER SUPPLY
CLEAN THE WATER FILTERS.
NO
CHECK THAT THE MAINS SUPPLY TO THE GENERATOR IS PRESENT.
REFER TO THE GENERATOR DOCUMENTATION

IF THE PW1710 CANNOT BE SWITCHED ON AT THIS POINT. USE THE MULTIMETER TO CHECK THAT THERE IS 220V A.C. PRESENT AT THE INPUT TO THE POWER MODULE. (REFER TO FIGURE 2.3).

IF VOLTAGE IS PRESENT AND SYSTEM STILL CANNOT BE SWITCHED ON, PROCEED WITH:

PULL THE PW1710 CONTROL MODULE OUT ENOUGH TO SEE THE CARDS INSIDE, AND LOOK TO SEE IF ALL LEDS ARE ON. THESE LEDS INDICATE THE PRESENCE OF THE SUPPLY VOLTAGES.

IF ONE OR MORE OF THE LEDS IS NOT LIT, CHECK THE FUSES. REFER TO FIGURE 2.3.

NOTE 1: If a fuse is replaced, and it blows again, do not replace it a second time, but contact your local Service Representitive.

NOTE 2: Spare fuses are delivered with the system.

6.4 PROCESSOR/VDU CHECK

Set the switch on the System Control PCB front panel to I.

Press RESET.

Every time the RESET button is pressed:

The SOD LED on the System Controller PCB should extinquish and then light again.

The VDU should display: TEST:

If this does not happen:

Processor Check.

Check: 6 MHz on the CPU (D6 on the System Controller) pins 1-2
: 3 MHz output from the CPU pin 37
: 30 KHz output from the System Controller PCB pin C16
: Timer interrupt (RST 7,5) on CPU pin D6, repitition time = 50ms

Set the switch on the System Controller PCB front panel to 0.

If any of these are not present, replace the System Controller PCB.

VDU Check:

If Dual Serial Interface is present, check all the switch settings for both interfaces as described in Section 2.5.3.

Set the VDU parameters as the DSI, with the exception of the echo bit. If the echo bit is set in the DSI and not the VDU, and there is an echo, then the line is O.K.

Reset the PW1710 (or switch OFF and ON again)

Press CR on the VDU, the goniometer should calibrate, and the PW1710, display should display WAIT 1.
When the goniometer has moved to the set position, the VDU should display:

C=
PW1710 will display the previous setting, and the
PW1710 REMOTE lamp should be lit

Give a command, (refer to the Command Survey Card), and check that the command is completed.

If any of the above checks do not occur as described:

1. Replace the Dual Serial Interface PCB and perform the VDU checks again.
2. If that does not cure the fault, replace the System Control PCB or the VDU.

6.5 PRINTER PC1409 (KSR43) CHECK

6.5.1 AS TERMINAL 1

Check that the paper is present and correctly inserted.

Switch the printer ON. If the ALARM lamp lights, check that the printer cover is secure.

Press and hold down the PRINTER TEST button on the printer:

> The printer will print all available characters.
> The ALARM lamp will be lit.
> When all the characters have been printed, the bell will sound.

Release the PRINTER TEST button:

> The LOCAL lamp should light.

Press DATA button:

If the INTERRUPT lamp is lit, check the connection to the PW1710.

Press TERM READY.

Select the correct Baudrate and handshake settings on the DSI.

Set the DUPLEX key on the printer to FULL.

To see if the command reaches the PW1710:

> Press RESET on PW1710.
>
> The printer should print VSx.x TERMINAL=
>
> Press CR, the PW1710 should react by calibrating the goniometer, and printing C= on the printer.
>
> Give a command e.g. SAN 10 CR, and check if it is obeyed.

If any of the above checks do not happen as described:

1. Replace the Dual Serial Interface PCB, and re-check the test that failed.
2. If the fault persists, Replace System Control PCB or the printer.

6.5.2 AS TERMINAL 2

Check that the paper is present and correctly inserted.

Switch the printer ON. If the ALARM lamp lights, check that the printer cover is secured.

Press and hold down the PRINTER TEST button on the printer:

> The printer will print all available characters.
> The ALARM lamp will be lit.
> When all the characters have been printed, the bell will sound.

Release the PRINTER TEST button:

> The LOCAL lamp should light.

Press DATA button:

If the INTERRUPT lamp is lit, check the connection to the PW1710.

Press TERM READY

On the PW1710, press RESET:

> On the printer, the DATA lamp extinguishes,
> TERM READY lights momentarily, then extinguishes and
> DATA lamp lights again.

On terminal 1:

> Press <CR>
> Give the command DON, CR
> Give the command HED, CR

The header "Date, Time, and current program number" should appear on both terminal 1 and the printer.

If any of the above checks do not happen as described:

1. Replace the Dual Serial Interface PCB, and re-check the test that failed.

2. If the fault persists, Replace the printer.

6.6 PW1710 KEYBOARD CHECK

RESET PW1710 and press ENTER,
(If the goniometer runs, wait for it to stop).

The BUSY, ASSEMBLY, and REMOTE lamps should all be extinguished.

Press all the "character" buttons once, until the display is full.

Check that the same character as the one you pressed appears on the display.

Press CLEAR 20 times, until all the characters are cleared from the display, the BUSY lamp lights, and the previous display returns.

Press the numerals 1 to 0, ., and -.

Check that they are all displayed, then clear them by using the CLEAR key.

On the PW1710 keyboard, give the command:

> SAN 30 ENTER, the goniometer should start to run to 30°.
>
> Before the goniometer reaches its final position
>
> Press STOP. The goniometer should stop running.

If any of the buttons should fail, perform the following actions in sequence. After each action, check to see if the fault has been cleared, if it is still there, carry on with the next action.

1. Check the flat ribbon cable between the front panel and the chassis.
2. Check that the button itself is not catching.
3. Replace the Display Keyboard Control PCB.
4. Replace the Display Keyboard.
5. Replace the System Controller PCB.

6.7 STEPPING MOTOR CHECK

This routine is valid for both 2 θ and θ drives. If the problem is with the θ drive, replace the cards in the options rack (PW1747) and not those in the PW1710 control module.

Switch the PW1710 OFF and then ON.

Press ENTER, (or CR on the VDU).

The goniometer should calibrate (run to zero).

Using the PW1710/00 software commands, (refer to the Survey of Commands):

Check all the stepping motor functions
Check that the LED on the Goniometer Control PCB is lit

If any of the functions fail, perform the following actions. After each action, before going on to the next step, check to see if the fault has been rectified.

1. Check the stepping motor cable for proper connection and open circuit.
2. Check the d.c. power supply LEDs on the MOPS card.
3. If θ drive problem, check the wiring between the options rack motherboard and the PW1710 motherboard.
4. Check the fuses on the Power Unit.
5. Replace the Stepping Motor Supply Driver card.
6. Replace the Goniometer Control card.
7. Replace the stepping motor.

6.8 DETECTOR CIRCUIT CHECK

If there are either no counts, or not enough:

1. a. Check the lower and upper level settings.

   b. Check the goniometer alignment.

2. a. Set the switch on the Amplifier Analyser Card to TEST. If the option PW1748 is present, also switch the Amplifier Analyser Card in the options rack to TEST.

   b. Enter the command DPL X, and if PW1748 is present, DPR F.

   c. The display should show XI 29980 (if a PW1748 is present, in left AND right-hand display segments). If it does not, first replace the Amplifier analyser Card, and if that does not cure the fault, the 4 Digit Binary Counter. Change the cards in the PW1710 control module if the left display was not there, and the cards in the options rack if the problem was with the right-hand display.

   d. Set the switch on the Amplifier Analyser Card back to NORM.

3. Check the High Voltage on the output of the HV2000 card:

   For gas detectors it should not be higher than 1800V.

   For scintillation detectors it should not be higher than 1200V.

   If it is not there, replace the card.

4. Replace the Detector.

Set the goniometer for a reflection angle:

1. Press the CAL button behind the front panel, and enter PHD. Note the reading on the recorder.

2. Enter PHD (not pressing CAL).

3. If there is any difference between 1 and 2, adjust the HT.

4. If adjustment of the HT is not possible, replace the Amplifier Analyser Card.

If the detector resolution is out of specification:

Replace the Detector.

6.9 ALIGNMENT CHECK

Check the alignment as follows:

1. Insert the standard silicon sample into the goniometer.
2. Set the goniometer to a known reflection angle. e.g. 56,12°for a CU tube.
3. Run the following program:

```
SAN  56,12
MXN  20
MXT  1
MXS  0,01
MAX
```

If the maximum count is not found on 56,12° ± 0,1°, realign the goniometer according to the alignment instructions contained in the goniometer manual.

6.10 SAMPLE CHANGER CHECK (PW1775)

If the Sample Changer does not function:

1. Check the operation of the sample changer by means of the Test switch on the PCB of the PW1775 Sample Changer, as described in the PW1775 documentation.

If all of these functions are correct:

2. Check the cable connections

If the Sample Changer still does not function correctly:

3. Replace the Changer Spinner Shutter Control Card.
4. Check the position of the sample detector inside the PW1775 or the PW1774.

6.11 PW1170 SAMPLE CHANGER AND PW1717 INTERFACE CHECK

Check the operation of the PW1170 by using the software commands.

If any of the functions do not work:

1. Check the connecting cable.
2. Check the micro-switches in the PW1170. (Refer to the PW1170 documentation).
3. Replace the PW1717 Interface.

6.12 SPINNER CONTROL CHECK (PW1774)

Check the operation of the Spinner using the software commands.

If any of the functions do not work:

1. Check the connecting cable.
2. Check the Spinner.
3. Replace the Shutter/Spinner Control Card.

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7.1 INTRODUCTION

This chapter comprises a list of parts for each of the printed circuit boards in the PW1710/00 together with all of the options. The printed circuit boards are listed in the same sequence as they are in ChAPTER 4. If you need to refer to the card component layout, they are all provided at the rear of Chapter 4.

7.2 SYSTEM CONTROL CARD 5322 694 14473

7.2.1 CAPACITORS

Item	Description			Ordering Code
C 0001	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945
C 0002	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0003	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0004	CAPACITOR,CERAM	2%	22PF	4822 122 31063
C 0005	CAPACITOR,CERAM	-20+80%	1NF	4822 122 30027
C 0006	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0007	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0008	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0009	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945
C 0010	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0011	CAP,ELECTROLYT.	16V 20%	15UF	4822 124 20977
C 0012	CAP,ELECTROLYT.	16V 20%	15UF	4822 124 20977
C 0013	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0014	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945

7.2.2 INTEGRATED CIRCUITS

Item	Description		Ordering Code
D 0005	INTEGR.CIRCUIT	N74LS74AN	4822 209 80782
D 0007	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0008	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 0009	INTEGR.CIRCUIT	HM6116LP-4	5322 209 81081
D 0010	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0011	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0014	INTEGR.CIRCUIT	N74LS42N	4822 209 50008
D 0015	INTEGR.CIRCUIT	HEF4526BD	4822 209 10289
D 0016	INTEGR.CIRCUIT	HEF40175BD	4822 209 10284
D 0017	INTEGR.CIRCUIT	HEF4737VD	5322 209 14842
D 0018	INTEGR.CIRCUIT	N74LS90N	5322 209 85255
D 0019	INTEGR.CIRCUIT	HEF4518BD	4822 209 10275
D 0020	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 0021	INTEGR.CIRCUIT	N74LS42N	4822 209 50008
D 0022	INTEGR.CIRCUIT	N74LS02N	5322 209 85312
D 0023	INTEGR.CIRCUIT	N74LS32N	5322 209 85311
D 0024	INTEGR.CIRCUIT	HEF4072BD	4822 209 10308
D 0025	INTEGR.CIRCUIT	N74LS04N	4822 209 80783
D 0026	INTEGR.CIRCUIT	HEF4023BD	4822 209 10252
D 0027	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0028	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0029	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0030	INTEGR.CIRCUIT	HEF4011BD	4822 209 10247
D 0031	INTEGR.CIRCUIT	HEF4044BD	4822 209 10305
D 0032	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0033	INTEGR.CIRCUIT	N74LS174N	4822 209 50008
D 0034	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0035	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0036	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0037	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0038	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0039	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0040	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0041	INTEGR.CIRCUIT	N7407N	5322 209 84761

Item	Description			Ordering Code

7.2.3 RESISTORS

Item	Description			Ordering Code
R 0001	RESISTOR,M.FILM	MR25	1% 3K32	5322 116 54005
R 0002	RESISTOR,M.FILM	MR25	1% 3K32	5322 116 54005
R 0003	RESISTOR,M.FILM	MR25	1% 15K4	5322 116 55459
R 0004	RESISTOR,M.FILM	MR25	1% 1M	5322 116 55535
R 0005	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0006	RESISTOR,M.FILM	MR25	1% 178E	5322 116 54492
R 0007	RESISTOR,M.FILM	MR25	1% 48K7	5322 116 50442
R 0008	RESISTOR,M.FILM	MR25	1% 332E	4822 116 51226
R 0009	RESISTOR,M.FILM	MR25	1% 332E	4822 116 51226
R 0010	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0011	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0012	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0013	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0015	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0016	RESISTOR,M.FILM	MR25	1% 48K7	5322 116 50442
R 0017	RESISTOR,M.FILM	MR25	1% 82E5	5322 116 54462
R 0020	RESISTOR,M.FILM	MR25	1% 48K7	5322 116 50442
R 0021	RESISTOR.WW.	7X0.2W	2% 100K	5322 111 94254
R 0022	RESISTOR,M.FILM	MR25	1% 1K	4822 116 51235
R 0023	RESISTOR.WW.	7X0.2W	2% 100K	5322 111 94254
R 0024	RESISTOR.WW.	7X0.2W	2% 100K	5322 111 94254
R 0025	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0026	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0027	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0028	RESISTOR,M.FILM	MR25	1% 10K	4822 116 51253
R 0029	RESISTOR,M.FILM	MR25	1% 332E	4822 116 51226
R 0030	RESISTOR,M.FILM	MR25	1% 100K	4822 116 51268

7.2.4 SEMICONDUCTORS

Item	Description		Ordering Code
V 0001	LED	CQY24B-III	4822 130 31144
V 0002	DIODE,REFERENCE	BZV46-C2V0	4822 130 31248
V 0003	TRANSISTOR	BC638	4822 130 41087
V 0004	TRANSISTOR	BC549C	4822 130 44246
V 0005	TRANSISTOR	BC549C	4822 130 44246
V 0006	DIODE	BAW62	4822 130 30613
V 0007	TRANSISTOR	BC549C	4822 130 44246
V 0008	DIODE,REFERENCE	BZX79-C6V8	4822 130 34278

7.2.5 MISCELLANEOUS

Item	Description		Ordering Code
G 0001	BATTERY	3,6V	4822 138 10046
S 0001	SWITCH		5322 277 14232
	SOCKET,MALE		5322 265 64082
	SOCKET,IC		5322 255 40248
	SOCKET,IC		5322 255 44217

7.2.6 PROMS

Item	Description		Ordering Code
D 1	BOARD,PRINTED	PROM D1 SYSTEM CONTR	5322 694 14564
D 2	BOARD,PRINTED	PROM D2 SYSTEM CONTR	5322 694 14565
D 3	BOARD,PRINTED	PROM D3 SYSTEM CONTR	5322 694 14566
D 4	BOARD.PRINTED	PROM D4 SYSTEM CONTR	5322 694 14567
D 5	BOARD,PRINTED	PROM D5 SYSTEM CONTR	5322 694 14583

Item Description Ordering Code

7.3 MEMORY EXTENSION 5322 694 14714

7.3.1 CAPACITORS

Item	Description	Ordering Code
C 0001	-20+80% 22NF	4822 122 30103
C 0002	-20+80% 22NF	4822 122 30103

7.3.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0001	74LS02	5322 209 85312
D 0003	74LS02	5322 209 85312
D 0004	HEF4011BD	4822 209 10247
D 0005	SN74LS373N-00	5322 209 86062
D 0006	74LS42	4822 209 80781
D 0006	P8085-AH	5322 209 50032
D 0007	SN74LS373N-00	5322 209 86062
D 0008	HEF4724BD	4822 209 10316

7.3.3 RESISTORS

Item	Description	Ordering Code
R 0001	MR25 1% 48K7	5322 116 50442

7.3.4 MISCELLANEOUS

Item	Description	Ordering Code
	I C VOET DIL	5322 255 44217
	I C VOET DIL	5322 255 40248
	SCHUIFSCHAK	5322 277 24045
	ADAPTER PLUG	5322 263 50102
	I C VOET DIL	5322 255 44047

7.4 DUAL SERIAL INTERFACE CARD 5322 694 14475

7.4.1 CAPACITORS

Item	Description			Ordering Code
C 0001	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0002	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0003	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0004	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0005	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0006	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0007	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0008	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0009	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0010	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0011	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0012	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0013	CAPACITOR,CERAM	2%	56PF	4822 122 31521
C 0014	CAPACITOR,CERAM	2%	56PF	4822 122 31521
C 0015	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0016	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0017	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0018	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0019	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945
C 0020	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945
C 0021	CAP,ELECTROLYT.	16V 20%	15UF	4822 124 20977
C 0022	CAP,ELECTROLYT.	16V 20%	15UF	4822 124 20977
C 0023	CAP,ELECTROLYT.	-10+50%	100UF	5322 124 24178
C 0024	CAP,ELECTROLYT.	16V 20%	15UF	4822 124 20977

7.4.2 INTEGRATED CIRCUITS

Item	Description		Ordering Code
D 0001	INTEGR.CIRCUIT	HEF4049BD	4822 209 10306
D 0002	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0003	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0004	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0005	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0006	INTEGR.CIRCUIT	N8T16N	5322 209 85831
D 0007	INTEGR.CIRCUIT	N8T16N	5322 209 85831
D 0008	INTEGR.CIRCUIT	N8T16N	5322 209 85831
D 0009	INTEGR.CIRCUIT	N8T16N	5322 209 85831
D 0010	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0011	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0012	INTEGR.CIRCUIT	4702BDC	5322 209 81662
D 0013	INTEGR.CIRCUIT	4702BDC	5322 209 81662
D 0014	INTEGR.CIRCUIT	N8T15N	5322 209 85829
D 0015	INTEGR.CIRCUIT	N8T15N	5322 209 85829
D 0016	INTEGR.CIRCUIT	N8T15N	5322 209 85829
D 0017	INTEGR.CIRCUIT	P8251A	5322 209 85847
D 0018	INTEGR.CIRCUIT	P8251A	5322 209 85847
D 0019	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0020	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0021	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0022	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0023	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0024	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0025	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0026	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0027	INTEGR.CIRCUIT	N74LS42N	4822 209 50008
D 0028	INTEGR.CIRCUIT	HEF4071BD	4822 209 10307
D 0029	INTEGR.CIRCUIT	N74LS32N	5322 209 85311
D 0030	INTEGR.CIRCUIT	N74LS32N	5322 209 85311
D 0031	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0032	INTEGR.CIRCUIT	HEF4050BD	4822 209 10261
D 0033	INTEGR.CIRCUIT	HEF4049BD	4822 209 10306
D 0034	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281
D 0035	INTEGR.CIRCUIT	HEF4072BD	4822 209 10308

7.4.3 RESISTORS

R 0001	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0002	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0003	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0004	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0005	RESISTOR,M.FILM	MR25	1%	178E	5322 116 54492
R 0006	RESISTOR,M.FILM	MR25	1%	178E	5322 116 54492
R 0007	RESISTOR,M.FILM	MR25	1%	178E	5322 116 54492
R 0008	RESISTOR,M.FILM	MR25	1%	178E	5322 116 54492
R 0009	COMPOSITIONRES.	5X0.2W	2%	10K	5322 111 94203
R 0010	COMPOSITIONRES.	5X0.2W	2%	10K	5322 111 94203
R 0011	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0012	RESISTOR,M.FILM	PR37	5%	1K	5322 116 54909
R 0013	RESISTOR,M.FILM	PR37	5%	1K	5322 116 54909
R 0014	RESISTOR,M.FILM	PR37	5%	1K	5322 116 54909
R 0015	RESISTOR,M.FILM	PR37	5%	1K	5322 116 54909

Item	Description				Ordering Code
R 0016	RESISTOR,HT	CR25	5%	10M	4822 110 72214
R 0017	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0018	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0019	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0020	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0021	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0023	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0024	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0025	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0026	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0028	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0029	RESISTOR,M.FILM	MR25	1%	154K	5322 116 54714
R 0030	RESISTOR,M.FILM	MR25	1%	154K	5322 116 54714
R 0031	RESISTOR,M.FILM	MR25	1%	154K	5322 116 54714
R 0032	RESISTOR,M.FILM	MR25	1%	121E	5322 116 54426
R 0033	RESISTOR,M.FILM	MR25	1%	154K	5322 116 54714
R 0034	RESISTOR,M.FILM	MR25	1%	121E	5322 116 54426

7.4.4 SEMICONDUCTORS

V 0001	TRANSISTOR	BC549C	4822 130 44246
V 0002	TRANSISTOR	BC549C	4822 130 44246
V 0003	TRANSISTOR	BC549C	4822 130 44246
V 0004	TRANSISTOR	BC549C	4822 130 44246
V 0005	DIODE	BAX12A	5322 130 34605
V 0006	DIODE	BAX12A	5322 130 34605
V 0007	DIODE,REFERENCE	BZX79-C3V6	5322 130 34834
V 0008	DIODE,REFERENCE	BZX79-C3V6	5322 130 34834
V 0009	DIODE,REFERENCE	BZX79-C6V8	4822 130 34278

7.4.5 MISCELLANEOUS

SOCKET,MALE	5322 265 64082
SWITCH	5322 277 24045
SOCKET	5322 267 70121
SOCKET,MALE	5322 265 64097
CONNECTOR	5322 265 54044
CONNECTOR	5322 267 54149
SOCKET	5322 268 20109
PLUG	5322 267 64058

7.5 DISPLAY KEYBOARD CONTROL CARD

5322 694 14471

7.5.1 CAPACITORS

C 0001	-20+80%	22NF	4822 122 30103
C 0002	-20+80%	22NF	4822 122 30103
C 0003	-20+80%	22NF	4822 122 30103
C 0004	-20+80%	22NF	4822 122 30103
C 0005	-20+20%	100UF	5322 124 24091
C 0006	-20+20%	68UF	5322 124 24095
C 0007	-20+20%	68UF	5322 124 24095
C 0008	-10+50%	150UF	4822 124 20799
C 0009	-20+80%	22NF	4822 122 30103

7.5.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0001	UA741CN	4822 209 80617
D 0002	UA741CN	4822 209 80617
D 0003	HEF4049BD	4822 209 10306
D 0004	HEF4049BD	4822 209 10306
D 0005	SN74LS373N-00	5322 209 86062
D 0006	HEF4104BD	4822 209 10273
D 0007	HEF4104BD	4822 209 10273
D 0008	HEF4049BD	4822 209 10306
D 0009	SN74LS373N-00	5322 209 86062
D 0010	HEF4073BD	4822 209 10266
D 0011	HEF4023BD	4822 209 10252
D 0012	HEF4011BD	4822 209 10247
D 0013	HEF4082BD	4822 209 10271
D 0014	HEF4012BD	4822 209 10294

7.5.3 RESISTORS

Item	Description	Ordering Code
R 0001	MR25 1% 464E	5322 116 50536
R 0002	MR25 1% 464E	5322 116 50536
R 0003	MR25 1% 4K64	5322 116 50484
R 0004	MR25 1% 4K64	5322 116 50484
R 0005	MR25 1% 2K15	5322 116 50767
R 0006	MR25 1% 464E	5322 116 50536
R 0007	0.05W 20% 10K	4822 100 10035
R 0008	4W 5% 18E	4822 112 21061
R 0009	MR25 1% 1K	4822 116 51235

7.5.4 SEMICONDUCTORS

Item	Description	Ordering Code
V 0001	BC547B	4822 130 40959
V 0002	BY179	4822 130 31638
V 0003	BZX79-C47	4822 130 34383
V 0004	BZX79-C33	4822 130 34142
V 0005	BD681	5322 130 44786
V 0006	BZX87-C7V5	5322 130 34596
V 0007	BZX87-C8V2	5322 130 34577
V 0008	BZX79-C6V8	4822 130 34278

7.5.5 MISCELLANEOUS

7.6 DISPLAY KEYBOARD 5322 694 14502

7.6.1 CAPACITORS

Item	Description			Ordering Code
C 0001	CAP,ELECTROLYT.	-10+50%	330UF	4822 124 20684
C 0002	CAP,ELECTROLYT.	-10+50%	220UF	4822 124 20693
C 0003	CAP,ELEC.TANTAL	10V 20%	15UF	5322 124 14036
C 0004	CAPACITOR,CERAM	10%	3.9NF	4822 122 30098
C 0005	CAPACITOR,CERAM	0.25PF	5.6PF	4822 122 31047
C 0006	CAPACITOR,CERAM	0.25PF	5.6PF	4822 122 31047
C 0007	CAP,ELECTROLYT.	10V 20%	33UF	4822 124 20945
C 0008	CAP,ELEC.TANTAL	10V 20%	15UF	5322 124 14036
C 0009	CAPACITOR,CERAM	-20+80%	10NF	4822 122 30043
C 0010	CAP,ELECTROLYT.	25V 20%	1UF	4822 124 20944
C 0011	CAPACITOR,CERAM	10%	470PF	4822 122 30034
C 0012	CAP,ELEC.TANTAL	10V 20%	15UF	5322 124 14036
C 0014	CAP,ELEC.TANTAL	10V 20%	15UF	5322 124 14036
C 0015	CAPACITOR,CERAM	10%	2.2NF	4822 122 30114

7.6.2 INTEGRATED CIRCUITS

Item	Description		Ordering Code
D 0001	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0002	INTEGR.CIRCUIT	HEF4011BD	4822 209 10247
D 0003	INTEGR.CIRCUIT	HEF4049BD	4822 209 10306
D 0004	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0005	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0006	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0007	INTEGR.CIRCUIT	HEF4071BD	4822 209 10307
D 0008	INTEGR.CIRCUIT	SN74LS373N-00	5322 209 86062
D 0009	INTEGR.CIRCUIT	MCM51L01P45	5322 209 14445
D 0010	INTEGR.CIRCUIT	MCM51L01P45	5322 209 14445
D 0011	INTEGR.CIRCUIT	MCM51L01P45	5322 209 14445
D 0012	INTEGR.CIRCUIT	MCM51L01P45	5322 209 14445
D 0013	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0014	INTEGR.CIRCUIT	HEF4532BD	4822 209 10278
D 0015	INTEGR.CIRCUIT	HEF4532BD	4822 209 10278
D 0016	INTEGR.CIRCUIT	HEF40193BD	4822 209 10286
D 0017	INTEGR.CIRCUIT	HEF40193BD	4822 209 10286
D 0018	INTEGR.CIRCUIT	HEF4081BD	4822 209 10269
D 0019	INTEGR.CIRCUIT	HEF4515BD	4822 209 10312
D 0020	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281

7.6.3 RESISTORS

Item	Description				Ordering Code
R 0001	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0002	RESISTOR,M.FILM	MR25	1%	51K1	5322 116 50672
R 0003	RESISTOR,M.FILM	MR25	1%	51K1	5322 116 50672
R 0004	RESISTOR,M.FILM	MR25	1%	51K1	5322 116 50672
R 0005	RESISTOR,M.FILM	MR25	1%	51K1	5322 116 50672
R 0006	RESISTOR,M.FILM	MR25	1%	4K87	5322 116 55445
R 0007	RESISTOR,M.FILM	MR25	1%	59K	5322 116 54678
R 0008	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0009	RESISTOR,M.FILM	MR25	1%	14K7	5322 116 54632
R 0010	COMPOSITIONRES.	4X0.3W	2%	330E	5322 111 94182
R 0011	COMPOSITIONRES.	4X0.3W	2%	4K7	5322 111 94153

Item	Description	Ordering Code
R 0012	RESISTOR,M.FILM MR25 1% 22K6	5322 116 50481
R 0013	RESISTOR,M.FILM MR25 1% 22K6	5322 116 50481
R 0014	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0015	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0016	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0017	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0018	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0019	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0020	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0021	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0022	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0023	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0024	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0025	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0026	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0027	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0028	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0029	RESISTOR.WW. 7X0.2W 2% 22K	5322 111 94191
R 0030	RESISTOR.WW. 7X0.2W 2% 22K	5322 111 94191
R 0031	RESISTOR.WW. 7X0.2W 2% 22K	5322 111 94191
R 0032	RESISTOR.WW. 7X0.2W 2% 22K	5322 111 94191
R 0033	RESISTOR.WW. 7X0.2W 2% 22K	5322 111 94191
R 0034	RESISTOR,M.FILM MR25 1% 1K69	5322 116 54567
R 0035	RESISTOR,M.FILM MR25 1% 3K32	5322 116 54005
R 0036	RESISTOR,M.FILM MR25 1% 4K02	5322 116 55448

7.6.4 SEMICONDUCTORS

V 0001	TRANSISTOR	BC547B	4822 130 40959
V 0002	TRANSISTOR	BC547B	4822 130 40959
V 0003	TRANSISTOR	BC547B	4822 130 40959
V 0004	TRANSISTOR	BC547B	4822 130 40959
V 0005	TRANSISTOR	BCY59-X	5322 130 44453
V 0006	THYRISTOR	BSS68	5322 130 44247
V 0007	THYRISTOR	BSS68	5322 130 44247
V 0008	THYRISTOR	BSS68	5322 130 44247
V 0009	THYRISTOR	BSS68	5322 130 44247
V 0010	THYRISTOR	BSS68	5322 130 44247
V 0011	THYRISTOR	BSS68	5322 130 44247
V 0012	THYRISTOR	BSS68	5322 130 44247
V 0013	THYRISTOR	BSS68	5322 130 44247
V 0014	THYRISTOR	BSS68	5322 130 44247
V 0015	THYRISTOR	BSS68	5322 130 44247
V 0016	THYRISTOR	BSS68	5322 130 44247
V 0017	THYRISTOR	BSS68	5322 130 44247
V 0018	THYRISTOR	BSS68	5322 130 44247
V 0019	THYRISTOR	BSS68	5322 130 44247
V 0020	THYRISTOR	BSS68	5322 130 44247
V 0021	THYRISTOR	BSS68	5322 130 44247
V 0022	THYRISTOR	BSS68	5322 130 44247
V 0023	THYRISTOR	BSS68	5322 130 44247
V 0024	THYRISTOR	BSS68	5322 130 44247
V 0025	THYRISTOR	BSS68	5322 130 44247
V 0026	THYRISTOR	BSS68	5322 130 44247
V 0027	THYRISTOR	BSS68	5322 130 44247
V 0028	THYRISTOR	BSS68	5322 130 44247
V 0029	THYRISTOR	BSS68	5322 130 44247
V 0030	THYRISTOR	BSS68	5322 130 44247

Item	Description		Ordering Code
V 0031	THYRISTOR	BSS68	5322 130 44247
V 0032	THYRISTOR	BSS68	5322 130 44247
V 0033	THYRISTOR	BSS68	5322 130 44247
V 0034	THYRISTOR	BSS68	5322 130 44247
V 0035	THYRISTOR	BSS68	5322 130 44247
V 0036	THYRISTOR	BSS68	5322 130 44247
V 0037	THYRISTOR	BSS68	5322 130 44247
V 0038	THYRISTOR	BSS68	5322 130 44247
V 0039	THYRISTOR	BSS68	5322 130 44247
V 0040	THYRISTOR	BSS68	5322 130 44247
V 0041	THYRISTOR	BSS68	5322 130 44247
V 0042	DIODE	BAV21	4822 130 30842
V 0043	DIODE	BAV21	4822 130 30842
V 0044	DIODE	BAW62	4822 130 30613
V 0045	DIODE	BAW62	4822 130 30613
V 0046	DIODE	BAW62	4822 130 30613
V 0047	LED	CQY94-III	5322 130 35006
V 0048	LED	CQY94-III	5322 130 35006
V 0049	LED	CQY94-III	5322 130 35006
V 0050	DISPLAY	FG209M2	5322 131 90069
V 0051	DIODE	BAW62	4822 130 30613
V 0052	DIODE	BAW62	4822 130 30613

7.6.5 MISCELLANEOUS

	HOUSING,CONNECT	BLOK MOD4	5322 268 44141
	SWITCH,PUSHBUT.		5322 276 14338
A 26	KEYBOARD	DISPLAY KEYBOARD	5322 694 14502

7.7 SECONDARY CONTROL PANEL

5322 694 14503

7.7.1 RESISTORS

R 0001	RESISTOR,M.FILM	MR25	1%	2K37	5322 116 54576
R 0002	RESISTOR,M.FILM	MR25	1%	1K65	5322 116 54566
R 0003	RESISTOR,M.FILM	MR25	1%	1K18	5322 116 54556
R 0004	RESISTOR,M.FILM	MR25	1%	825E	5322 116 54541
R 0005	RESISTOR,M.FILM	MR25	1%	590E	5322 116 50561
R 0006	RESISTOR,M.FILM	MR25	1%	412E	5322 116 54521
R 0007	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0010	RESISTOR,M.FILM	MR25	1%	1K47	5322 116 50635
R 0011	RESISTOR,M.FILM	MR25	1%	511E	4822 116 51282
R 0012	RESISTOR,M.FILM	MR25	1%	205E	5322 116 55365
R 0013	RESISTOR,M.FILM	MR25	1%	365E	5322 116 54516
R 0014	RESISTOR,M.FILM	MR25	1%	1K15	5322 116 50415
R 0015	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0016	RESISTOR,M.FILM	MR25	1%	100E	5322 116 55549
R 0017	POTM,TRIMMING	1W	10%	50K	5322 101 10517
R 0019	RESISTOR,M.FILM	MR25	1%	18K7	5322 116 55362
R 0020	POTM,TRIMMING	1W	10%	50K	5322 101 10517
R 0022	RESISTOR,M.FILM	MR25	1%	68K1	4822 116 51266

7.7.2 MISCELLANEOUS

Item	Description	Ordering Code
	SOCKET,FEMALE	5322 265 54058
	CONNECTOR	5322 265 54059
	SWITCH	5322 276 11046
	SWITCH,SLIDE	5322 277 24006
	SWITCH,PUSHBUT.	5322 276 14338
	SWITCH	5322 277 24045

7.8 GONIOMETER CONTROL CARD

5322 694 14472

7.8.1 CAPACITORS

Item	Description		Ordering Code
C 0001	-20+80%	22NF	4822 122 30103
C 0002	-20+80%	22NF	4822 122 30103
C 0003	-20+80%	22NF	4822 122 30103
C 0004	-20+80%	22NF	4822 122 30103
C 0005	-20+80%	22NF	4822 122 30103
C 0006	-20+80%	22NF	4822 122 30103
C 0008	2%	22PF	4822 122 31063
C 0009	10%	470PF	4822 122 30034
C 0010	-20+80%	22NF	4822 122 30103
C 0011	-20+80%	22NF	4822 122 30103
C 0012	-20+80%	22NF	4822 122 30103
C 0013	-20+80%	22NF	4822 122 30103
C 0014	-20+80%	22NF	4822 122 30103
C 0015	-20+80%	22NF	4822 122 30103
C 0016	-20+80%	22NF	4822 122 30103
C 0017	-20+80%	22NF	4822 122 30103
C 0018	-20+80%	22NF	4822 122 30103
C 0019	25V 20%	2.2UF	4822 124 21255
C 0020	25V 20%	2.2UF	4822 124 21255
C 0021	25V 20%	2.2UF	4822 124 21255
C 0022	-20+80%	22NF	4822 122 30103
C 0023	100V 10%	100NF	5322 121 40323
C 0024	2%	220PF	4822 122 31506

7.8.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0001	P8085-AH	5322 209 50032
D 0002	P8155H	5322 209 10526
D 0003	P8255A	5322 209 86126
D 0005	HEF4528BD	4822 209 10277
D 0006	N74LS139N	5322 209 85839
D 0007	SN74LS373N-00	5322 209 86062
D 0008	HEF4081BD	4822 209 10269
D 0009	HEF4013BD	4822 209 10248
D 0010	HEF4049BD	4822 209 10306
D 0011	HEF4050BD	4822 209 10261
D 0012	HEF4050BD	4822 209 10261
D 0013	HEF4050BD	4822 209 10261
D 0014	HEF4104BD	4822 209 10273
D 0015	HEF4104BD	4822 209 10273
D 0016	HEF4104BD	4822 209 10273
D 0017	HEF4104BD	4822 209 10273
D 0018	HEF4104BD	4822 209 10273
D 0019	HEF4104BD	4822 209 10273

Item	Description	Ordering Code
D 0020	HEF4104BD	4822 209 10273
D 0021	HEF4051BD	4822 209 10262
D 0022	HEF4051BD	4822 209 10262
D 0023	HEF4051BD	4822 209 10262
D 0024	HEF4051BD	4822 209 10262
D 0025	HEF4556BD	4822 209 10281
D 0026	HEF4104BD	4822 209 10273

7.8.3 RESISTORS

R 0001	MR25	1%	51E1	5322 116 54442
R 0002	MR25	1%	51K1	5322 116 50672
R 0003	MR25	1%	5K11	5322 116 54595
R 0004	MR25	1%	5K11	5322 116 54595
R 0005	MR25	1%	5K11	5322 116 54595
R 0006	MR25	1%	5K11	5322 116 54595
R 0007	MR25	1%	51E1	5322 116 54442
R 0008	MR25	1%	51K1	5322 116 50672
R 0009	MR25	1%	511K	5322 116 55258
R 0010	MR25	1%	51E1	5322 116 54442
R 0011	MR25	1%	51K1	5322 116 50672
R 0012	MR25	1%	5K11	5322 116 54595
R 0013	MR25	1%	5K11	5322 116 54595
R 0014	MR25	1%	5K11	5322 116 54595
R 0015	MR25	1%	10K	4822 116 51253
R 0016	MR25	1%	10K	4822 116 51253
R 0017	MR25	1%	10K	4822 116 51253
R 0018	MR25	1%	10K	4822 116 51253
R 0019	MR25	1%	511E	4822 116 51282
R 0020	MR25	1%	10K	4822 116 51253
R 0021	MR25	1%	10K	4822 116 51253
R 0022	MR25	1%	10K	4822 116 51253
R 0023	MR25	1%	10K	4822 116 51253
R 0024	MR25	1%	10K	4822 116 51253
R 0025	MR25	1%	10K	4822 116 51253
R 0026	MR25	1%	274E	5322 116 54504
R 0027	7X0.2W	2%	100K	5322 111 94254
R 0028	7X0.2W	2%	100K	5322 111 94254
R 0029	7X0.2W	2%	100K	5322 111 94254
R 0030	7X0.2W	2%	100K	5322 111 94254
R 0031	MR25	1%	51K1	5322 116 50672
R 0032	MR25	1%	10K	4822 116 51253

7.8.4 SEMICONDUCTORS

V 0001	BC547B	4822 130 40959
V 0002	BC547B	4822 130 40959
V 0003	BC547B	4822 130 40959
V 0004	BC547B	4822 130 40959
V 0005	BZX79-C6V8	4822 130 34278
V 0006	CQY94-III	5322 130 35006

7.8.5 PROMS

D 4	BOARD,PRINTED PROM 1 GONCON	5322 694 14568

7.9 STEPPING MOTOR SUPPLY DRIVER

Ordering Code: 5322 694 14335

7.9.1 CAPACITORS

Item	Description	Ordering Code
C 0005	CAPACITOR,FOIL 100V 10% 1.5UF	4822 121 40215
C 0007	CAP,ELECTROLYT. -10+50% 680UF	4822 124 20794
C 0008	CAP,ELECTROLYT. -10+50% 680UF	4822 124 20794
C 0009	CAP,ELECTROLYT. -10+50% 680UF	4822 124 20794
C 0010	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771
C 0011	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771
C 0012	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771
C 0013	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771
C 0014	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771
C 0015	CAP,ELECTROLYT. -10+50% 2200UF	4822 124 20771

7.9.2 RESISTORS

Item	Description	Ordering Code
R 0001	RESISTOR,M.FILM CR25 5% 10K	4822 110 73134
R 0002	RESISTOR,M.FILM CR25 5% 10K	4822 110 73134
R 0003	RESISTOR,M.FILM CR25 5% 10K	4822 110 73134
R 0004	RESISTOR,M.FILM CR25 5% 10K	4822 110 73134
R 0005	RESISTOR,M.FILM CR25 5% 10K	4822 110 73134
R 0006	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0007	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0008	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0009	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0010	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0011	RESISTOR,CARBON CR37 5% 39E	4822 110 53069
R 0012	RESISTOR,CARBON CR37 5% 39E	4822 110 53069
R 0013	RESISTOR,CARBON CR37 5% 39E	4822 110 53069
R 0014	RESISTOR,CARBON CR37 5% 39E	4822 110 53069
R 0015	RESISTOR,M.FILM CR25 5% 1K	4822 110 73107
R 0016	RESISTOR,M.FILM CR25 5% 1K	4822 110 73107
R 0017	RESISTOR,M.FILM CR25 5% 1K	4822 110 73107
R 0018	RESISTOR,M.FILM CR25 5% 1K	4822 110 73107
R 0019	RESISTOR.WW. 4W 5% 270E	4822 112 21092
R 0020	RESISTOR.WW. 4W 5% 270E	4822 112 21092
R 0021	RESISTOR,M.FILM CR25 5% 2K2	4822 110 73116
R 0022	RESISTOR,M.FILM CR25 5% 2K2	4822 110 73116
R 0023	RESISTOR,M.FILM CR25 5% 5K6	4822 110 73127
R 0024	RESISTOR,M.FILM CR25 5% 2K2	4822 110 73116

7.9.3 SEMICONDUCTORS

Item	Description	Ordering Code
V 0001	TRANSISTOR BSS51	5322 130 44451
V 0002	TRANSISTOR BSS51	5322 130 44451
V 0003	TRANSISTOR BSS51	5322 130 44451
V 0004	TRANSISTOR BSS51	5322 130 44451
V 0005	TRANSISTOR BCY59-X	5322 130 44453
V 0006	TRANSISTOR BDX78 (TO220)	5322 130 44278
V 0007	TRANSISTOR BDX78 (TO220)	5322 130 44278
V 0008	TRANSISTOR BDX78 (TO220)	5322 130 44278
V 0009	TRANSISTOR BDX78 (TO220)	5322 130 44278
V 0010	TRANSISTOR BCY70	5322 130 40324
V 0011	TRANSISTOR BDX63	5322 130 44477
V 0012	DIODE BY527	4822 130 31509
V 0013	DIODE BY527	4822 130 31509

Item	Description		Ordering Code
V 0014	DIODE	BY527	4822 130 31509
V 0015	DIODE	BY527	4822 130 31509
V 0016	DIODE	BYX71-600	4822 130 34522
V 0017	DIODE	BYX71-600R	4822 130 30866
V 0018	DIODE	BYX71-600R	4822 130 30866
V 0019	DIODE	BYX71-600R	4822 130 30866
V 0020	DIODE	BYX71-600R	4822 130 30866

7.9.4 MISCELLANEOUS

F 0001	FUSE	F 5X20 3,15A	4822 253 20025
	SOCKET,MALE		5322 265 64082

7.10 CABLE CARD STEPPING MOTOR 5322 694 14483

7.11 WINDOW CONTROL CARD 5322 694 14332

7.11.1 CAPACITORS

C 0001	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0002	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0003	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0004	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0005	CAPACITOR,FOIL	100V 10%	100NF	5322 121 40323
C 0006	CAPACITOR,CERAM	2%	100PF	4822 122 31081
C 0007	CAPACITOR,CERAM	2%	100PF	4822 122 31081
C 0008	CAPACITOR,CERAM	2%	100PF	4822 122 31081
C 0009	CAPACITOR,CERAM	2%	100PF	4822 122 31081
C 0010	CAPACITOR,CERAM	2%	100PF	4822 122 31081
C 0011	CAPACITOR,CERAM	2%	100PF	4822 122 31081

7.11.2 INTEGRATED CIRCUITS

D 0001	INTEGR.CIRCUIT	UA741CN	4822 209 80617
D 0002	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0003	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0004	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0005	INTEGR.CIRCUIT	UA741CN	4822 209 80617
D 0006	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0007	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0008	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0009	INTEGR.CIRCUIT	UA741CN	4822 209 80617
D 0010	INTEGR.CIRCUIT	UA741CN	4822 209 80617
D 0011	INTEGR.CIRCUIT	UA741CN	4822 209 80617
D 0012	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0013	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0014	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0015	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0016	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0017	INTEGR.CIRCUIT	SD5000N	5322 209 85748

Item	Description	Ordering Code
D 0018	INTEGR.CIRCUIT SD5000N	5322 209 85748
D 0019	INTEGR.CIRCUIT HEF4556BD	4822 209 10281
D 0020	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0021	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0022	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0023	INTEGR.CIRCUIT HEF4539BD	4822 209 10313
D 0024	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0025	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0026	INTEGR.CIRCUIT HEF4539BD	4822 209 10313
D 0027	INTEGR.CIRCUIT HEF40192BD	4822 209 10285
D 0028	INTEGR.CIRCUIT HEF4011BD	4822 209 10247
D 0029	INTEGR.CIRCUIT HEF4049BD	4822 209 10306
D 0030	INTEGR.CIRCUIT HEF4518BD	4822 209 10275
D 0031	INTEGR.CIRCUIT HEF4049BD	4822 209 10306
D 0032	INTEGR.CIRCUIT HEF4027BD	4822 209 10255
D 0033	INTEGR.CIRCUIT HEF4556BD	4822 209 10281
D 0034	INTEGR.CIRCUIT HEF4011BD	4822 209 10247
D 0035	INTEGR.CIRCUIT HEF4049BD	4822 209 10306

7.11.3 RESISTORS

R 0001	POTM,TRIMMING	0,75W	10%	1K	5322 103 10023
R 0002	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0003	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0004	RESISTOR,M.FILM	MR25	1%	2K05	5322 116 50664
R 0006	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0007	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0008	RESISTOR,M.FILM	MR25	1%	5K11	5322 116 54595
R 0009	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0011	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0012	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0013	RESISTOR,M.FILM	MR24E	0.1%	5K11	5322 116 54792
R 0014	RESISTOR,M.FILM	MR24E	0.1%	10K	5322 116 50748
R 0016	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0017	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0018	RESISTOR,M.FILM	MR24E	0.1%	5K11	5322 116 54792
R 0019	RESISTOR,M.FILM	MR24E	0.1%	1K	5322 116 50747
R 0020	POTM,TRIMMING	0,75W	10%	10K	5322 103 14026
R 0021	RESISTOR,M.FILM	MR24E	0.1%	1K	5322 116 50747
R 0022	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0024	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0025	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0026	RESISTOR,M.FILM	MR24E	0.1%	5K11	5322 116 54792
R 0027	RESISTOR,M.FILM	MR24E	0.1%	10K	5322 116 50748
R 0029	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0030	RESISTOR,M.FILM	MR25	1%	100K	4822 116 51268
R 0031	RESISTOR,M.FILM	MR24E	0.1%	5K11	5322 116 54792
R 0032	RESISTOR,M.FILM	MR24E	0.1%	1K	5322 116 50747

Item	Description	Ordering Code
R 0033	POTM,TRIMMING 1W 10% 2K	5322 103 10135
R 0034	RESISTOR,M.FILM MR24E 0.1% 1K	5322 116 50747
R 0035	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0036	POTM,TRIMMING 0,75W 10% 10K	5322 103 14026
R 0037	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0038	RESISTOR,M.FILM MR24E 0.1% 10K	5322 116 50748
R 0039	RESISTOR,M.FILM MR24E 0.1% 10K	5322 116 50748
R 0040	RESISTOR,M.FILM MR24E 0.1% 10K	5322 116 50748
R 0041	POTM,TRIMMING 0,75W 10% 10K	5322 103 14026
R 0042	RESISTOR,M.FILM MR25 1% 9K09	4822 116 51284
R 0043	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0044	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0045	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0046	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0048	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0049	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0050	RESISTOR,M.FILM MR25 1% 102K	5322 116 54697
R 0051	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0052	RESISTOR,M.FILM MR25 1% 12K4	5322 116 54626
R 0053	RESISTOR,M.FILM MR25 1% 51K1	5322 116 50672
R 0054	RESISTOR,M.FILM MR25 1% 25K5	5322 116 54649
R 0055	RESISTOR,M.FILM MR34E 0.1% 102K	5322 116 54979
R 0056	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0057	RESISTOR,M.FILM MR24E 0.1% 12K4	5322 116 55182
R 0058	RESISTOR,M.FILM MR24E 0.1% 51K1	5322 116 54284
R 0059	RESISTOR,M.FILM MR24E 0.1% 25K5	5322 116 51894
R 0060	RESISTOR,M.FILM MR34E 0.1% 102K	5322 116 54979
R 0061	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0062	RESISTOR,M.FILM MR24E 0.1% 12K4	5322 116 55182
R 0063	RESISTOR,M.FILM MR24E 0.1% 51K1	5322 116 54284
R 0064	RESISTOR,M.FILM MR24E 0.1% 25K5	5322 116 51894
R 0065	RESISTOR,M.FILM MR34E 0.1% 102K	5322 116 54979
R 0066	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0067	RESISTOR,M.FILM MR24E 0.1% 12K4	5322 116 55182
R 0068	RESISTOR,M.FILM MR24E 0.1% 51K1	5322 116 54284
R 0069	RESISTOR,M.FILM MR24E 0.1% 25K5	5322 116 51894
R 0070	RESISTOR,M.FILM MR34E 0.1% 102K	5322 116 54979
R 0071	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0072	RESISTOR,M.FILM MR24E 0.1% 12K4	5322 116 55182
R 0073	RESISTOR,M.FILM MR24E 0.1% 51K1	5322 116 54284
R 0074	RESISTOR,M.FILM MR24E 0.1% 25K5	5322 116 51894
R 0075	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0076	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0077	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0078	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0079	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0080	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0081	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0082	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0083	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0084	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0085	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0086	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0087	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0088	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0089	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0090	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235

Item	Description		Ordering Code
V 0001	DIODE,REFERENCE	BZV14	5322 130 34568
V 0002	TRANSISTOR	BCY56	5322 130 40325
V 0003	TRANSISTOR	BCY56	5322 130 40325
V 0005	TRANSISTOR	BSX20	4822 130 41705
V 0006	TRANSISTOR	BSX20	4822 130 41705
V 0007	TRANSISTOR	BSX20	4822 130 41705

7.11.5 MISCELLANEOUS

SOCKET,MALE 5322 265 64082

7.12 AMPLIFIER ANALYSER CARD

5322 694 14331

7.12.1 CAPACITORS

C 0001	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0002	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0003	CAPACITOR,CERAM	0.25PF	8.2PF	4822 122 31052
C 0004	CAPACITOR,FOIL	100V 10%	1UF	5322 121 40197
C 0005	CAPACITOR,FOIL	100V 10%	1UF	5322 121 40197
C 0006	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0007	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0008	CAPACITOR,CERAM	0.25PF	4.7PF	4822 122 31045
C 0009	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0010	CAP,ELECTROLYT.	-10+50%	68UF	4822 124 20689
C 0011	CAPACITOR,CERAM	2%	15PF	4822 122 31058
C 0012	CAPACITOR,CERAM	10%	4,7NF	4822 122 30128
C 0013	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0014	CAPACITOR,FOIL	63V 1%	10NF	5322 121 54154
C 0015	CAPACITOR,FOIL	63V 1%	10NF	5322 121 54154
C 0016	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0017	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0018	CAPACITOR,CERAM	2%	82PF	4822 122 31237
C 0019	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0020	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0021	CAPACITOR,CERAM	2%	47PF	4822 122 31072
C 0022	CAPACITOR,CERAM	0.25PF	6.8PF	4822 122 31049
C 0023	CAPACITOR,CERAM	2%	82PF	4822 122 31237
C 0024	CAPACITOR,CERAM	10%	220PF	4822 122 30094
C 0025	CAPACITOR,CERAM	2%	33PF	4822 122 31067
C 0026	CAPACITOR,CERAM	2%	47PF	4822 122 31072
C 0027	CAPACITOR,CERAM	0.25PF	8.2PF	4822 122 31052
C 0028	CAPACITOR,CERAM	0.25PF	8.2PF	4822 122 31052
C 0029	CAP,ELECTROLYT.	-10+50%	68UF	4822 124 20689
C 0030	CAPACITOR,CERAM	2%	47PF	4822 122 31072
C 0031	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0032	CAPACITOR,CERAM	2%	47PF	4822 122 31072

Item	Description			Ordering Code
C 0033	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0034	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0035	CAP,ELECTROLYT.	-10+50%	150UF	4822 124 20586
C 0036	CAP,ELECTROLYT.	-10+50%	150UF	4822 124 20586
C 0037	CAP,ELECTROLYT.	-10+50%	68UF	4822 124 20689
C 0038	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0039	CAP,ELECTROLYT.	-10+50%	68UF	4822 124 20689
C 0040	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0041	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0042	CAPACITOR,CERAM	2%	33PF	4822 122 31067
C 0043	CAPACITOR,CERAM	2%	33PF	4822 122 31067
C 0044	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0045	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0046	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0047	CAP,ELECTROLYT.	-10+50%	47UF	4822 124 20678
C 0048	CAP,ELECTROLYT.	-10+50%	47UF	4822 124 20678
C 0049	CAP,ELECTROLYT.	-10+50%	68UF	4822 124 20689
C 0050	CAP,ELECTROLYT.	-10+50%	33UF	4822 124 20688
C 0051	CAPACITOR,CERAM	2%	120PF	4822 122 31348
C 0052	CAPACITOR,CERAM	2%	120PF	4822 122 31348
C 0053	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0054	CAP,ELECTROLYT.	-10+50%	47UF	4822 124 20678

7.12.2 INTEGRATED CIRCUITS

D 0001	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 0002	INTEGR.CIRCUIT	SN74LS123N-00	5322 209 85266
D 0003	INTEGR.CIRCUIT	N7406N	5322 209 86327
D 0004	INTEGR.CIRCUIT	N74LS132N	5322 209 85201
D 0005	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 0006	INTEGR.CIRCUIT	SN74LS123N-00	5322 209 85266
D 0007	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 0008	INTEGR.CIRCUIT	N74LS90N	5322 209 85255
D 0009	INTEGR.CIRCUIT	SN74LS123N-00	5322 209 85266
D 0010	INTEGR.CIRCUIT	NE521N	5322 209 14441
D 0011	INTEGR.CIRCUIT	NE521N	5322 209 14441
D 0012	INTEGR.CIRCUIT	N74LS00N	5322 209 84823
D 0013	INTEGR.CIRCUIT	N74LS10N	5322 209 84996
D 0014	INTEGR.CIRCUIT	SN74LS123N-00	5322 209 85266
D 0015	INTEGR.CIRCUIT	N74LS132N	5322 209 85201
D 0016	INTEGR.CIRCUIT	LM324N	4822 209 80587
D 0017	INTEGR.CIRCUIT	NE521N	5322 209 14441
D 0018	INTEGR.CIRCUIT	NE521N	5322 209 14441
D 0019	INTEGR.CIRCUIT	SD5000N	5322 209 85748
D 0020	INTEGR.CIRCUIT	HEF4081BD	4822 209 10269
D 0021	INTEGR.CIRCUIT	UA710HC	5322 209 86414
D 0022	INTEGR.CIRCUIT	NE536H	5322 209 86201
D 0023	INTEGR.CIRCUIT	LM324N	4822 209 80587
D 0025	INTEGR.CIRCUIT	LM308AN	5322 209 86056
D 0026	INTEGR.CIRCUIT	LM308AN	5322 209 86056

7.12.3 RESISTORS

Item	Description	Ordering Code
R 0001	RESISTOR,M.FILM MR25 1% 4K42	5322 116 50556
R 0002	RESISTOR,M.FILM MR25 1% 7K5	5322 116 54608
R 0003	RESISTOR,M.FILM MR25 1% 6K49	5322 116 54603
R 0004	RESISTOR,M.FILM MR25 1% 4K02	5322 116 55448
R 0005	RESISTOR,M.FILM MR25 1% 162E	5322 116 50417
R 0006	RESISTOR,M.FILM MR25 1% 162E	5322 116 50417
R 0007	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0008	RESISTOR,M.FILM MR25 1% 4K22	5322 116 50729
R 0009	RESISTOR,SAFETY MR25 1% 7K87	5322 116 50458
R 0010	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0011	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0012	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0013	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0014	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0015	RESISTOR,M.FILM MR25 1% 825E	5322 116 54541
R 0016	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0017	RESISTOR,M.FILM MR25 1% 19K6	5322 116 54641
R 0018	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0019	RESISTOR,M.FILM MR25 1% 3K48	5322 116 55367
R 0020	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0021	RESISTOR,M.FILM MR25 1% 348E	5322 116 54515
R 0022	RESISTOR,M.FILM MR25 1% 7K5	5322 116 54608
R 0023	RESISTOR,M.FILM MR25 1% 3K16	5322 116 50579
R 0024	RESISTOR,M.FILM MR25 1% 19K6	5322 116 54641
R 0025	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0026	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0027	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0028	RESISTOR,M.FILM MR25 1% 261E	5322 116 54502
R 0029	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0030	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0031	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0032	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0033	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0034	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0035	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0036	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0037	RESISTOR,M.FILM MR25 1% 11K	5322 116 54623
R 0038	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0039	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0040	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0041	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0042	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0043	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0044	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0045	RESISTOR,M.FILM MR25 1% 2K74	5322 116 50636
R 0046	RESISTOR,M.FILM MR25 1% 1K96	5322 116 54571
R 0047	RESISTOR,M.FILM MR25 1% 4K02	5322 116 55448
R 0049	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0050	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0051	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0052	RESISTOR,M.FILM MR25 1% 30K1	5322 116 54655
R 0053	POTM,TRIMMING 1W 10% 20K	5322 101 10516
R 0054	RESISTOR,M.FILM MR25 1% 1K4	5322 116 54562
R 0055	RESISTOR,M.FILM MR25 1% 115E	5322 116 54476
R 0056	RESISTOR,M.FILM MR25 1% 115E	5322 116 54476
R 0057	RESISTOR,M.FILM MR25 1% 383E	5322 116 55368
R 0058	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0059	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253

Item	Description	Ordering Code
R 0060	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0061	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0062	RESISTOR,M.FILM MR25 1% 649E	5322 116 54532
R 0063	RESISTOR,M.FILM MR25 1% 261E	5322 116 54502
R 0064	RESISTOR,M.FILM MR25 1% 261E	5322 116 54502
R 0065	RESISTOR,M.FILM MR30 1% 1M	4822 116 51279
R 0066	RESISTOR,M.FILM MR30 1% 1M	4822 116 51279
R 0067	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0068	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0069	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0070	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0071	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0072	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0073	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0074	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0075	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0076	RESISTOR,M.FILM MR25 1% 4K22	5322 116 50729
R 0077	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0078	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0079	RESISTOR,M.FILM MR25 1% 40K2	5322 116 54665
R 0080	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0081	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0082	RESISTOR,M.FILM MR25 1% 40K2	5322 116 54665
R 0083	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0084	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0085	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0086	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0087	RESISTOR,M.FILM MR25 1% 31K6	5322 116 54657
R 0088	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0089	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0090	RESISTOR,M.FILM MR25 1% 4K22	5322 116 50729
R 0091	RESISTOR,M.FILM MR25 1% 8K25	5322 116 54558
R 0092	RESISTOR,SAFETY MR25 1% 7K87	5322 116 50458
R 0093	RESISTOR,M.FILM MR25 1% 4K22	5322 116 50729
R 0094	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0095	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0096	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0097	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0098	RESISTOR,M.FILM MR25 1% 3K83	5322 116 54589
R 0099	RESISTOR,M.FILM MR25 1% 226E	5322 116 54497
R 0100	RESISTOR,M.FILM MR25 1% 205K	5322 116 54727

Item	Description		Ordering Code
7.12.4	SEMICONDUCTORS		
V 0001	DIODE	BAW62	4822 130 30613
V 0002	DIODE	BAW62	4822 130 30613
V 0003	DIODE	BAV45	5322 130 34037
V 0004	DIODE	BAW62	4822 130 30613
V 0005	DIODE	BAW62	4822 130 30613
V 0006	DIODE,REFERENCE	BZX79-C6V2	4822 130 34167
V 0008	DIODE,REFERENCE	BZV12	5322 130 34269
V 0009	DIODE	BAW62	4822 130 30613
V 0010	DIODE	BAW62	4822 130 30613
V 0011	DIODE	BAW62	4822 130 30613
V 0012	DIODE	BAW62	4822 130 30613
V 0013	DIODE	BAW62	4822 130 30613
V 0014	DIODE,REFERENCE	BZX79-C6V2	4822 130 34167
V 0015	DIODE	BAW62	4822 130 30613
V 0016	DIODE	BAV45	5322 130 34037
V 0017	DIODE,REFERENCE	BZX79-C6V8	4822 130 34278
V 0021	TRANSISTOR	BC547	4822 130 44257
V 0022	TRANSISTOR	BC547	4822 130 44257
V 0023	TRANSISTOR	BC547	4822 130 44257
V 0024	TRANSISTOR	BFR90A-02	5322 130 42119
V 0025	TRANSISTOR	BF324	4822 130 41448
V 0026	TRANSISTOR	BFR90A-02	5322 130 42119
V 0027	TRANSISTOR	BF199	4822 130 44154
V 0028	TRANSISTOR	BFR90A-02	5322 130 42119
V 0029	TRANSISTOR	BF324	4822 130 41448
V 0030	TRANSISTOR	BF199	4822 130 44154
V 0031	TRANSISTOR	BC547	4822 130 44257
V 0032	TRANSISTOR	BC557	4822 130 44256
V 0033	TRANSISTOR	BC557	4822 130 44256
V 0034	TRANSISTOR	BC547	4822 130 44257
V 0035	TRANSISTOR,FET	BFW13	5322 130 40516
V 0036	TRANSISTOR,FET	BFW13	5322 130 40516
V 0037	TRANSISTOR	BC557	4822 130 44256
V 0038	TRANSISTOR	BC557	4822 130 44256
7.12.5	MISCELLANEOUS		
	SOCKET,MALE		5322 265 64082
S 0001	SWITCH		5322 277 14232

Item	Description	Ordering Code
7.13	FOUR DIGIT BINARY COUNTER	5322 694 14514

7.13.1 CAPACITORS

C 0001	CAP,ELECTROLYT.	16V	20%	15UF	4822 124 20977
C 0002	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0003	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0004	CAP,ELECTROLYT.	10V	20%	33UF	4822 124 20945

7.13.2 INTEGRATED CIRCUITS

D 0001	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281
D 0002	INTEGR.CIRCUIT	HEF4081BD	4822 209 10269
D 0003	INTEGR.CIRCUIT	HEF4071BD	4822 209 10307
D 0004	INTEGR.CIRCUIT	HEF4001BD	4822 209 10246
D 0005	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281
D 0006	INTEGR.CIRCUIT	HEF4013BD	4822 209 10248
D 0007	INTEGR.CIRCUIT	HEF4520BD	4822 209 10276
D 0008	INTEGR.CIRCUIT	HEF4520BD	4822 209 10276
D 0009	INTEGR.CIRCUIT	HEF4104BD	4822 209 10273
D 0010	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0011	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0012	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0013	INTEGR.CIRCUIT	N74LS107N	5322 209 85816
D 0014	INTEGR.CIRCUIT	HEF4049BD	4822 209 10306

7.13.3 RESISTORS

R 0001	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0002	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253

7.13.4 SEMICONDUCTORS

V 0001	DIODE,REFERENCE	BZX79-C6V8	4822 130 34278

7.13.5 MISCELLANEOUS

	SOCKET,MALE	5322 265 64082

Item	Description				Ordering Code
7.14	**RATEMETER**				5322 694 14333
7.14.1	CAPACITORS				
C 0001	CAPACITOR,CERAM		2%	120PF	4822 122 31348
C 0002	CAPACITOR,FOIL	630V	1%	100PF	4822 121 50562
C 0003	CAPACITOR,FOIL	250V	1%	820PF	5322 121 54072
C 0004	CAPACITOR,CERAM		-20+80%	22NF	4822 122 30103
C 0005	CAPACITOR,FOIL	400V	10%	33NF	5322 121 44025
C 0007	CAP,ELECTROLYT.		-10+50%	100UF	4822 124 20679
C 0008	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0009	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0010	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0011	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0012	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0013	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0014	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0015	CAPACITOR,CERAM		2%	12PF	4822 122 31056
C 0016	CAPACITOR,FOIL	100V	10%	1UF	5322 121 40197
C 0017	CAPACITOR,FOIL	100V	10%	680NF	5322 121 40233
C 0018	CAPACITOR,FOIL	100V	10%	1UF	5322 121 40197
C 0019	CAPACITOR,FOIL	100V	10%	330NF	4822 121 40257
C 0020	CAPACITOR,FOIL	100V	10%	150NF	4822 121 40231
C 0021	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0022	CAPACITOR,FOIL	400V	10%	33NF	5322 121 44025
C 0023	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0024	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0025	CAP,ELECTROLYT.		-10+50%	68UF	4822 124 20689
C 0026	CAP,ELECTROLYT.		-10+50%	150UF	4822 124 20586
C 0027	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0028	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0029	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0030	CAP,ELECTROLYT.		-10+50%	68UF	4822 124 20689
C 0031	CAPACITOR,CERAM		2%	180PF	5322 122 34144
7.14.2	INTEGRATED CIRCUITS				
D 0001	INTEGR.CIRCUIT	HEF4051BD			4822 209 10262
D 0002	INTEGR.CIRCUIT	HEF4071BD			4822 209 10307
D 0003	INTEGR.CIRCUIT	HEF4052BD			4822 209 10263
D 0004	INTEGR.CIRCUIT	HEF4052BD			4822 209 10263
D 0005	INTEGR.CIRCUIT	HEF4556BD			4822 209 10281
D 0006	INTEGR.CIRCUIT	HEF4042BD			4822 209 10258
D 0007	INTEGR.CIRCUIT	HEF4027BD			4822 209 10255
D 0008	INTEGR.CIRCUIT	HEF4029BD			4822 209 10302
D 0009	INTEGR.CIRCUIT	HEF4555BD			4822 209 10279
D 0010	INTEGR.CIRCUIT	HEF4049BD			4822 209 10306
D 0011	INTEGR.CIRCUIT	HEF4081BD			4822 209 10269
D 0012	INTEGR.CIRCUIT	HEF4001BD			4822 209 10246
D 0013	INTEGR.CIRCUIT	HEF4001BD			4822 209 10246
D 0014	INTEGR.CIRCUIT	HEF4528BD			4822 209 10277
D 0015	INTEGR.CIRCUIT	HEF4085BD			4822 209 10272
D 0016	INTEGR.CIRCUIT	HEF4518BD			4822 209 10275
D 0017	INTEGR.CIRCUIT	N74LS26N			5322 209 85832
D 0018	INTEGR.CIRCUIT	N74LS90N			5322 209 85255
D 0019	INTEGR.CIRCUIT	LM324N			4822 209 80587
D 0020	INTEGR.CIRCUIT	SN74LS123N-00			5322 209 85266
D 0021	INTEGR.CIRCUIT	NE536H			5322 209 86201

Item	Description	Ordering Code
7.14.3	RESISTORS	
R 0002	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0003	RESISTOR,M.FILM MR25 1% 2K61	5322 116 50671
R 0004	RESISTOR,M.FILM MR25 1% 3K48	5322 116 55367
R 0005	RESISTOR,M.FILM MR25 1% 3K48	5322 116 55367
R 0006	RESISTOR,M.FILM MR25 1% 215E	5322 116 55274
R 0009	RESISTOR,M.FILM MR25 1% 30E1	5322 116 50904
R 0010	RESISTOR,M.FILM CR25 5% 1M	4822 110 73187
R 0011	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0012	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0013	RESISTOR,M.FILM MR30 1% 1M	4822 116 51279
R 0014	RESISTOR,M.FILM MR30 1% 1M	4822 116 51279
R 0015	RESISTOR,M.FILM MR30 1% 1M	4822 116 51279
R 0016	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0017	POTM,TRIMMING 0.05W 20% 10K	4822 100 10035
R 0018	RESISTOR,M.FILM MR25 1% 5K11	5322 116 54595
R 0019	RESISTOR,M.FILM MR25 1% 82K5	5322 116 55374
R 0021	RESISTOR,M.FILM MR25 1% 7K5	5322 116 54608
R 0023	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0024	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0025	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0026	RESISTOR,M.FILM MR25 1% 1K47	5322 116 50635
R 0027	RESISTOR,M.FILM MR25 1% 147E	5322 116 50766
R 0028	RESISTOR,M.FILM MR25 1% 226K	5322 116 54729
R 0029	RESISTOR,M.FILM MR25 1% 226K	5322 116 54729
R 0030	RESISTOR,M.FILM MR25 1% 21K5	5322 116 50451
R 0031	RESISTOR,M.FILM MR25 1% 21K5	5322 116 50451
R 0032	RESISTOR,M.FILM MR25 1% 21K5	5322 116 50451
R 0033	RESISTOR,M.FILM MR25 1% 21K5	5322 116 50451
R 0034	RESISTOR,HT VR25 10% 15M	4822 116 60142
R 0035	RESISTOR,M.FILM MR25 1% 750E	4822 116 51234
R 0036	RESISTOR,M.FILM MR25 1% 4K22	5322 116 50729
R 0037	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0038	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0039	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0040	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0041	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0042	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0043	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0044	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0045	RESISTOR,M.FILM MR25 1% 511K	5322 116 55258
R 0046	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0047	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0048	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0049	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0050	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0051	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0052	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0053	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0054	RESISTOR,M.FILM MR25 1% 12K1	5322 116 50572
R 0055	RESISTOR,M.FILM MR25 1% 5K62	4822 116 51281
R 0056	RESISTOR,M.FILM MR25 1% 1K78	5322 116 50515
R 0057	RESISTOR,M.FILM MR25 1% 23K7	5322 116 54646
R 0058	RESISTOR,M.FILM MR25 1% 1M	5322 116 55535
R 0059	RESISTOR,HT VR25 5% 10M	4822 110 72214
R 0060	RESISTOR,M.FILM MR25 1% 5K62	4822 116 51281
R 0061	RESISTOR,M.FILM MR25 1% 1K78	5322 116 50515
R 0062	RESISTOR,M.FILM MR25 1% 23K7	5322 116 54646
R 0063	RESISTOR,M.FILM MR25 1% 1M	5322 116 55535
R 0064	RESISTOR,HT VR25 5% 10M	4822 110 72214
R 0065	RESISTOR,M.FILM MR25 1% 5K62	4822 116 51281

Item	Description				Ordering Code
R 0066	RESISTOR,M.FILM	MR25	1%	1K78	5322 116 50515
R 0067	RESISTOR,M.FILM	MR25	1%	23K7	5322 116 54646
R 0068	RESISTOR,M.FILM	MR25	1%	1M	5322 116 55535
R 0069	RESISTOR,HT	VR25	5%	10M	4822 110 72214
R 0070	RESISTOR,M.FILM	MR25	1%	5K62	4822 116 51281
R 0071	RESISTOR,M.FILM	MR25	1%	1K78	5322 116 50515
R 0072	RESISTOR,M.FILM	MR25	1%	23K7	5322 116 54646
R 0073	RESISTOR,M.FILM	MR25	1%	1M	5322 116 55535
R 0074	RESISTOR,HT	VR25	5%	10M	4822 110 72214
R 0075	RESISTOR,M.FILM	MR25	1%	5K62	4822 116 51281
R 0076	RESISTOR,M.FILM	MR25	1%	1K78	5322 116 50515
R 0077	RESISTOR,M.FILM	MR25	1%	23K7	5322 116 54646
R 0078	RESISTOR,M.FILM	MR25	1%	1M	5322 116 55535
R 0079	RESISTOR,HT	VR25	5%	10M	4822 110 72214
R 0080	RESISTOR,M.FILM	MR25	1%	5K62	4822 116 51281
R 0081	RESISTOR,M.FILM	MR25	1%	1K78	5322 116 50515
R 0082	RESISTOR,M.FILM	MR25	1%	23K7	5322 116 54646
R 0083	RESISTOR,M.FILM	MR25	1%	1M	5322 116 55535
R 0084	RESISTOR,HT	VR25	5%	10M	4822 110 72214
R 0085	RESISTOR,M.FILM	MR25	1%	4E64	5322 116 51359
R 0086	RESISTOR,M.FILM	MR25	1%	2E26	5322 116 51835
R 0087	RESISTOR,M.FILM	CR25	5%	4E7	4822 110 73045
R 0088	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0089	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0090	RESISTOR,M.FILM	MR25	1%	3K48	5322 116 55367
R 0091	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0092	RESISTOR,HT	CR25	10%	3M9	4822 110 72203
R 0093	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235

7.14.4 SEMICONDUCTORS

Item	Description		Ordering Code
V 0001	TRANSISTOR	2N2907	5322 130 40218
V 0002	TRANSISTOR,FET	BSV78	5322 130 44093
V 0003	DIODE	BAW62	4822 130 30613
V 0004	DIODE	BAW62	4822 130 30613
V 0005	TRANSISTOR	BC557	4822 130 44256
V 0006	DIODE	BAW62	4822 130 30613
V 0007	TRANSISTOR	BC547	4822 130 44257
V 0008	TRANSISTOR	BC547	4822 130 44257
V 0009	DIODE,REFERENCE	BZX75-C2V1	4822 130 34049
V 0010	DIODE,REFERENCE	BZX79-C6V2	4822 130 34167
V 0011	DIODE	BAW62	4822 130 30613
V 0012	DIODE	BAW62	4822 130 30613
V 0013	DIODE	BAW62	4822 130 30613
V 0014	DIODE	BAW62	4822 130 30613
V 0015	DIODE	BAW62	4822 130 30613
V 0016	DIODE	BAW62	4822 130 30613
V 0017	TRANSISTOR	BC547	4822 130 44257
V 0018	TRANSISTOR	BC557	4822 130 44256
V 0019	TRANSISTOR	BC557	4822 130 44256
V 0020	TRANSISTOR	BC557	4822 130 44256
V 0021	TRANSISTOR	BC557	4822 130 44256
V 0022	TRANSISTOR	BC557	4822 130 44256
V 0023	TRANSISTOR	BC557	4822 130 44256
V 0024	DIODE	BAW62	4822 130 30613
V 0025	DIODE	BAW62	4822 130 30613
V 0026	DIODE	BAW62	4822 130 30613
V 0027	DIODE	BAW62	4822 130 30613
V 0028	DIODE	BAW62	4822 130 30613
V 0029	DIODE	BAW62	4822 130 30613
V 0030	DIODE	BAW62	4822 130 30613
V 0031	DIODE	BAW62	4822 130 30613
V 0032	DIODE	BAW62	4822 130 30613
V 0033	DIODE	BAW62	4822 130 30613
V 0034	DIODE	BAW62	4822 130 30613
V 0035	TRANSISTOR,FET	BSV79	5322 130 44017
V 0036	TRANSISTOR,FET	BSV79	5322 130 44017
V 0037	TRANSISTOR,FET	BSV79	5322 130 44017
V 0038	TRANSISTOR,FET	BSV79	5322 130 44017
V 0039	TRANSISTOR,FET	BSV79	5322 130 44017
V 0040	TRANSISTOR,FET	BSV79	5322 130 44017
V 0041	DIODE	BAW62	4822 130 30613
V 0042	DIODE	BAW62	4822 130 30613
V 0043	DIODE	BAW62	4822 130 30613
V 0044	DIODE	BAW62	4822 130 30613
V 0045	DIODE	BAW62	4822 130 30613
V 0046	DIODE	BAW62	4822 130 30613

7.14.5 MISCELLANEOUS

	SOCKET,MALE		5322 265 64082

Item	Description	Ordering Code

7.15 CABLE CARD "DETECTOR" 5322 694 14481

7.15.1 CAPACITORS

Item	Description	Ordering Code
C 0001	CAPACITOR,CERAM -20+80% 22NF	4822 122 30103

7.15.2 RESISTORS

Item	Description	Ordering Code
R 0001	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0002	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0003	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0004	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549

7.15.3 MISCELLANEOUS

Item	Description	Ordering Code
	SOCKET,MALE	5322 265 64094
	CONNECTOR	5322 267 54187

7.16 HV 2000 CARD

Ordering Code: 5322 694 14511

7.16.1 CAPACITORS

Item	Description				Ordering Code
C 0001	CAPACITOR,CERAM		10%	1.8NF	4822 122 30048
C 0002	CAPACITOR,FOIL	100V	10%	100NF	5322 121 40323
C 0003	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0004	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0005	CAPACITOR,CERAM		-20+80%	22NF	4822 122 30103
C 0006	CAP,ELECTROLYT.		-20+20%	10UF	5322 124 24089
C 0007	CAPACITOR	1000V	5%	68NF	5322 121 41896
C 0008	CAPACITOR,FOIL	1500V	5%	33NF	4822 121 40542
C 0009	CAPACITOR	1500V	5%	68NF	5322 121 41897
C 0010	CAPACITOR	1500V	5%	68NF	5322 121 41897
C 0011	CAPACITOR	1500V	5%	68NF	5322 121 41897
C 0012	CAPACITOR	1500V	5%	68NF	5322 121 41897
C 0013	CAPACITOR,CERAM		2%	100PF	4822 122 31316
C 0014	CAPACITOR,CERAM		-20+80%	2.2NF	4822 122 30114
C 0015	CAPACITOR,CERAM		-20+50%	10NF	4822 122 31414
C 0016	CAP,ELECTROLYT.		-20+20%	10UF	5322 124 24089
C 0017	CAPACITOR,CERAM		-20+50%	10NF	4822 122 31414
C 0018	CAPACITOR,CERAM		-20+80%	22NF	4822 122 30103
C 0019	CAPACITOR,CERAM		10%	1NF	4822 122 30027
C 0020	CAPACITOR,FOIL	100V	10%	470NF	5322 121 40175
C 0021	CAPACITOR,PAPER	250V	10%	47NF	5322 121 44138
C 0022	CAPACITOR,CERAM		-20+50%	10NF	4822 122 31414
C 0023	CAPACITOR,CERAM		-20+50%	10NF	4822 122 31414
C 0024	CAPACITOR,CERAM		-20+80%	22NF	4822 122 30103
C 0025	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0026	CAPACITOR,FOIL	100V	10%	220NF	4822 121 40232
C 0027	CAPACITOR,CERAM		-20+80%	1NF	4822 122 30027
C 0028	CAP,ELECTROLYT.		-20+20%	10UF	5322 124 24094

7.16.2 RESISTORS

Item	Description				Ordering Code
R 0001	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0002	POTM,TRIMMING	0.05W	20%	2K2	4822 100 10029
R 0003	RESISTOR,M.FILM	MR25	1%	909E	5322 116 55278
R 0004	RESISTOR,M.FILM	MR25	1%	100E	5322 116 55549
R 0005	RESISTOR,M.FILM	MR25	1%	100E	5322 116 55549
R 0006	RESISTOR,M.FILM	MR25	1%	402E	5322 116 54519
R 0007	RESISTOR,M.FILM	MR25	1%	100E	5322 116 55549
R 0008	RESISTOR,M.FILM	MR25	1%	402E	5322 116 54519
R 0009	RESISTOR,M.FILM	MR25	1%	1K	4822 116 51235
R 0010	RESISTOR,M.FILM	CR25	5%	1E	4822 110 73027
R 0011	RESISTOR,HT	VR37	5%	15M	4822 110 42218
R 0012	RESISTOR,CARBON	CR37	5%	100K	4822 110 53161
R 0013	RESISTOR.WW.	4W	5%	1K5	4822 112 21112
R 0015	RESISTOR,M.FILM	2W	1%	70M	5322 116 54998
R 0016	RESISTOR,M.FILM		0.1%	174K	5322 116 51891
R 0017	RESISTOR,M.FILM	MR25	1%	174K	5322 116 54719
R 0018	RESISTOR,M.FILM	MR25	1%	10E	5322 116 50452
R 0019	RESISTOR,M.FILM	MR25	1%	174K	5322 116 54719
R 0020	RESISTOR,M.FILM	MR25	1%	10K	4822 116 51253
R 0021	RESISTOR,M.FILM	MR25	1%	226E	5322 116 54497
R 0022	RESISTOR,M.FILM	MR25	1%	464E	5322 116 50536
R 0023	POTM,TRIMMING	0.05W	20%	1K	4822 100 10037
R 0024	RESISTOR,HT	VR37	5%	22M	4822 110 42223

Item	Description	Ordering Code
R 0025	RESISTOR,M.FILM MR25 1% 82K5	5322 116 55374
R 0026	POTM,TRIMMING 0.05W 20% 100K	4822 100 10052
R 0027	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0028	RESISTOR,M.FILM MR25 1% 1M	5322 116 55535
R 0029	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0030	RESISTOR,M.FILM MR25 1% 1M	5322 116 55535
R 0031	RESISTOR,M.FILM MR25 1% 48K7	5322 116 50442
R 0032	RESISTOR,M.FILM MR24E 0.1% 10K	5322 116 50748
R 0033	RESISTOR,M.FILM MR24E 0.1% 32K4	5322 116 51896
R 0034	RESISTOR,M.FILM MR25 1% 261E	5322 116 54502
R 0035	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0036	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0037	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0038	RESISTOR,M.FILM MR25 1% 16K2	5322 116 55361
R 0039	RESISTOR,M.FILM MR25 1% 12K4	5322 116 54626
R 0040	RESISTOR,M.FILM MR25 1% 121E	5322 116 54426
R 0041	RESISTOR,M.FILM MR25 1% 10E	5322 116 50452
R 0042	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253

7.16.3 SEMICONDUCTORS

V 0001	TRANSISTOR	BC547	4822 130 44257
V 0002	TRANSISTOR	BC557	4822 130 44256
V 0003	TRANSISTOR	BC547	4822 130 44257
V 0004	TRANSISTOR	BC557	4822 130 44256
V 0005	TRANSISTOR	BSW68A	5322 130 44788
V 0006	TRANSISTOR	BSW68A	5322 130 44788
V 0007	TRANSISTOR	BD438	4822 130 40995
V 0008	TRANSISTOR	BC547	4822 130 44257
V 0009	TRANSISTOR	BC557	4822 130 44256
V 0010	TRANSISTOR	BC547	4822 130 44257
V 0011	TRANSISTOR	BC557	4822 130 44256
V 0015	DIODE	BY509	4822 130 41485
V 0016	DIODE	BY509	4822 130 41485
V 0017	DIODE	BY509	4822 130 41485
V 0018	DIODE	BY509	4822 130 41485
V 0019	DIODE	BAW62	4822 130 30613
V 0020	DIODE	BAW62	4822 130 30613
V 0021	DIODE	BAW62	4822 130 30613
V 0022	DIODE,REFERENCE	BZX79-C3V6	5322 130 34834
V 0023	DIODE,REFERENCE	BZX79-C10	4822 130 34297
V 0024	DIODE	BAW62	4822 130 30613
V 0025	DIODE,REFERENCE	1N827	5322 130 34336
V 0026	DIODE,REFERENCE	BZX79-C5V6	4822 130 34173

7.16.4 MISCELLANEOUS

LA0001	LAMP,NEON	GL2 0.5MA	4822 134 20128
	SOCKET,MALE	PW CON DIPSOLD	5322 265 64094
	BIT,SOLDERING	SOLDEERPEN	5322 290 34123
	PLUG,COAX MALE	PENCONTACTDOOS	5322 264 14023

7.16.5 INTEGRATED CIRCUITS

D 0001	INTEGR.CIRCUIT	NE555N	4822 209 80775
D 0002	INTEGR.CIRCUIT	HEF4017BD	4822 209 10297
D 0003	INTEGR.CIRCUIT	LM208H	5322 209 85475
D 0004	INTEGR.CIRCUIT	LM208H	5322 209 85475

Item	Description	Ordering Code
7.17	**RECORDER CONTROL CARD**	**5322 694 14477**
7.17.1	CAPACITORS	
C 0001	-20+50% 1NF	4822 122 30027
C 0002	-20+50% 1NF	4822 122 30027
C 0003	-20+50% 1NF	4822 122 30027
C 0004	16V 20% 15UF	4822 124 20977
C 0005	10V 20% 33UF	4822 124 20945
C 0006	16V 20% 15UF	4822 124 20977
C 0007	-20+80% 22NF	4822 122 30103
C 0008	-20+80% 22NF	4822 122 30103
C 0009	-20+80% 22NF	4822 122 30103
C 0010	-20+80% 22NF	4822 122 30103
C 0011	-20+80% 22NF	4822 122 30103
C 0012	-20+80% 22NF	4822 122 30103
C 0013	-20+80% 22NF	4822 122 30103
C 0014	2% 120PF	4822 122 30093
C 0015	2% 56PF	4822 122 31521
C 0016	2% 56PF	4822 122 31521
C 0017	-20+50% 1NF	4822 122 30027
7.17.2	INTEGRATED CIRCUITS	
D 0001	P8251A	5322 209 85847
D 0002	HEF40175BD	4822 209 10284
D 0003	HEF40097BD	4822 209 10317
D 0004	HEF40097BD	4822 209 10317
D 0005	HEF4104BD	4822 209 10273
D 0006	SN74LS373N-00	5322 209 86062
D 0007	N8T16N	5322 209 85831
D 0008	N8T15N	5322 209 85829
D 0009	HEF4050BD	4822 209 10261
D 0010	HEF4556BD	4822 209 10281
D 0011	HEF4104BD	4822 209 10273
D 0012	HEF4050BD	4822 209 10261
D 0013	HEF4049BD	4822 209 10306
D 0014	HEF4071BD	4822 209 10307
D 0015	N74LS42N	4822 209 50008
D 0016	HEF4049BD	4822 209 10306
D 0017	HEF40174BD	4822 209 10283
D 0018	HEF40098BD	4822 209 10282
D 0019	HEF4081BD	4822 209 10269
D 0020	HEF4050BD	4822 209 10261
D 0021	HEF4071BD	4822 209 10307
D 0022	HEF4049BD	4822 209 10306
D 0023	HEF4071BD	4822 209 10307
D 0024	HEF4051BD	4822 209 10262
D 0025	HEF4518BD	4822 209 10275
D 0026	HEF4526BD	4822 209 10289
D 0027	LM324N	4822 209 80587
D 0028	LM208H	5322 209 85475
D 0029	HEF40174BD	4822 209 10283
D 0030	HEF4013BD	4822 209 10248
D 0031	HEF4526BD	4822 209 10289
D 0032	4702BDC	5322 209 81662
D 0033	HEF4049BD	4822 209 10306

Item	Description	Ordering Code
7.17.3	RESISTORS	
R 0007	MR24E 0.1% 27K4	5322 116 51895
R 0008	MR24E 0.1% 3K16	5322 116 54788
R 0009	MR24E 0.1% 27K4	5322 116 51895
R 0010	MR24E 0.1% 3K16	5322 116 54788
R 0012	MR25 1% 10E	5322 116 50452
R 0014	MR25 1% 10E	5322 116 50452
R 0015	MR25 1% 48E7	5322 116 50511
R 0016	MR25 1% 48E7	5322 116 50511
R 0017	MR25 1% 48E7	5322 116 50511
R 0018	MR25 1% 48E7	5322 116 50511
R 0019	MR25 1% 10K	4822 116 51253
R 0020	MR25 1% 10K	4822 116 51253
R 0021	MR25 1% 10K	4822 116 51253
R 0022	MR25 1% 2K05	5322 116 50664
R 0023	MR25 1% 1K	4822 116 51235
R 0024	MR25 1% 2K05	5322 116 50664
R 0025	MR25 1% 3K65	5322 116 54587
R 0026	MR25 1% 3K01	4822 116 51246
R 0027	MR25 1% 2K05	5322 116 50664
R 0028	MR25 1% 11K5	5322 116 55358
R 0029	MR25 1% 2K05	5322 116 50664
R 0030	MR25 1% 10K	4822 116 51253
R 0031	MR25 1% 6K19	5322 116 55426
R 0032	MR25 1% 14K	5322 116 55571
R 0033	MR25 1% 10K	4822 116 51253
R 0035	MR25 1% 10K	4822 116 51253
R 0036	MR24E 0.1% 1K93	5322 116 51893
R 0037	0.1% 102E	5322 116 51889
R 0038	MR25 1% 10K	4822 116 51253
R 0039	MR25 1% 10K	4822 116 51253
R 0040	MR25 1% 4K87	5322 116 55445
R 0041	MR25 1% 10K	4822 116 51253
R 0042	MR25 1% 2K49	5322 116 50581
R 0043	MR25 1% 10K	4822 116 51253
R 0044	VR25 5% 10M	4822 110 72214
R 0045	MR25 1% 3K01	4822 116 51246
R 0046	MR25 1% 3K01	4822 116 51246
R 0047	MR24E 0.1% 107E	5322 116 51892
7.17.4	SEMICONDUCTORS	
V 0001	BAW62	4822 130 30613
V 0002	BZX79-C6V8	4822 130 34278
V 0003	BC547B	4822 130 40959
V 0004	BC547B	4822 130 40959
V 0005	BZX79-C7V5	4822 130 30861
V 0006	BZX79-C7V5	4822 130 30861
V 0007	BZX79-C7V5	4822 130 30861
V 0008	BZX79-C7V5	4822 130 30861
V 0009	BZX79-C7V5	4822 130 30861
V 0010	BZX79-C7V5	4822 130 30861
7.17.5	MISCELLANEOUS	
	PW CON DIPSOLD	5322 265 64082
	I C VOET DIL	5322 255 44047

7.18 PW1170 INTERFACE CARD 5322 694 14479

7.18.1 CAPACITORS

C 0001	CAP,ELECTROLYT.	-10+50%	47UF	5322 124 21358
C 0002	CAP,ELECTROLYT.	25V 20%	2.2UF	4822 124 21255
C 0003	CAPACITOR,FOIL	100V 10%	100NF	5322 121 40323
C 0004	CAPACITOR,CERAM	-20+50%	10NF	4822 122 31414
C 0005	CAPACITOR,CERAM	-20+50%	10NF	4822 122 31414
C 0006	CAPACITOR,CERAM	-20+50%	10NF	4822 122 31414
C 0007	CAPACITOR,CERAM	-20+50%	10NF	4822 122 31414
C 0008	CAP,ELEC.TANTAL	16V 20%	10UF	5322 124 14066
C 0009	CAP,ELEC.TANTAL	16V 20%	10UF	5322 124 14066
C 0010	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0011	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0012	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0013	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0014	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0015	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0016	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0017	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0018	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0019	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0020	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0021	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0022	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103
C 0023	CAPACITOR,CERAM	-20+80%	22NF	4822 122 30103

7.18.2 INTEGRATED CIRCUITS

D 0001	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0002	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0003	INTEGR.CIRCUIT	HEF40097BD	4822 209 10317
D 0004	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0005	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0006	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0007	INTEGR.CIRCUIT	HEF4082BD	4822 209 10271
D 0008	INTEGR.CIRCUIT	HEF4082BD	4822 209 10271
D 0009	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0010	TRANSIST,PHOTO	CNX36	5322 130 90097
D 0011	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0012	INTEGR.CIRCUIT	HEF4071BD	4822 209 10307
D 0013	INTEGR.CIRCUIT	HEF4555BD	4822 209 10279
D 0014	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281
D 0015	INTEGR.CIRCUIT	HEF4556BD	4822 209 10281
D 0016	INTEGR.CIRCUIT	HEF4071BD	4822 209 10307
D 0017	INTEGR.CIRCUIT	HEF4093BD	5322 209 14927
D 0018	INTEGR.CIRCUIT	HEF4528BD	4822 209 10277
D 0019	INTEGR.CIRCUIT	HEF4528BD	4822 209 10277
D 0020	INTEGR.CIRCUIT	HEF4075BD	4822 209 10267
D 0021	INTEGR.CIRCUIT	HEF4047BD	4822 209 10259
D 0022	INTEGR.CIRCUIT	HEF4081BD	4822 209 10269
D 0023	INTEGR.CIRCUIT	HEF4076BD	4822 209 10268
D 0024	INTEGR.CIRCUIT	HEF4040BD	4822 209 10257
D 0025	INTEGR.CIRCUIT	HEF4043BD	4822 209 10304
D 0026	INTEGR.CIRCUIT	HEF4076BD	4822 209 10268
D 0027	INTEGR.CIRCUIT	HEF40174BD	4822 209 10283
D 0028	INTEGR.CIRCUIT	HEF4049BD	4822 209 10306
D 0029	INTEGR.CIRCUIT	UA741CN	4822 209 80617

7.18.3 RESISTORS

Item	Description	Ordering Code
R 0001	RESISTOR,M.FILM MR25 1% 23K7	5322 116 54646
R 0002	RESISTOR,M.FILM MR25 1% 187E	5322 116 54494
R 0003	RESISTOR,M.FILM MR25 1% 4K87	5322 116 55445
R 0004	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0005	RESISTOR,M.FILM MR25 1% 68K1	4822 116 51266
R 0006	RESISTOR,M.FILM MR25 1% 68K1	4822 116 51266
R 0007	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0008	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0009	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0010	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0011	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0012	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0013	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0014	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0015	RESISTOR,M.FILM MR25 1% 487K	5322 116 51358
R 0016	RESISTOR,M.FILM MR25 1% 274E	5322 116 54504
R 0017	RESISTOR,M.FILM MR25 1% 274E	5322 116 54504
R 0018	RESISTOR,M.FILM MR25 1% 274E	5322 116 54504
R 0019	RESISTOR,M.FILM MR25 1% 274E	5322 116 54504
R 0020	RESISTOR,M.FILM MR25 1% 68K1	4822 116 51266
R 0021	RESISTOR,M.FILM MR25 1% 68K1	4822 116 51266
R 0022	RESISTOR,M.FILM MR25 1% 6K19	5322 116 55426
R 0023	RESISTOR,M.FILM MR25 1% 6K19	5322 116 55426
R 0024	RESISTOR,M.FILM MR25 1% 6K19	5322 116 55426
R 0025	RESISTOR,M.FILM MR25 1% 6K19	5322 116 55426
R 0026	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0027	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0028	RESISTOR,M.FILM MR25 1% 100K	4822 116 51268
R 0029	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0030	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0031	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0032	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0033	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0034	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0035	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0036	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0037	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0038	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0039	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0040	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0041	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0042	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0043	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0044	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0045	RESISTOR,M.FILM MR25 1% 1K	4822 116 51235
R 0046	RESISTOR,M.FILM MR25 1% 10K	4822 116 51253
R 0047	POTM,TRIMMING 0.05W 20% 470E	5322 101 10511
R 0048	RESISTOR,M.FILM MR25 1% 100E	5322 116 55549
R 0049	RESISTOR.WW. 7X0.2W 2% 100K	5322 111 94254

Item	Description		Ordering Code

7.18.4 SEMICONDUCTORS

Item	Description		Ordering Code
V 0001	DIODE	BZX79-C12	4822 130 34197
V 0002	DIODE	BY527	4822 130 31509
V 0003	DIODE	BAW62	4822 130 30613
V 0004	TRANSISTOR	BD140	4822 130 40824
V 0005	TRANSISTOR	BC557B	4822 130 44568
V 0006	TRANSISTOR	BC547B	4822 130 40959
V 0007	TRANSISTOR	BC547B	4822 130 40959
V 0008	TRANSISTOR	BC547B	4822 130 40959
V 0009	TRANSISTOR	BC547B	4822 130 40959
V 0010	TRIAC	BT139-600	5322 130 24079
V 0011	TRIAC	BT139-600	5322 130 24079
V 0012	TRIAC	BT139-600	5322 130 24079
V 0013	TRIAC	BT139-600	5322 130 24079
V 0014	DIODE	BAV21	4822 130 30842
V 0015	TRANSISTOR	BC557B	4822 130 44568

7.18.5 MISCELLANEOUS

Item	Description		Ordering Code
	PLUG		5322 265 64104
	PLUG		5322 267 64058
	SHAFT		5322 255 44068
F 0001	FUSE	F 5X20 315MA	5322 253 24009

7.19 CHANGER SPINNER SHUTTER CONTROL CARD 5322 694 14476

7.19.1 CAPACITORS

Item	Description		Ordering Code
C 0001	-20+80%	10NF	4822 122 30043
C 0002	100V 10%	100NF	5322 121 40323
C 0003	100V 10%	100NF	5322 121 40323
C 0004	2%	100PF	4822 122 31316
C 0005	100V 10%	100NF	5322 121 40323
C 0006	-20+80%	10NF	4822 122 30043
C 0007	-20+80%	10NF	4822 122 30043
C 0008	-20+80%	10NF	4822 122 30043
C 0009	-20+80%	10NF	4822 122 30043
C 0010	-20+80%	10NF	4822 122 30043
C 0011	-20+80%	10NF	4822 122 30043
C 0012	100V 10%	330NF	4822 121 40257
C 0013	-20+80%	10NF	4822 122 30043
C 0014	100V 10%	100NF	5322 121 40323
C 0015	100V 10%	100NF	5322 121 40323
C 0016	100V 10%	100NF	5322 121 40323
C 0017	-20+80%	10NF	4822 122 30043
C 0018	-20+80%	10NF	4822 122 30043
C 0019	-20+80%	10NF	4822 122 30043
C 0020	-20+80%	10NF	4822 122 30043
C 0021	-20+80%	10NF	4822 122 30043

7.19.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0001	UA741CN	4822 209 80617
D 0002	NE5008N	5322 209 85791
D 0003	HEF40174BD	4822 209 10283
D 0004	HEF40174BD	4822 209 10283
D 0005	HEF4050BD	4822 209 10261
D 0007	HEF4072BD	4822 209 10308
D 0008	HEF4528BD	4822 209 10277
D 0009	HEF40097BD	4822 209 10317
D 0010	HEF40097BD	4822 209 10317
D 0011	HEF40097BD	4822 209 10317
D 0012	HEF40097BD	4822 209 10317
D 0014	HEF4049BD	4822 209 10306
D 0015	HEF4023BD	4822 209 10252
D 0016	HEF4093BD	5322 209 14927
D 0017	HEF40097BD	4822 209 10317
D 0018	HEF40097BD	4822 209 10317
D 0019	HEF4071BD	4822 209 10307
D 0020	HEF4013BD	4822 209 10248
D 0021	HEF4013BD	4822 209 10248
D 0022	HEF4528BD	4822 209 10277
D 0023	HEF4071BD	4822 209 10307
D 0024	HEF40097BD	4822 209 10317
D 0025	HEF4093BD	5322 209 14927
D 0026	HEF4050BD	4822 209 10261
D 0027	HEF4013BD	4822 209 10248
D 0028	HEF4556BD	4822 209 10281
D 0029	HEF4556BD	4822 209 10281
D 0030	HEF40097BD	4822 209 10317
D 0031	HEF4013BD	4822 209 10248
D 0032	HEF4013BD	4822 209 10248
D 0033	HEF4093BD	5322 209 14927
D 0034	HEF4556BD	4822 209 10281
D 0035	HEF4556BD	4822 209 10281
D 0036	HEF40097BD	4822 209 10317
D 0037	HEF4050BD	4822 209 10261
D 0038	HEF4013BD	4822 209 10248
D 0039	HEF4556BD	4822 209 10281
D 0040	HEF40097BD	4822 209 10317

7.19.3 RESISTORS

R 0001	MR25 1% 2K15	5322 116 50767
R 0002	1W 10% 10K	5322 103 10239
R 0003	1W 10% 500E	5322 103 10238
R 0004	MR25 1% 6K19	5322 116 55426
R 0005	MR25 1% 365E	5322 116 54516
R 0006	MR25 1% 3K65	5322 116 54587
R 0008	MR25 1% 3K16	5322 116 50579
R 0009	MR25 1% 1K54	5322 116 50586
R 0010	MR25 1% 511E	4822 116 51282
R 0011	MR25 1% 681E	4822 116 51233
R 0012	MR25 1% 1K	4822 116 51235
R 0013	MR25 1% 1K	4822 116 51235
R 0014	MR25 1% 10K	4822 116 51253

Item	Description	Ordering Code
R 0015	MR25 1% 100K	4822 116 51268
R 0016	MR25 1% 100K	4822 116 51268
R 0017	MR25 1% 100K	4822 116 51268
R 0018	MR25 1% 100K	4822 116 51268
R 0019	MR25 1% 100K	4822 116 51268
R 0020	MR25 1% 100K	4822 116 51268
R 0021	VR25 5% 1M8	4822 110 72194
R 0022	MR25 1% 100K	4822 116 51268
R 0023	MR25 1% 1K	4822 116 51235
R 0024	MR25 1% 1K	4822 116 51235
R 0025	MR25 1% 1K	4822 116 51235
R 0026	MR25 1% 1K	4822 116 51235
R 0027	MR25 1% 1K	4822 116 51235
R 0028	MR25 1% 1K	4822 116 51235
R 0029	MR25 1% 1K	4822 116 51235
R 0030	MR25 1% 100K	4822 116 51268
R 0031	MR25 1% 1K	4822 116 51235
R 0032	MR25 1% 1K	4822 116 51235
R 0033	MR25 1% 100K	4822 116 51268
R 0034	MR25 1% 1K	4822 116 51235
R 0035	MR25 1% 100K	4822 116 51268
R 0036	MR25 1% 100K	4822 116 51268
R 0037	MR25 1% 100K	4822 116 51268
R 0040	7X0.2W 2% 100K	5322 111 94254
R 0041	7X0.2W 2% 100K	5322 111 94254

7.19.4 SEMICONDUCTORS

V 0001	CQY24B-III	4822 130 31144
V 0002	BAW62	4822 130 30613
V 0003	1N823	5322 130 34405
V 0004	BAW62	4822 130 30613
V 0005	BAW62	4822 130 30613
V 0006	BAW62	4822 130 30613
V 0007	BAW62	4822 130 30613
V 0008	BAW62	4822 130 30613
V 0009	BAW62	4822 130 30613
V 0010	BAW62	4822 130 30613
V 0011	BAW62	4822 130 30613
V 0012	BAW62	4822 130 30613
V 0013	BAW62	4822 130 30613
V 0014	BAW62	4822 130 30613
V 0015	BAW62	4822 130 30613

7.19.5 MISCELLANEOUS

PW CON DIPSOLD	5322 265 64104

Item	Description	Ordering Code

7.20 SHUTTER SPINNER DRIVE CARD

5322 694 14478

7.20.1 CAPACITORS

Item	Description	Ordering Code
C 0001	100V 10% 2.2UF	5322 121 44246
C 0002	100V 10% 220NF	4822 121 40232
C 0003	-10+50% 47UF	4822 124 20948
C 0004	-10+50% 47UF	4822 124 20948
C 0005	-20+80% 22NF	4822 122 30103
C 0006	16V 20% 15UF	4822 124 20977
C 0007	-20+80% 22NF	4822 122 30103
C 0008	-10+50% 1000UF	5322 124 24249
C 0009	-10+50% 100UF	4822 124 20808
C 0010	-10+50% 150UF	5322 124 24138
C 0011	100V 10% 2.2UF	5322 121 44246
C 0012	100V 10% 2.2UF	5322 121 44246
C 0013	400V 10% 220NF	5322 121 41836
C 0014	400V 10% 220NF	5322 121 41836

7.20.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0001	HEF4013BD	4822 209 10248
D 0002	HEF4047BD	4822 209 10259
D 0003	HEF4528BD	4822 209 10277
D 0004	HEF4093BD	5322 209 14927
D 0005	CNX36	5322 130 90097
D 0006	CNX36	5322 130 90097

7.20.3 RESISTORS

Item	Description	Ordering Code
R 0001	CR25 5% 1M2	4822 110 72189
R 0002	MR25 1% 28K7	5322 116 54653
R 0003	CR25 5% 1M2	4822 110 72189
R 0004	3.5W 5% 100E	4822 112 21081
R 0005	MR25 1% 511K	5322 116 55258
R 0006	MR25 1% 1K	4822 116 51235
R 0007	MR25 1% 100K	4822 116 51268
R 0008	MR25 1% 7K5	5322 116 54608
R 0009	MR25 1% 12K1	5322 116 50572
R 0010	MR25 1% 1K	4822 116 51235
R 0011	MR25 1% 100K	4822 116 51268
R 0012	MR25 1% 10K	4822 116 51253
R 0013	MR25 1% 100K	4822 116 51268
R 0014	PR37 5% 3K3	4822 116 51149
R 0015	PR37 5% 4K7	4822 116 51155
R 0016	MR25 1% 5K11	5322 116 54595
R 0017	MR25 1% 46K4	5322 116 50557
R 0018	MR25 1% 1K	4822 116 51235
R 0019	MR25 1% 12K1	5322 116 50572
R 0020	MR25 1% 12K1	5322 116 50572
R 0021	MR25 1% 12K1	5322 116 50572
R 0022	MR25 1% 12K1	5322 116 50572
R 0023	MR25 1% 205E	5322 116 55365
R 0024	MR25 1% 681K	5322 116 55284
R 0025	MR25 1% 681K	5322 116 55284
R 0026	MR25 1% 10K	4822 116 51253
R 0027	MR25 1% 10K	4822 116 51253
R 0028	MR25 1% 100K	4822 116 51268
R 0029	MR25 1% 12K1	5322 116 50572

Item	Description	Ordering Code
7.20.4	SEMICONDUCTORS	
V 0001	BT139-800E	5322 130 20159
V 0002	BAV21	4822 130 30842
V 0004	BD682	5322 130 44695
V 0005	BC557B	4822 130 44568
V 0006	BAV21	4822 130 30842
V 0007	BZX79-C3V0	4822 130 31251
V 0008	BY527	4822 130 31509
V 0009	BZX79-C12	4822 130 34197
V 0011	BY527	4822 130 31509
V 0012	BY527	4822 130 31509
V 0013	BC557B	4822 130 44568
V 0014	BC557B	4822 130 44568
V 0015	BAV21	4822 130 30842
V 0016	BAV21	4822 130 30842
V 0017	CQY95	4822 130 30923
V 0018	BAV21	4822 130 30842
V 0019	BAV21	4822 130 30842
7.20.5	MISCELLANEOUS	
	PW CON DIPSOLD	5322 265 64082
	CON RH BUS	5322 267 54187
F 0001	T 5X20 250MA	4822 253 30013
K 0001	312-4C-4.5H	5322 280 74101
K 0002	311-2C-24H	5322 280 24111
K 0003	311-2C-24H	5322 280 24111
7.21	CABLE CARD "SHUTTER/CHANGER"	5322 694 14482
7.22	MULTIPLE OUTPUT POWER SUPPLY CARD	5322 694 14474
7.22.1	CAPACITORS	
C 0001	25V 20% 2.2UF	4822 124 21255
C 0002	100V 10% 220NF	4822 121 40232
C 0003	-20+80% 22NF	4822 122 30103
C 0004	100V 10% 100NF	5322 121 40323
C 0005	100V 10% 220NF	4822 121 40232
C 0006	-20+80% 22NF	4822 122 30103
C 0007	100V 10% 100NF	5322 121 40323
C 0008	100V 10% 220NF	4822 121 40232
C 0009	-20+80% 22NF	4822 122 30103
C 0010	25V 20% 2.2UF	4822 124 21255
C 0011	10% 1NF	4822 122 30027
C 0012	-20+80% 22NF	4822 122 30103
C 0013	-10+50% 470UF	5322 124 24186
C 0014	100V 10% 220NF	4822 121 40232
C 0015	100V 10% 100NF	5322 121 40323
C 0016	-20+80% 22NF	4822 122 30103
C 0017	-20+50% 10NF	4822 122 31414
C 0018	2% 100PF	4822 122 31504

7.22.2 INTEGRATED CIRCUITS

Item	Description	Ordering Code
D 0002	LM324N	4822 209 80587
D 0004	UA723CN	5322 209 85889

7.22.3 RESISTORS

Item	Description	Ordering Code
R 0001	MR25 1% 619E	4822 116 51232
R 0002	MR25 1% 5K11	5322 116 54595
R 0003	MR25 1% 1K	4822 116 51235
R 0004	MR25 1% 681K	5322 116 55284
R 0005	MR25 1% 5K11	5322 116 54595
R 0006	MR25 1% 1K54	5322 116 50586
R 0007	MR25 1% 3K48	5322 116 55367
R 0008	MR25 1% 274E	5322 116 54504
R 0009	MR25 1% 274E	5322 116 54504
R 0010	MR25 1% 274E	5322 116 54504
R 0011	MR25 1% 12K1	5322 116 50572
R 0012	MR25 1% 1K	4822 116 51235
R 0013	MR25 1% 1K	4822 116 51235
R 0014	MR25 1% 1K	4822 116 51235
R 0016	MR25 1% 10K	4822 116 51253
R 0017	MR25 1% 10K	4822 116 51253
R 0018	MR25 1% 274E	5322 116 54504
R 0020	MR25 1% 487K	5322 116 51358
R 0021	MR25 1% 10K	4822 116 51253
R 0022	MR25 1% 1K	4822 116 51235
R 0023	MR25 1% 487K	5322 116 51358
R 0024	MR25 1% 402E	5322 116 54519
R 0025	MR25 1% 105E	5322 116 54472
R 0026	MR25 1% 10K	4822 116 51253
R 0027	MR25 1% 2K05	5322 116 50664
R 0028	MR25 1% 10K	4822 116 51253
R 0029	MR25 1% 100K	4822 116 51268
R 0030	MR25 1% 10K	4822 116 51253
R 0031	MR25 1% 1K	4822 116 51235
R 0032	MR25 1% 274E	5322 116 54504
R 0033	MR25 1% 274E	5322 116 54504
R 0034	MR25 1% 511E	4822 116 51282
R 0035	MR25 1% 12K1	5322 116 50572
R 0036	MR25 1% 1K	4822 116 51235
R 0037	MR25 1% 1K	4822 116 51235
R 0038	MR25 1% 2K26	5322 116 50675
R 0039	MR25 1% 1K21	5322 116 54557
R 0040	MR25 1% 2K26	5322 116 50675
R 0042	MR25 1% 100K	4822 116 51268
R 0043	MR25 1% 10K	4822 116 51253
R 0044	MR25 1% 100K	4822 116 51268
R 0045	MR25 1% 464E	5322 116 50536
R 0046	MR25 1% 750E	4822 116 51234
R 0048	MR25 1% 10K	4822 116 51253
R 0049	MR25 1% 4K87	5322 116 55445
R 0050	MR25 1% 2K74	5322 116 50636
R 0051	MR25 1% 1K54	5322 116 50586
R 0052	MR25 1% 1K	4822 116 51235
R 0053	MR25 1% 8K25	5322 116 54558
R 0054	MR25 1% 1K	4822 116 51235
R 0055	MR25 1% 274E	5322 116 54504
R 0056	MR25 1% 274E	5322 116 54504

Item	Description	Ordering Code
R 0057	MR25 1% 121E	5322 116 54426
R 0058	MR25 1% 12K1	5322 116 50572
R 0059	MR25 1% 274E	5322 116 54504
R 0060	MR25 1% 274E	5322 116 54504
R 0061	MR25 1% 274E	5322 116 54504
R 0062	MR25 1% 12K1	5322 116 50572
R 0063	3.5W 10% 1E2	5322 113 80327
R 0064	3.5W 10% 1E2	5322 113 80327
R 0065	3.5W 10% 1E2	5322 113 80327

7.22.4 SEMICONDUCTORS

Item	Description	Ordering Code
V 0001	BAX12A	5322 130 34605
V 0002	CQY95A	4822 130 30923
V 0003	CQY95A	4822 130 30923
V 0004	CQY95A	4822 130 30923
V 0005	CQY95A	4822 130 30923
V 0006	BAX12A	5322 130 34605
V 0007	CQY95A	4822 130 30923
V 0008	CQY95A	4822 130 30923
V 0009	CQY95A	4822 130 30923
V 0010	BAX12A	5322 130 34605
V 0011	CQY95A	4822 130 30923
V 0012	CQY95A	4822 130 30923
V 0013	CQY95A	4822 130 30923
V 0014	CQY95A	4822 130 30923
V 0015	GL2 0.5MA	4822 134 20128
V 0016	UA7912UC	5322 209 81179
V 0017	BAX12A	5322 130 34605
V 0018	BAX12A	5322 130 34605
V 0019	BC557B	4822 130 44568
V 0020	BZX79-C15	4822 130 34281
V 0021	BZX79-C9V1	4822 130 30862
V 0022	BT151-500R	5322 130 24081
V 0023	BC547B	4822 130 40959
V 0024	BC547B	4822 130 40959
V 0025	1N823	5322 130 34405
V 0026	BZX79-C33	4822 130 34142
V 0027	BZX79-C18	4822 130 31024
V 0028	BZX79-C27	4822 130 34379
V 0029	BZX79-C9V1	4822 130 30862
V 0030	BC557B	4822 130 44568
V 0031	UA7824UC	5322 209 86026
V 0032	BC557B	4822 130 44568
V 0033	BT151-500R	5322 130 24081
V 0034	BC547B	4822 130 40959
V 0035	BD681	5322 130 44786
V 0036	BT151-500R	5322 130 24081
V 0037	BZX79-C5V6	4822 130 34173
V 0038	BC557B	4822 130 44568
V 0039	BZX79-C15	4822 130 34281
V 0040	BC557B	4822 130 44568
V 0041	BT151-500R	5322 130 24081
V 0042	BC557B	4822 130 44568
V 0043	UA7812UC	5322 209 86176
V 0044	BAW62	4822 130 30613
V 0045	BAW62	4822 130 30613
V 0046	BZX79-C6V2	4822 130 34167

Item	Description	Ordering Code
7.22.5	MISCELLANEOUS	
	PW CON DIPSOLD	5322 265 64104
	CON RH PEN	5322 265 64109
	WASHER TO-220	4822 255 40174
	MICA PLAAT	4822 255 40161

7.23 POWER UNIT PW1710 RECTIFIER CARD 5322 694 14504

7.23.1 CAPACITORS

C 0001	CAP,ELECTROLYT.	-10+50%	100UF	5322 124 24178
C 0002	CAP,ELECTROLYT.	-10+50%	330UF	5322 124 24192
C 0003	CAPACITOR,FOIL	400V 10%	10NF	5322 121 44201
C 0004	CAPACITOR,FOIL	400V 10%	10NF	5322 121 44201

7.23.2 RESISTORS

R 0001	RESISTOR,M.FILM MR25	1%	1K	4822 116 51235

7.23.3 SEMICONDUCTORS

V 0001	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0002	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0003	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0004	TRANSIST,PHOTO	CNX36	5322 130 90097
V 0005	TRANSIST,PHOTO	CNX36	5322 130 90097
V 0006	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0007	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0008	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031
V 0009	BRIDGE RECT.	SKB2/08 L5A	5322 130 32031

7.24 PW1710 POWER SUPPLY "MAINFRAME"

7.24.1 CAPACITORS

C 0101	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181
C 0102	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181
C 0103	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181
C 0104	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181
C 0105	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181
C 0106	CAP,ELECTROLYT.	-10+30%	3300UF	5322 124 74181

Item Description Ordering Code

7.24.2 SEMICONDUCTORS

Item	Description		Ordering Code
V 0100	DIODE	BY261-600	5322 130 31497
V 0101	TRANSISTOR	BDX65A	4822 130 40997

7.24.3 MISCELLANEOUS

Item	Description		Ordering Code
F 0100	FUSE	T 5X20 1,6A	4822 253 30024
F 0101	FUSE	T 5X20 1,6A	4822 253 30024
F 0102	FUSE	T 5X20 1,6A	4822 253 30024
F 0103	FUSE	T 5X20 6,3A	4822 253 30031
F 0104	FUSE	T 5X20 6,3A	4822 253 30031
F 0105	FUSE	T 5X20 1,6A	4822 253 30024
F 0106	FUSE	T 5X20 100MA	4822 253 30006
F 0107	FUSE	T 5X20 200MA	4822 253 30012
F 0108	FUSE	T 5X20 200MA	4822 253 30012
F 0109	FUSE	T 5X20 200MA	4822 253 30012
F 0110	FUSE	T 5X20 50MA	4822 253 30003
F 0114	FUSE	T 5X20 315MA	4822 253 30014
F 0115	FUSE	T 5X20 1,25A	4822 253 30022
F 0116	FUSE	T 5X20 100MA	4822 253 30006
F 0117	FUSE	T 5X20 800MA	4822 253 30019
F 0118	FUSE	T 5X20 1,25A	4822 253 30022
F 0119	FUSE	T 5X20 4A	4822 253 30028
S 0100	SWITCH,TUMBLER	2P 2ST 250V 16A	5322 277 10167
Z 0100	FILTER,MAINS	10A	5322 219 80589

7.25 SECONDARY CONTROL PANEL FOR PW1748 5322 694 14724

For spare parts refer to paragraph 7.7

7.26 SPARE PARTS KIT PW1718

ITEM	QTY	ORDERING CODE	DESCRIPTION
		5322 694	
1.	1	14514	4-BIT BINARY COUNTER
2.	1	14333	RATE-METER
3.	1	14332	WINDOW CONTROL
4.	1	14331	AMPLIFIER / ANALYZER
5.	1	14335	STEPPER MOTOR SUPPLY DRIVER
6.	1	14472	GONIOMETER CONTROL
7.	1	14471	DISPLAY KEYBOARD CONTROL
8.	1	14502	DISPLAY KEYBOARD CARD
9.	1	14503	SECONDARY CONTROL PANEL
10.	1	14473	SYSTEM CONTROLLER
11.	1	14474	MULTIPLE OUTPUT POWER SUPPLY
12.	1	14504	RECTIFIER CARD
13.	1	14477	RECORDER CONTROL
14.	1	14511	HV 2000
15.	2	5322 124 74181	CAPACITOR ELCO 3300 uF ,40V , -10 / +30%
16.	1	5322 130 34788	BRIDGE RECTIFIER SCBE1
17.	2	4822 130 40997	LF TRANSISTOR BDX 65A
18.	3	4822 267 14338	TIP SWITCH

NOTE: If your system has any options fitted, we recommend that you also hold spare cards as follows:

PW1712	.....	Dual Serial Interface, 5322 694 14475.
PW1713	.....	Changer/Spinner/Shutter Control, 5322 694 14476 Shutter/Spinner Driver, 5322 694 14478.
PW1714	.....	Shutter/Spinner Driver, 5322 694 14478.
PW1717	.....	Interface for PW1170, 5322 694 14479.
PW1747	.....	Use the spare cards recommended above, BUT , check the address settings on the card as described in Section 2.5.8 of this manual.
PW1748	.....	Use the spare cards recommended above, BUT , check the address settings on the card as described in Section 2.5.9 of this manual.

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A.1 PW1710/00 Wiring Diagram A-8

NOTES

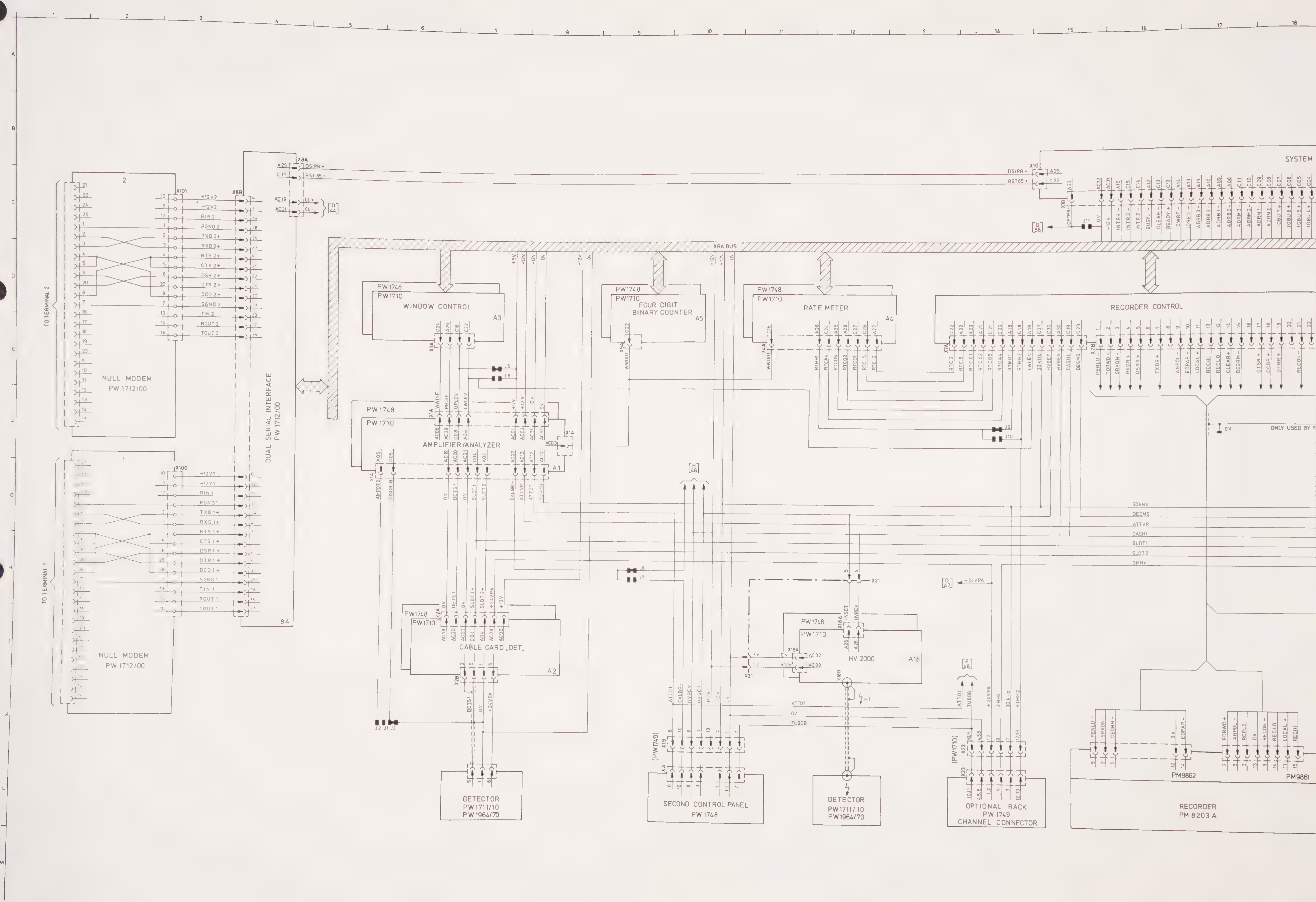
Read the following notes before using figure A.1:

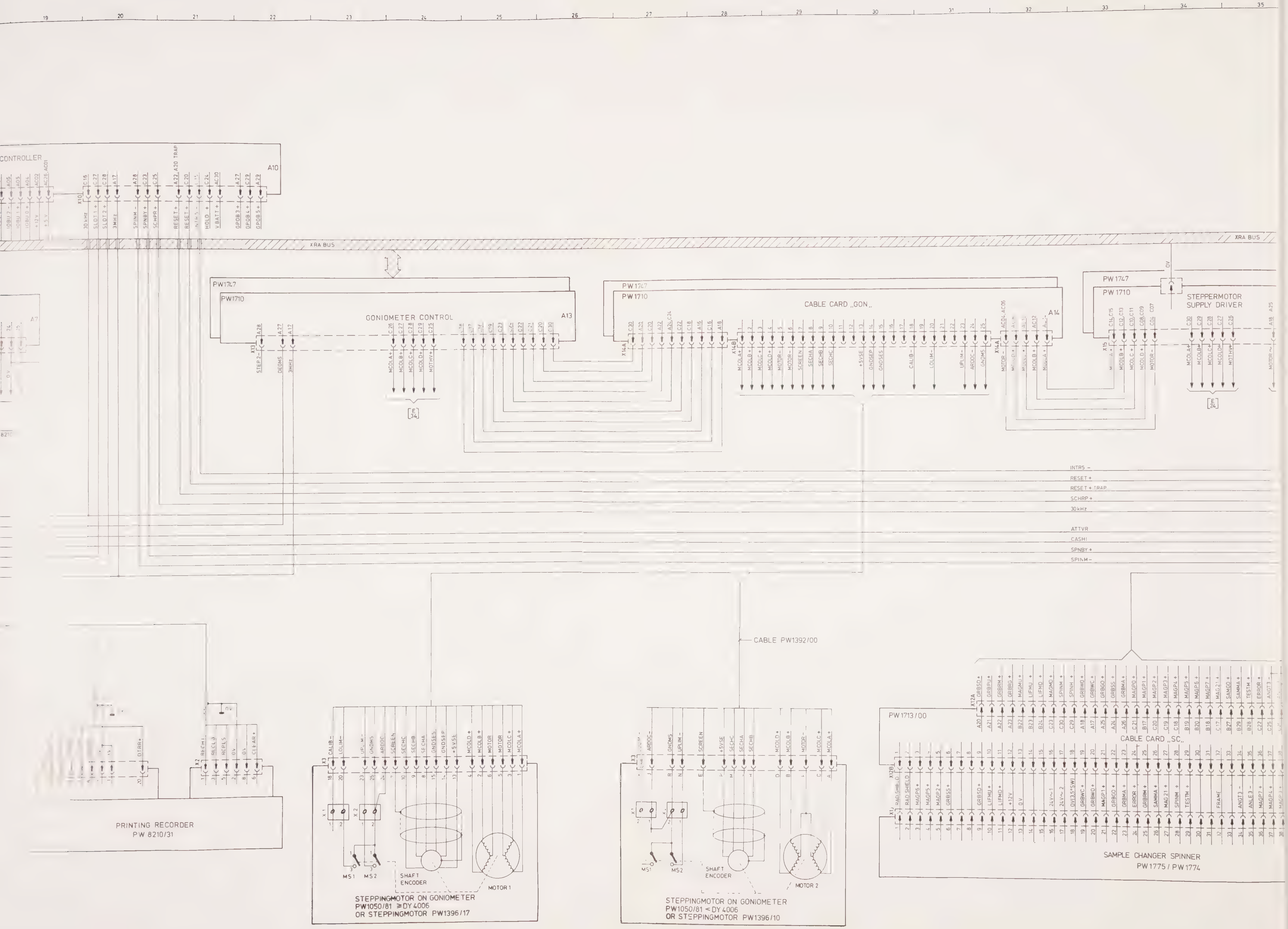
NOTE 1: Figure A.1 shows the wiring for the complete PW1710 with all of the possible options.

NOTE 2: Two of the options (PW1747 and PW1748) consist of cards that must be fitted into the Options Rack PW1749, these cards are the same as those used for the first counting channel and/or stepping motor and have the same connections (the only difference is their addresses).

Note 3: If the Options Rack PW1749 is present, the wiring in it is the same as the PW1710/00 but they have to be connected together by coupling (with cables) connectors X23, X24 and X25 of both units.

Note 4: If the PW1748 option is present the Secondary Control Panel in the Options Rack must also be connected to X19 of the Options Rack PW1749 as shown in figure A.1 ´M-5,6¸.


SYSTEM
TO TERMINAL 2
NULL MODEM
PW 1712/00
TO TERMINAL 1
NULL MODEM
PW 1712/00
DUAL SERIAL INTERFACE
PW 1712/00
8A
X8A
X8B
X101
X100
+12V2
-12V2
RIN 2
PGND 2
TXD 2+
RXD 2+
RTS 2+
CTS 2+
DSR 2+
DTR 2+
DCD 2+
SGND 2
TIN 2
ROUT 2
TOUT 2
+12V1
-12V1
RIN 1
PGND 1
TXD 1+
RXD 1+
RTS 1+
CTS 1+
DSR 1+
DTR 1+
DCD 1+
SGND 1
TIN 1
ROUT 1
TOUT 1
DSIPR +
RST 65 +
CL +
CL -
XRA BUS
PW 1748
PW 1710
WINDOW CONTROL
A3
FOUR DIGIT
BINARY COUNTER
A5
RATE METER
A4
RECORDER CONTROL
AMPLIFIER/ANALYZER
A1
CABLE CARD DET.
A2
HV 2000
A18
DETECTOR
PW 1711/10
PW 1964/70
SECOND CONTROL PANEL
PW 1748
(PW1749)
DETECTOR
PW 1711/10
PW 1964/70
OPTIONAL RACK
PW 1749
CHANNEL CONNECTOR
(PW1710)
RECORDER
PM 8203 A
PM9862
PM9861
ONLY USED BY P
30kHz
DEGMS
ATTVR
CASHI
SLOT1
SLOT2
3MHz
+24VPA
ATTOT
TLB08
HT
X21
J1
J2
J3
J5
J6
J7
J8
J9
J10
J11


CONTROLLER
A10
XRA BUS
PW1747
PW1710
GONIOMETER CONTROL
A13
CABLE CARD ,,GON,,
A14
STEPPERMOTOR
SUPPLY DRIVER
INTRS –
RESET +
RESET + TRAP
SCHRP +
30kHz
ATTVR
CASHI
SPNBY +
SPINM –
CABLE PW1392/00
PW1713/00
CABLE CARD ,,SC,,
SAMPLE CHANGER SPINNER
PW1775 / PW1774
PRINTING RECORDER
PW 8210/31
SHAFT ENCODER
MOTOR 1
MOTOR 2
MS1
MS2
STEPPINGMOTOR ON GONIOMETER
PW1050/81 ≥DY 4006
OR STEPPINGMOTOR PW1396/17
STEPPINGMOTOR ON GONIOMETER
PW1050/81 <DY 4006
OR STEPPINGMOTOR PW1396/10

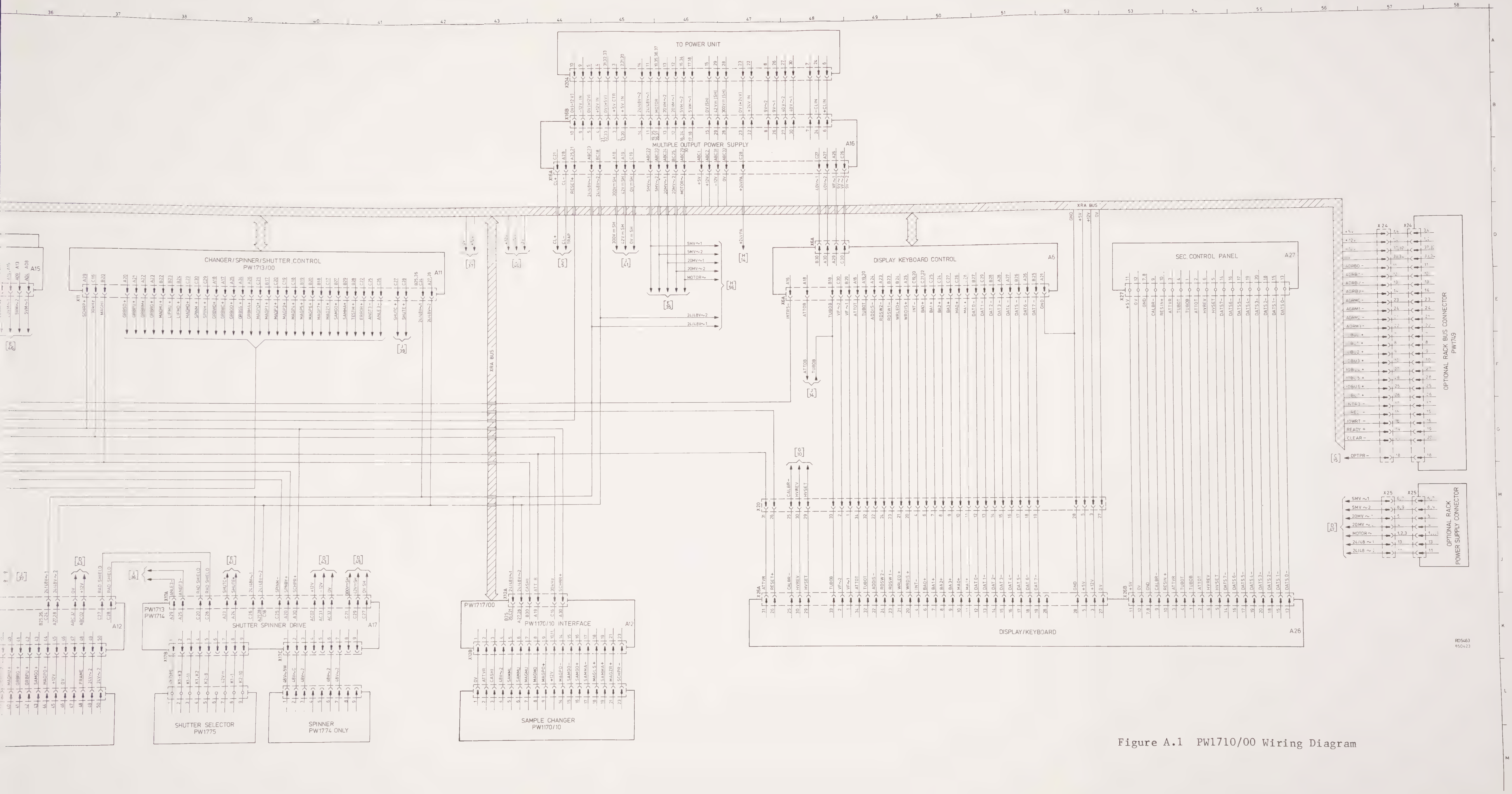

TO POWER UNIT
X20A
X16B
MULTIPLE OUTPUT POWER SUPPLY
A16
X16A
XRA BUS
CHANGER/SPINNER/SHUTTER CONTROL
PW1713/00
A11
A15
DISPLAY KEYBOARD CONTROL
A5
X6A
SEC. CONTROL PANEL
A27
X27
OPTIONAL RACK BUS CONNECTOR
PW1749
X24
OPTIONAL RACK POWER SUPPLY CONNECTOR
X25
5MV~1
5MV~2
20MV~1
20MV~2
MOTOR~
24/48V~1
24/48V~2
X20
A12
PW1713
PW1714
X17A
SHUTTER SPINNER DRIVE
A17
X17B
X17C
PW1717/00
X12A
PW1170/10 INTERFACE
X12B
X26A
X26B
DISPLAY/KEYBOARD
A26
SHUTTER SELECTOR
PW1775
SPINNER
PW1774 ONLY
SAMPLE CHANGER
PW1170/10
RD5463
950423

Figure A.1 PW1710/00 Wiring Diagram

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Figure B.7 Two Wire Current Loop Wiring B-13

B.1 INTRODUCTION

Certain protocols are provided to enable communication in a serial binary form between different devices. These protocols are given in EIA-RS232C or CCITT-V24.

EIA: Electronic Industries Association (USA)
CCITT: Comitê Consultatif International de Telephonie et Telegraphie (Europe)

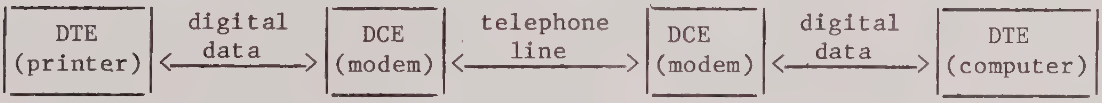
The way in which they are used is that each end of a communications link is strictly controlled according to the protocol. With these protocols a serial link is used to send data in a character serial, bit serial form. It has the advantage that only a few lines are required, but the speed is limited.

B.2 LINKING DATA EQUIPMENT TOGETHER

B.2.1 VIA THE TELEPHONE LINE

A piece of equipment which is able to transmit and receive digital data (VDU, printer, computer) is called a "data terminal equipment" (DTE). Normally a telephone line (switched network or leased lines) is used to connect two DTEs (for example: a printer and a computer, or, computer and computer) to each other. The link between the DTE and the telephone line is made with a modem (MOdulator/DEModulator), which is called a "data communications equipment" DCE. This equipment converts pulse trains into a modulated signal, and vice-versa.

A typical set-up could be the following:



A major principle of this type of serial communication is that the lines between DTE and DCE each have a clearly defined use. Each DTE must have a 25 pin connector (with male contacts), and most of these pins have a specific purpose. The pins have the same functions for EIA and CCITT, the only difference being in the circuit designation. Table B.1 shows how these 25 pins are allocated:

It is possible to have two complete channels using these protocols (a primary channel, and a secondary channel). A secondary channel is only required if two channels with different signal rates have to share a common interface connector.

As there are separate input and output data lines each channel, data can flow in two directions simultaneously (full duplex mode). If only one direction of data flow is to be used (half duplex mode), an aggreed character must be used to "turn the line around".

All of the functions mentioned in table B.1 are not required in every system set-up, and in practice, each manufacturer of DTEs makes his own selections. A quite commonly used subset of V24 (standard for x-ray) is shown in table B.2.

Table B.1 Pin Allocation

PIN Nr.	DESIGNATION EIA	CCITT	TYPE	FROM	DESCRIPTION (seen from the DTE)
1	AA	101	Ground	-	Protective Ground
2	BA	103	Data	DTE	Transmitted Data
3	BB	104	Data	DCE	Received Data
4	CA	105	Control	DTE	Request To Send
5	CB	106	Control	DCE	Clear To Send
6	CC	107	Control	DCE	Data Set Ready
7	AB	102	Ground	-	Signal Ground (Common Return)
8	CF	109	Control	DCE	Received Line Signal Detector
9	-	-	Testing		Reserved for data set testing
10	-	-	Testing		Reserved for data set testing
11	-	-	Unassigned		
12	SCF	122	Control	DCE	Second. Rec´d Line Signal Detector
13	SCB	121	Control	DCE	Secondary Clear To Send
14	SBA	118	Data	DTE	Secondary Transmitted Data
15	DB	114	Timing	DCE	Transmission Signal Element Timing
16	SBB	119	Data	DCE	Secondary Received Data
17	DD	115	Timing	DCE	Receiver Signal Element Timing
18	-	-	Unassigned		
19	SCA	120	Control	DTE	Secondary Request To Send
20	CD	108.2	Control	DTE	Data Terminal Ready
21	CG	110	Control	DCE	Signal Quality Detector
22	CE	125	Control	DCE	Ring Indicator
23	CH/	111/	Control	DTE/	Data Signal Rate Selector
"	CI	112	Control	DCE	Data Signal Rate Selector
24	DA	113	Timing	DTE	Transmit Signal Element Timing
25	-	-	Unassigned		

Table B.2 V24 Sub-set for x-ray

PIN Nr.	MNEMONIC for x-ray	TYPE	FROM	DESCRIPTION
1	F.GND	Ground	-	Frame (protective) ground
2	TxD	Data	DTE	Transmitted data
3	RxD	Data	DCE	Received data
4	RTS	Control	DTE	Request to send
5	CTS	Control	DCE	Clear to send (Ready to transmit)
6	DSR	Control	DCE	Data set ready
7	S.GND	Ground	-	Signal ground
8	DCD	Control	DCE	Data carrier detected from remote DCE (Ready to receive)
20	DTR	Control	DTE	Data terminal ready

The lines, mentioned above, can be divided into three main groups:

Ground connections
Data lines
Control/handshake lines

The use of the first two groups is obvious; the third group is used to provide a hardware handshake. Handshaking is a method of confirming that the transmission path is present, and working, before the data is transmitted; and, telling the DTE that a signal has been received. The signals involved in the hardware handshake are:

DTR	prepares the DCE to be connected to the communications channel (telephone line).
DSR	indicates that the DCE is connected to the communications channel and ready to operate.
RTS	the request from the DTE to transmit.
CTS	indicates that the DCE is ready to transmit.
DCD	the DCE indicates to the DTE that a carrier wave has been received.

The first four signals (DTR, DSR, RTS and CTS) are all involved in the transmission channel, and must all be present before the DTE can transmit.

The connection between a DTE and a DCE is shown in figure B.1.

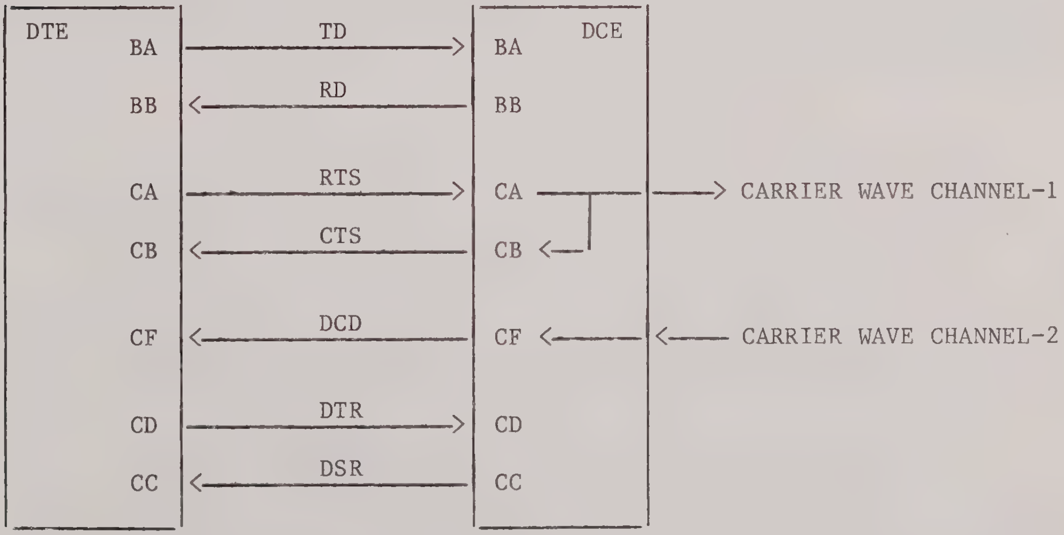


Figure B.1 Hardware connection lines

If required, the hardware handshake lines are used during transmission as a "pause" mechanism. If for example, an input buffer is full, it can ask for a pause by causing one of the lines to be switched "low", this will stop the transmission until that line is switched "high" again.

Another handshake method is a software-based one. In this case, control signals are used instead of special lines. Only ground connections and data lines are used (data-only wiring). If software controlled transmission is used, the hardware handshake lines must all be connected so that they are permanantly in the "ON" condition.

B.2.2 SHORT DISTANCES WITHOUT MODEM

When the two connected DTEs are located close together (like x-ray equipment and its printer), a telephone line is not needed. Then the two modems and the telephone line are replaced by a device, called a null modem or a modem eliminator.

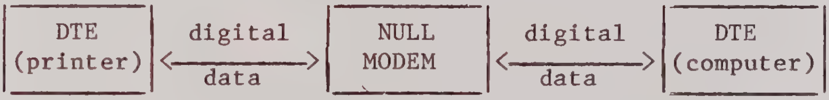

DTE
(printer)
digital
data
NULL
MODEM
digital
data
DTE
(computer)

Figure B.2 Null Modem

It is a simple box or a cable with two female connectors, a number of crossed wires and a number of jumpers in it, it can be wired such that it resembles a modem (DCE) to both DTEs and can be adapted to various interpretations of V24. The wiring could be as shown in figure B.3 (and is the standard for x-ray equipment):

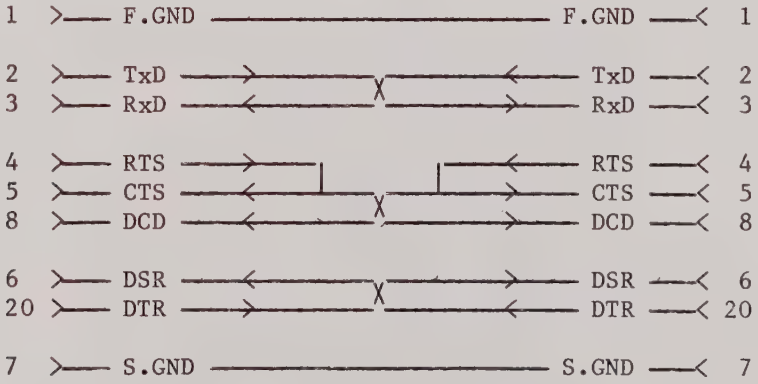

1 F.GND
F.GND 1
2 TxD
3 RxD
TxD 2
RxD 3
4 RTS
5 CTS
8 DCD
RTS 4
CTS 5
DCD 8
6 DSR
20 DTR
DSR 6
DTR 20
7 S.GND
S.GND 7

Figure B.3 Standard Null Modem Wiring

The functions of the lines remain the same as in a normal DTE/DCE set-up over telephone lines.

When a data-only link is used, a four wire connection is required. Additional wires could cause a problem (for instance a DEC PDP11 computer in NO REMOTE mode will switch all handshake signals low). Therefore, either the extra wires should be removed, or a null modem wired as shown in figure B.4 should be used. If this sort of modem is used, a terminal (like for example, the PW1710) must be switched to data only.

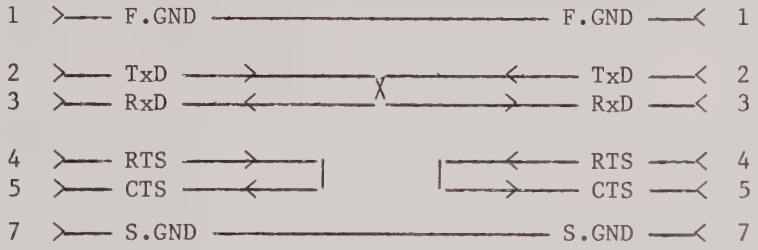


Figure B.4 Modified Null Modem wiring

B.3 TECHNICAL SPECIFICATIONS OF THE BIT STREAM

B.3.1 SPEED

Each character is serialised in the transmitter, and each bit (least significant bit first) is put on the line for a fixed time (bit time).

The number of bits which can be transmitted per second is the baud rate . The standard series of baud rates is 50, 75, 110, 134.5, 150, 200, 300, 600, 1200, 1800, 2400, 4800, 9600 and 19200 baud.

B.3.2 LEVELS

EIA-RS232C defines two logic levels.
HIGH = a voltage more positive than +3V d.c. (max. +25V d.c.).
LOW = a voltage more negative than -3V d.c. (min. -25V d.c.).

Levels, according to EIA-RS232C, and their meanings are:

level	voltage	state name	bit type		
			frame bit	control bit	data bit
HIGH	> +3V	SPACING	START	ON	"0"
LOW	< -3V	MARKING	STOP	OFF	"1"

The area between -3V d.c. and +3V d.c. is called the transition region. Each signal must proceed through the transition region to the opposite signal state and may not re-enter this region until the next significant change of signal condition. No reversal of the direction of voltage change is allowed in this region.

B.3.3 SLEW RATES

The maximum time to pass through the transition region is:

For control lines: 1 ms.
For data and timing lines: 1 ms or 4% of the bit time, whichever is the less.

The maximum instantaneous slew rate should never exceed 30 V/us.

B.3.4 LOADS

The load impedance of the receiver must be between 3000 and 7000 ohms with a maximum capacitance of 2500 pF.

The transmitter output shall be such that, when loaded with any resistance from 3000 to 7000 ohms, the output voltage shall not be less than 5V d.c. nor exceed 15V d.c. in magnitude.

B.3.5 DISTANCES

Between DTE and DCE, or two DTEs with a null modem: not more than 15m.

B.3.6 FORMAT

To enable the receiver to determine when the transmission of a character has been completed, the format (how many bits are there in a character) has to be defined before a transfer is made.

There are two ways of transmitting a number of characters after each other:

Synchronously.

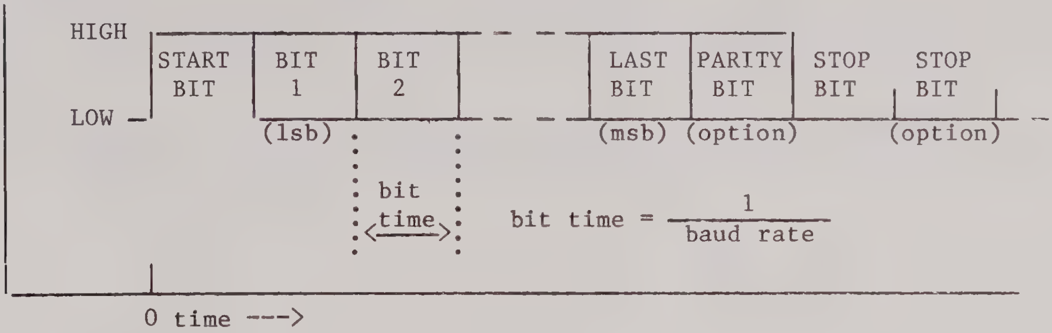
Special synchronisation characters are sent first, and then after that all data characters are sent without a pause. If a pause is unavoidable, the transmitter must continuously issue the same special characters to maintain synchronisation. This is a good solution for intensive data exchange at high speeds.

Asynchronously.

Each character is put in a frame. This frame consists of a start bit at the beginning, and one or more stop bits at the end of each character. Characters can follow each other immediately or with a pause of random length.

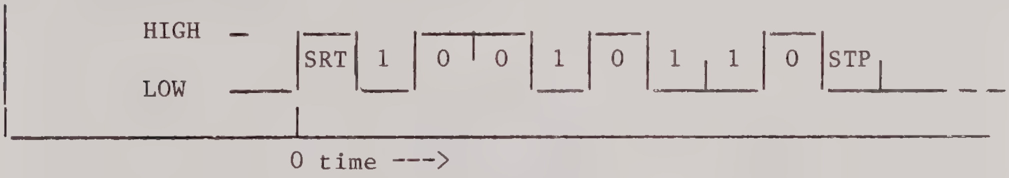
To check for a properly received character, various kinds of checks are possible. Apart from methods like checksums per block of characters, it is possible for the transmitter to add a special test bit to each character, and the receiver could test this bit. This bit, the parity bit (in asynchronous mode inserted between the last, most significant bit and the first stop bit), indicates by a logic "1" that the number of "logic one" data bits in a character is even in case of even parity check, or odd in case of odd parity check. Otherwise this bit is "0".

The general format of a character according to RS232C in asynchronous mode is as follows:

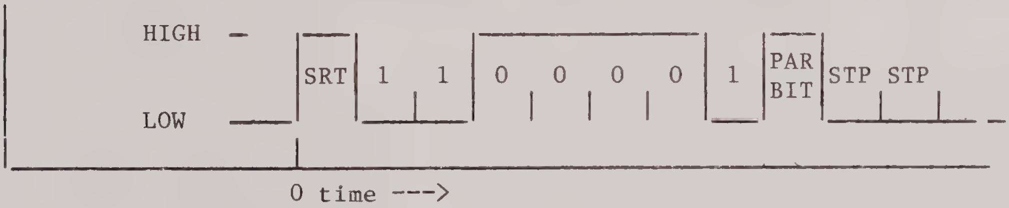

HIGH
LOW
START BIT
BIT 1
(lsb)
BIT 2
LAST BIT
(msb)
PARITY BIT
(option)
STOP BIT
STOP BIT
(option)
bit time
bit time = 1 / baud rate
0 time --->

Examples:

An 8-bit character, without parity bit, one stop bit:


HIGH
LOW
SRT
1
0
0
1
0
1
1
0
STP
0 time --->

The letter "C" in ASCII-code *), with even parity, two stop bits:


HIGH
LOW
SRT
1
1
0
0
0
0
1
PAR BIT
STP STP
0 time --->

The letter C is represented as 43 in hexadecimal, and as 1000011 in binary. Three bits (1, 2 and 7) are "1" (an odd number), therefore the parity bit is "0".

*) ASCII = American Standardisation Committee for Information Interchange.

The ASCII code uses seven bits (BIT1 to BIT7) to code all characters to be interchanged between DTEs (letters, figures, control characters and so on).

B.4 ECHO

The correct tranmission of characters between DTEs can be confirmed by transmitting these characters back to the sending DTE. This mechanism is called echoing.

When an analytical instrument is connected to a VDU, it could echo all properly received characters back to that VDU (echoplex). In that case, there should be no direct connection between the keyboard and screen of that VDU, otherwise, all the characters would appear twice on the screen (the first directly from the keyboard, and the second via echo).

Generally, software in microcomputers and minicomputers of x-ray equipment does not expect to get its output echoed back. Therefore, terminals should not echo characters that they receive from the micro or minicomputer.

B.5 CURRENT LOOP

The unused pins can be used to combine more transmission systems in one connector. Full duplex current loop can be added according to the S&I proposal as follows:

NOTE: In x-ray equipment, the two systems (current loop and V24) are not used simultaneously.

Pin no.	x-ray mnemonic	description
12	RIN	Receiver input
14	ROUT	Receiver output
13	TIN	Transmitter input
16	TOUT	Transmitter output

B.5.1 PRINCIPLE OF CURRENT LOOP

The block diagram shown in figure B.5 shows the basic current loop wiring.

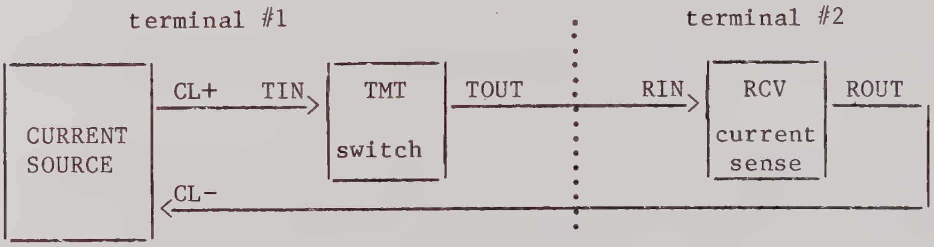


Figure B.5 Current Loop Wiring

A current source provides a constant d.c. current through the tranmitter and the receiver. Popular values for this current are 60mA (for older teletypes) and 20mA (for modern terminals).

There is no strict definition of tolerances on this nominal current value (neither ON or OFF). In practice: no current means below a certain value (for example: 2mA), and current means more than a certain value (for example: 15mA).

Switching the transmitter causes an absence or presence of current through the receiver. These two states have meanings similar to HIGH and LOW in the RS232C/V24 protocol.

B.5.2 MODES IN CURRENT LOOP

There are two modes in which current loop can operate (speed and format are the same as those described in paragraphs 3.1 and 3.6 of this Appendix), the two modes are:

QUIESCENT CURRENT PRINCIPLE. In rest, the transmitter contact is closed and a current is flowing through the receiver.

The meaning of the two states is as follows:

state	state name	bit type		
		frame bit	control bit	data bit
CURRENT	SPACING	START	ON	"0"
NO CURRENT	MARKING	STOP	OFF	"1"

WORKING CURRENT PRINCIPLE. In rest, the transmitter contact is opened and no current can flow.

The meaning of the two states is as follows:

state	state name	bit type		
		frame bit	control bit	data bit
NO CURRENT	SPACING	START	ON	"0"
CURRENT	MARKING	STOP	OFF	"1"

B.5.3 WIRING OF CURRENT LOOP CONNECTIONS

For a bi-directional connection, four wires are required.

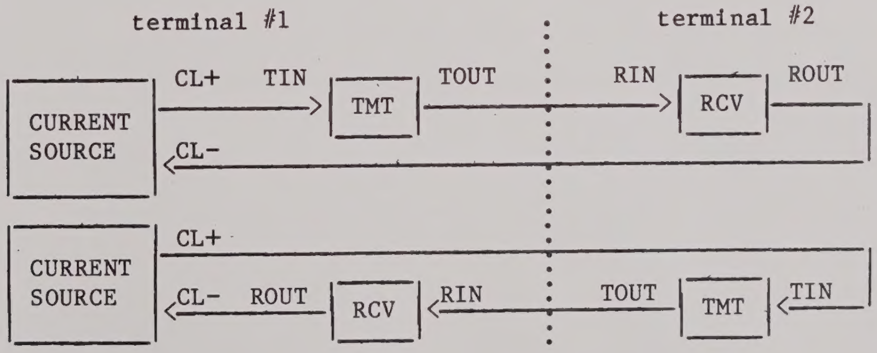


Figure B.6 Bi-directional Current Loop Wiring

In this case, a software handshake protocol could be used as well as the echoing mechanism.

The location of the current source in either terminal #1 or terminal #2 is immaterial. The terminal which is supplying the current is called active, and the terminal which is NOT supplying a current is called passive.

A two-wire connection greatly reduces the number of possibilities.

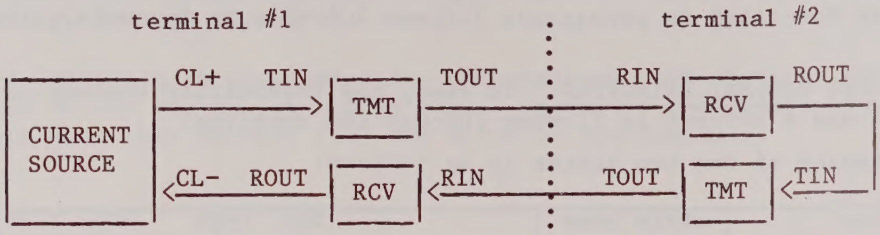

terminal #1
terminal #2
CURRENT SOURCE
CL+
TIN
TMT
TOUT
RIN
RCV
ROUT
CL-
ROUT
RCV
RIN
TOUT
TMT
TIN

Figure B.7 Two Wire Current Loop Wiring

Simultaneous transmission from both sides could mutilate characters, therefore, only half duplex is allowed (not supported by actual x-ray analytical equipment). No echo facilities are possible.

B.6 GUIDANCE

If you are going to connect a peripheral to an x-ray equipment, you should consider the following points:

- V24 or Current Loop
- Baud rate
- Number of bits per character (7 or 8)
- Number of stop bits (1 or 2)
- Parity (none/even/odd)
- Echoplex (yes/no)
- If V24: Handshake (hardware/software)
- If current loop: which side should supply the current

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